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Zero Voltage Switched Full Bridge Converters for the Battery Charger of Electric Vehicle

Rizwan Ullah, Abdar Ali, Zahid Ullah

***Abstract*—**This paper illustrates the study of three isolated zero voltage switched (ZVS) PWM full bridge (FB) converters to charge the high voltage battery in the charger of electric vehicle (EV). EV battery chargers have several challenges such as high efficiency, high reliability, low cost, isolation, and high power density. The cost of magnetic and filter components in the battery charger is reduced when switching frequency is increased. The increase in the switching frequency increases switching losses. ZVS is used to reduce switching losses and to operate the converter in the battery charger at high frequency. The performance of each of the three converters is evaluated on the basis of ZVS range, dead times of the switches, conduction losses of switches, circulating current stress, circulating energy, duty cycle loss, and efficiency. The limitations and merits of each PWM FB converter are reviewed. The converter with broader ZVS range, high efficiency and low switch stresses is selected for battery charger applications in EV.

***Keywords*—**Electric vehicle, PWM FB converter, zero voltage switching, circulating energy, duty cycle loss, battery charger.

I. Introduction

THE vehicle industries are nowadays working to reduce exhaust emissions, acoustic noise, and vibrations in order to get high conversion efficiency. This is a difficult task for the vehicle industries to achieve all these characteristics in vehicles that run on fossil fuels. Conventional vehicles, which consume fossil fuels and emit green house gasses, lead to climate changes and causes global warming. Vehicle manufacturers are diverting towards the EVs because EVs have the ability to remove the draw backs of conventional vehicles. The electricity needed to store in the batteries of EVs is obtained from the AC grid as shown in Fig. 1 [1].

The battery charger of EV consists of a rectifier, a DC/DC converter and a battery pack.The rectifier takes its input from an AC grid while the DC/DC converter generates the required voltage for the battery pack. The battery life and charging time depends upon the characteristics of modules used in the battery charger [2], [3]. These modules are manufactured worldwide by various vehicle industries for EVs. The design and charging pattern of the battery module determines the performance of the charger. High efficiency, high reliability, low cost, isolation, and high power density are the major challenges for EV battery chargers.

EV is electrically disconnected from the AC grid through galvanic isolation. This galvanic isolation in the battery charger of EV is performed using high frequency transformer in DC/DC converter.

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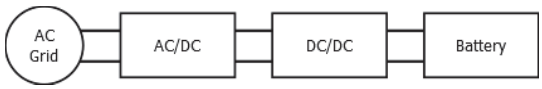

Fig. 1 Battery charger for electric vehicle

The cost of magnetic components and filter components in the battery charger is reduced by increasing the switching frequency of the DC/DC converters. A limit will also come on the maximum switching frequency due to the increase of switching losses. However, incorporation of soft switching methods reduces switching losses and operates the converter in battery charger at high frequency [4]. The conventional FB converters are typically hard switched, and the hard switching converters are not suitable to achieve high efficiency. Soft switching is incorporated in FB converters to solve the above problems. Soft switching technique i.e. zero voltage soft switching and zero current soft switching turn on/off converters at zero voltage and current, respectively.

ZVS PWM FB converters utilize the stored energy in the leakage inductance of the primary winding of power transformer and output filter inductor for obtaining ZVS [5]. Conventional ZVS PWM converters output rectifier diodes suffer from hard-switching, results in severe voltage spike and ringing across the output rectifier diodes, high switching losses, circulating current, and low efficiency [6], [7]. ZVS and ZCS reduce switching losses in converters. Conduction losses are decreased by eliminating circulating currents. Consequently, a high efficiency can be achieved for the on-board battery charger of EVs [8], [9]. Main focus of the paper is to design a 2 kW ZVS DC/DC converter to charge the high voltage battery in the on board charger of EV. Simulation of the converters has been done in PSIM to verify the design. In this paper, three isolated 2 kW DC/DC converters namely, ZVS PS PWM FB converter using leakage inductance, ZVS PS PWM FB converter using saturable inductance, and ZVS zero PS PWM FB converter using leakage inductance have been selected and designed for battery charger applications of EV. The characteristics of these converters are compared to select the suitable converter for battery charger system of EV.

The remaining paper is organized as follows: Section II discusses literature review of various ZVS PWM FB converters. Section III presents operation principles and analysis of ZVS PWM FB converters. Section IV includes the designed parameters of the selected converters for the given specifications. Section V provides the discussion on the comparison of the characteristics and simulation results of the converters. Section VI concludes the paper with future work.

II. Literature Review

ZVS PWM FB converters are broadly used in medium to high power DC/DC conversion applications such as EVs battery chargers, DC motor drives, computers, telecommunication systems, DC distributed systems, and welding machines etc [10].

Efficiency, power density, reliability and cost are the important parameters in these types of converters. In order to get high power density and small size for the converters, it is usually required to operate the converter at high frequency. However, switching power loss is proportional to high transistor switching frequency which lowers converter efficiency. Therefore, ZVS or ZCS topologies allow for high frequency operation while minimizing the switching loss. The size and cost of isolated DC/DC converters can be reduced by using high fixed frequency transformer [11]. The ZVS topologies operate at high frequency can improve the converter efficiency resulting high power densities [12].

Various types of ZVS PWM FB converters are reviewed with the objective of identifying converters with high efficiency and low circulating current, duty cycle loss, conduction losses and voltage ringing of rectifier diodes. Several ZVS topologies exist. However, not all of these ZVS topologies are feasible for the battery charger of EV.

In [13], ZVS FB PWM converter achieves ZVS with the help of transformer primary leakage inductance and the parasitic capacitances of the semiconductor switches. The energy stored in the output filter inductor and transformer primary leakage inductor help in ZVS for leading leg. ZVS in lagging leg is lost under low load condition because of the low energy stored in small primary leakage inductance [14]–[16].

When ZVS is required at low load currents, the transformer primary leakage inductance is intentionally increased and/or large external resonant inductor is connected in series with primary leakage inductance of transformer, resulting in high duty cycle loss and rectifier diodes parasitic voltage ringing [17].

A saturable resonant inductor is used to improve the performance of the converter rather than using a large linear external resonant inductor. ZVS in lagging leg is obtained over a wider load range. The duty cycle loss on the secondary side of transformer also reduces. However the saturable inductance limits the switching frequency and produces parasitic ringing across rectifier diodes [18].

In order to eliminate these problems, a classical converter in [19], [20] is proposed. Two primary clamping diodes are introduced,which clamp the voltage across the diodes present in the rectifier circuit to the reflected input voltage and the voltage oscillations are removed. The diodes in the secondary may be used with lower voltage ratings. Thus the converter efficiency is improved. The transformer primary one terminal is attached with the bridge leading leg and the primary inductor is attached with the bridge lagging leg. In this converter in one switching period, the clamping diodes conduct two times, but for voltage clamping one time conduction of the clamping diodes are necessary. The primary inductor current is freewheeling and produces higher conduction losses in zero state.

An improved ZVS FB PWM converter is proposed in [21], and the transformer and resonant inductor positions are interchanged. The lagging leg of the inverter is attached with the transformer. This topology not only reduces the voltage oscillations but the clamping diodes in the primary conduct once and reduces current of the resonant inductor in zero state, which reduces conduction losses in the primary. The clamping diodes conduct for half switching peroid at low load current and produces severe reverse recovery due to hard turned off of clamping diodes. In high input voltage applications, the clamping diodes are easily damaged. It is essential for clamping diodes to reset its current quickly to zero in zero state.

An enhanced ZVS FB PWM converter is proposed with extra auxillary transformer [22]. This auxiliary transformer forces the current of clamping diode quickly to zero over a wider load current, results in low conduction losses of clamping diodes and in the leading leg.

III. ZVS PWM Converters Operation and Analysis

A. ZVS PWM PS Converter Using Leakage Inductance

Converters with low switching losses are used in high frequency power conversion [13]. The circuit shown in Fig. 2 operates under ZVS by using parasitic components. To get ZVS, the primary bridge inverter legs are operated with a phase shift. This operation discharges the MOSFET parasitic capacitance and later on forces the conduction of the MOSFET body diode. Fig. 3 demonstrates the primary current and voltage waveforms of ZVS PS FB PWM converter.

The energy stored in leakage inductor at time t_2 is used for discharging the output capacitor of switch Q_4 and charging the output capacitor of switch Q_2, and has to satisfy (1):

$$E = \frac{1}{2} L_{lk} I_2^2 > \frac{4}{3} C_{MOS} V_{in}^2 + \frac{1}{2} C_{TR} V_{in}^2 \qquad (1)$$

where I_2 is the current flowing at time t_2 (or t_6) in Fig. 3, C_{MOS} is the effective output capacitance of the MOSFET and C_{TR} is the winding capacitance of the transformer. To turn on switch Q_4 with zero voltage, a dead time is needed between the turn off of switch Q_2 and turn on of switch Q_4, such that switch Q_4 diode conducts before to turn on switch Q_4. The resonance between the leakage inductance of primary winding of transformer L_{lk} and the equivalent output capacitances of switches (C_{MOS2} + C_{MOS4}) and transformer winding capacitance C_{TR} produces sinusoidal voltage across switches Q_2 and Q_4 that reaches to maximum value at one fourth of the resonant period. The dead time between switches in the lagging leg can be calculated at one fourth of the resonant period as given in (2) [13]:

$$t_{d24} = \frac{\pi}{2} \sqrt{L_{lk} C_{eq}} \qquad (2)$$

where C_{eq} = C_{MOS2} + C_{MOS4} + C_{TR}.

The rising voltages across switch Q_4 at time t_2 for three different load currents are shown in Fig. 4. The first waveform in Fig. 4 (a) shows the case when the energy stored in L_{lk} is greater than the energy required to charge or discharge the output capacitors. Switch Q_4 output capacitor is charged in

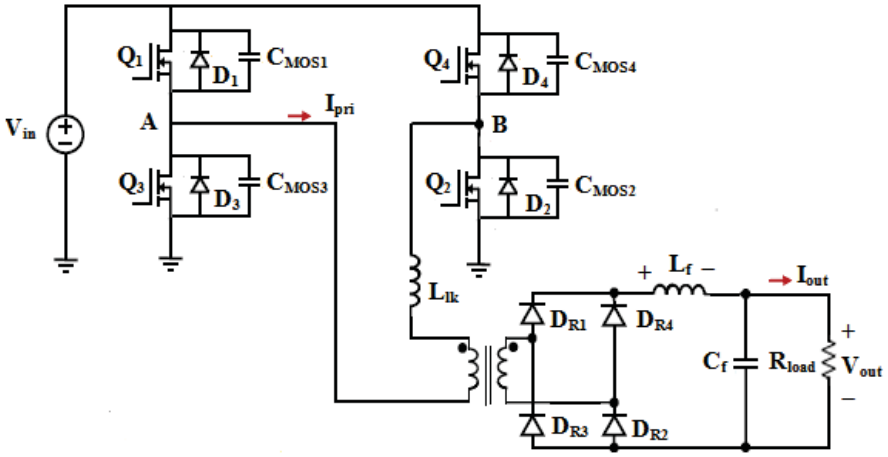

Fig. 2 ZVS PWM FB converter using leakage inductance

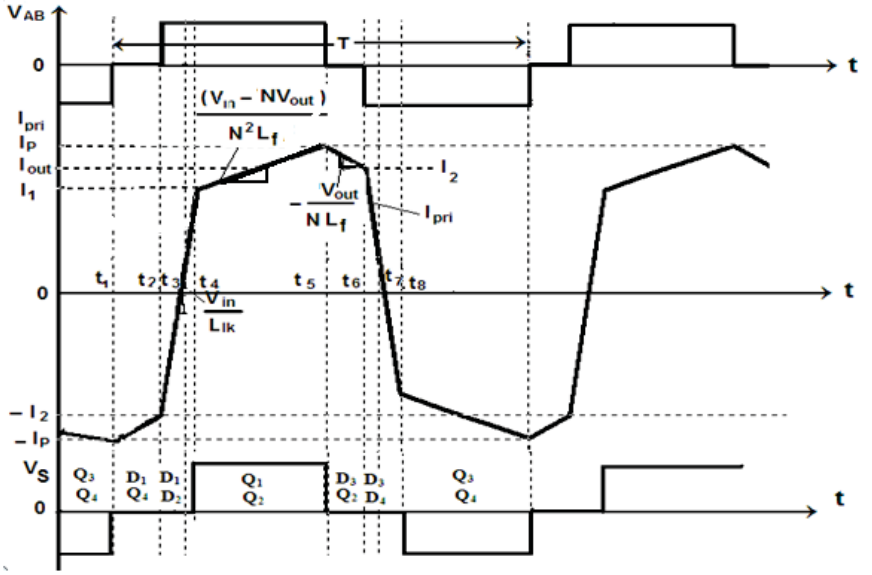

Fig. 3 ZVS PS FB PWM converter key waveforms

less than t_{d24}. Thus, the voltage across switch Q_4 is clamped to V_{in}. Fig. 4 (b) shows the case when the energy in the L_{lk} is equal to the energy needed to charge or discharge output capacitors of switches. The last voltage waveform in Fig. 4c shows the condition when the energy in L_{lk} is less than the energy needed to charge or discharge the parasitic output capacitors and hence ZVS is lost. After t_{d24}, switch Q_4 or Q_2 is on and the primary voltage sharply clamped to V_{in}.

At low load currents, the energy stored in L_{lk} at time t_2 or t_6 is not sufficient to turn on switch diode D_2 or D_4 of the lagging leg [13], [23]. In leading leg, switch Q_1 at time t_5 is turned off and the energy needed to charge Q_1 output capacitance and discharge Q_3 output capacitance is the energy in (L_{lk} + L_f) [13]. The dead time t_{d13} needed between switches Q_1 and Q_3 may be calculated from (3).

$$4C_{MOS}V_{in} + C_{TR}V_{in} = I_P t_{d13} \quad (3)$$

The term $4C_{MOS}V_{in}$ in (3) is the charged stored on two nonlinear output capacitors of MOSFETs. The charge stored on one non linear output capacitor of MOSFET is $2C_{MOS}V_{in}$. The phase shift between switches Q_1 and Q_2 is determined from Fig. 3 and may be written as (4):

$$\phi_{12} = (1 - D - \frac{2t_{d13}}{T})180^\circ \quad (4)$$

1) Requirement of ZVS for Leading and Lagging Legs: Switches Q_1 and Q_3 can easily achieve ZVS even at low load currents because the reflected output filter inductor current always turn on body diodes D_1 and D_3 [13]. ZVS for switches Q_2 and Q_4 can be achieved at a primary current greater than the critical current I_{cri}. The critical current in primary at time

t_2 (or t_6), required for ZVS of switches Q_2 and Q_4 is obtained from (1) and may be written as (5):

$$I_{cri} = \sqrt{\frac{2}{L_{lk}}(\frac{4}{3}C_{MOS}V_{in}^2) + \frac{1}{2}C_{TR}V_{in}^2} \quad (5)$$

The current in the primary at time t_2 may be determined from Fig. 3 and is given by (6):

$$I_2 = \frac{N_s}{N_p}(I_{out} + \frac{\Delta I}{2} - \frac{V_{out}}{L_f}(1-D)\frac{1}{2f_s}) \quad (6)$$

where D is the converter primary duty cycle, L_f is the output inductance, V_{out} is the average output voltage of the converter, f_s is switching frequency, I_{out} is converter average output current, ΔI is the peak-peak output inductor current ripple, and N_p and N_s are the primary and secondary turns, respectively.

ZVS for lagging leg at time t_2 (or t_6) is achieved when the primary current is greater than the primary critical current. The relation for ZVS at time t_2 (or t_6) is given by (7). ZVS for switch Q_2 and switch Q_4 at t_2 (or t_6) has to satisfy (7) and (8):

$$I_2 > I_{cri} \quad (7)$$

$$\frac{N_s}{N_p}(I_{out} + \frac{\Delta I}{2} - \frac{V_{out}}{L_f}(1-D)\frac{1}{2f_s}) > I_{cri} \quad (8)$$

The voltage conversion ratio of ZVS PS PWM converter may be written as given in (9):

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p}D_{eff} \quad (9)$$

where D_{eff} is the secondary voltage duty cycle.

D is set by the gate signals of the primary switches and expressed as (10):

$$D = D_{eff} + \Delta D \quad (10)$$

In (10), ΔD is the duty cycle loss produced by L_{lk}.

From Fig. 3, the steady state equation for duty cycle loss ΔD is given by (11):

$$\Delta D = \frac{2L_{lk}f_s(I_1 + I_2)}{V_{in}} \quad (11)$$

$$\Delta D = \frac{2L_{lk}f_s(\frac{2I_{out}}{N})}{V_{in}} \quad (12)$$

Using (1) and (12) duty cycle may be written as (13):

$$\Delta D = \frac{32C_{MOS}f_sV_{in}I_{out}}{3I_{cri}^2} \quad (13)$$

In Fig. 3, I_1 is the primary current at time t_4 and may be written as (14):

$$I_1 = \frac{N_s}{N_p}(I_{out} - \frac{\Delta I}{2}) \quad (14)$$

The substitution of (6) and (14) into (11) leads to the (15) for duty cycle loss:

$$\Delta D = \frac{\frac{N_s}{N_p}}{\frac{V_{in}}{L_{lk}}\frac{T}{2}}(2I_{out} - \frac{V_{out}}{L_f}(1-D)\frac{T}{2}) \quad (15)$$

The substitution of (15) into (10) leads to (16):

$$D = \frac{1 + 4\frac{L_{lk}f_s}{R'_{load}} - \frac{L_{lk}}{L'_f}}{\frac{1}{D_{eff}} - \frac{L_{lk}}{L'_f}} \quad (16)$$

where $R'_{load} = (\frac{N_p}{N_s})^2R_{load}$ and $L'_f = (\frac{N_p}{N_s})^2L_f$. When the term $\frac{V_{out}}{L_f}(1-D)\frac{T}{2}$ is much smaller as compared to $2I_{out}$ in (15), then (15) may be simplified to (17):

$$\Delta D = \frac{\frac{N_s}{N_p}}{\frac{V_{in}}{L_{lk}}\frac{T}{2}} \quad (17)$$

2) Conduction Losses: The conduction losses of the primary switches and body diodes may be determined from Fig. 5 as (18)-(21):

$$P_{Q2,4} = R_{on}[A + B + C] \quad (18)$$

where $A = (\frac{I_1}{\sqrt{3}})^2\frac{\Delta D}{4}$, $B = \frac{\Delta I_1^2}{12})\frac{D_{eff}}{2}$ and $C = (I_{cav}^2 + \frac{\Delta I_2^2}{12})\frac{D'}{2}$

$$P_{Q1,3} = R_{on}[(\frac{I_1}{\sqrt{3}})^2\frac{\Delta D}{4} + (I_{out}^2 + \frac{\Delta I_1^2}{12})\frac{D_{eff}}{2}] \quad (19)$$

$$P_{D2,4} = (\frac{I_2}{2})V_{diode}\frac{\Delta D}{4} \quad (20)$$

$$P_{D1,3} = V_{diode}(\frac{D'}{2}I_{out} + \frac{1}{2}\frac{\Delta D}{4}I_2) \quad (21)$$

where the first and second term used in the brackets of (18) and (19) are the rms currents during intervals (t_3 - t_4) and (t_4 - t_5) in Fig. 3, respectively. The third term in the bracket of (18) is the rms current during interval (t_1 - t_2) or (t_5 - t_6). There is no conduction loss during state (t_1 - t_2) or (t_5 - t_6) for switches Q_1 and Q_3, respectively. During the operation of converter, a high circulating current flows during the intervals (t_1 - t_2) and (t_5 - t_6) shown in Fig. 3. In these intervals, two upper or lower switches in the primary bridge are on at the same time in one cycle and clamp the transformer primary voltage to zero and increases conduction losses. All secondary diodes are on during these intervals and no power is delivered to load. For wider ZVS range of lagging leg, primary leakage inductance is increased or large linear resonant external inductor is used in series with L_{lk} [21]. The minimum energy stored in the linear resonant inductor at critical current is given by (22):

$$E_{min} = \frac{1}{2}L_{ro}I_{cri}^2 \quad (22)$$

The stored energy in the large linear resonant inductor at maximum output current is much more than is required for ZVS of the primary bridge switches as shown in Fig. 6. During intervals (t_2 - t_4) and (t_6 - t_8) in Fig. 3 energy is returned to the source known as circulating energy and is given in (23):

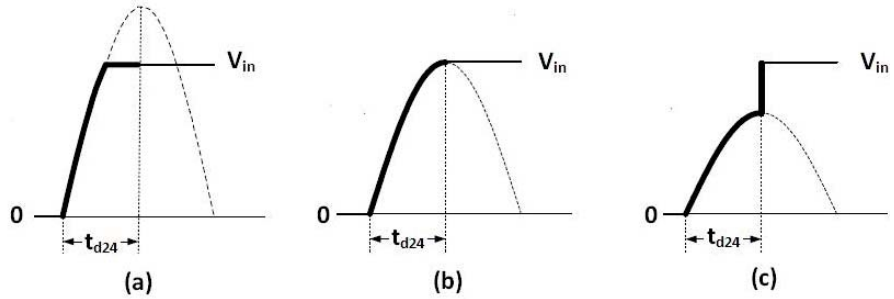

Fig. 4 Rising voltage across the switch Q_4 at turn off

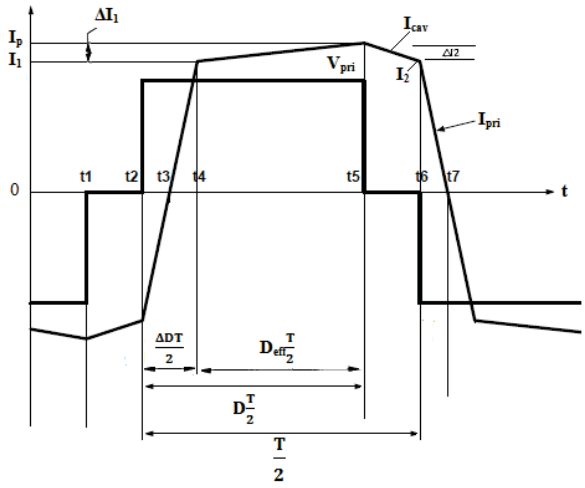

Fig. 5 ZVS PWM converter key waveforms showing output inductor current ripple

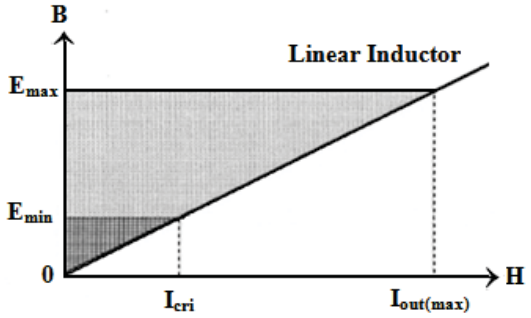

Fig. 6 Circulating energy stored in linear inductor

$$E_{cir} = E_{max} = E_{min}(\frac{I_{out(max)}}{I_{cri}})^2 \quad (23)$$

This circulating energy is very high and helps in achieving ZVS, though it also increases switch conduction losses and duty cycle loss. The maximum energy stored in the linear resonant inductor at maximum output current is given by (24).

$$E_{max} = \frac{1}{2}L_{ro}I^2_{out(max)} \quad (24)$$

B. ZVS PS PWM FB Converter Using Saturable Inductor

The large linear resonant inductor in the primary over a broad ZVS range produces high duty cycle loss, high switch conduction losses, high current and voltage stresses [18]. The converter output voltage with large linear resonant inductor may be written as (25):

$$V_{out} = \frac{DV_{in}}{N} - \frac{4L_{ro}f_sI_{out}}{N^2} \quad (25)$$

It is observed from (25) that the converter output voltage depends on the output current. V_{out} is more sensitive to variation in the output current for a given primary duty cycle and resonant inductor. A large resonant inductor causes low output voltage. To achieve the required output voltage, smaller turns ratio is needed. Conversely a smaller turns ratio increases the primary current stress, $\frac{I_{out}}{N}$, which increases the rectifier diode voltage stress, $\frac{V_{in}}{N}$, and primary conduction losses. These major limitations in the ZVS PS PWM converters mentioned above can be removed by using saturable inductor in place of resonant inductor as shown in Fig. 7.

The stored energy in saturable inductor is unchanged if the primary current increases above I_{cri} as shown in Fig. 9. The minimum stored energy in saturable inductor must fulfill (22). At t_2 (or t_6), the saturable inductor is saturated and the inductor current reaches to critical saturation current . Then the primary current, I_{pri} reaches rapidly to $\frac{I_{out}}{N}$, the converter voltage in the secondary reaches to $\frac{V_{in}}{N}$, and in half period, $\frac{\Delta DT}{2}$is reduced by $\frac{\Delta D_eT}{2}$ as shown in Fig. 8. Switch Q_1 at time t_4 is turned off and the current drops rapidly to critical saturation current I_{cri}. During intervals (t_0 - t_1) and (t_4 - t_5) in Fig. 8 the current stresses of primary switches are decreased. Fig. 8 also shows that when primary current exceeds I_{cri} then the duty cycle loss depends upon the critical current which may be written as (26):

$$\Delta D = \frac{32}{3}\frac{C_{MOS}f_sV_{in}}{NI_{cri}} \quad (26)$$

The converter output voltage using saturable inductor may be written as (27) or (28):

$$V_{out} = \frac{DV_{in}}{N} - \frac{4L_{ro}f_sI_{out}}{N^2} \quad (27)$$

when $\frac{I_{out}}{N} < I_{cri}$

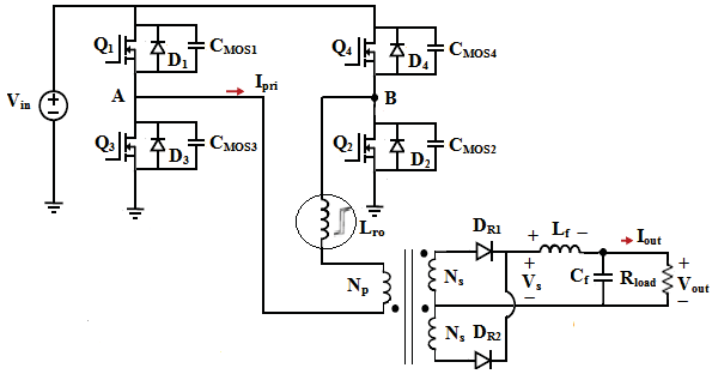

Fig. 7 ZVS PWM FB converter circuit using saturable inductor

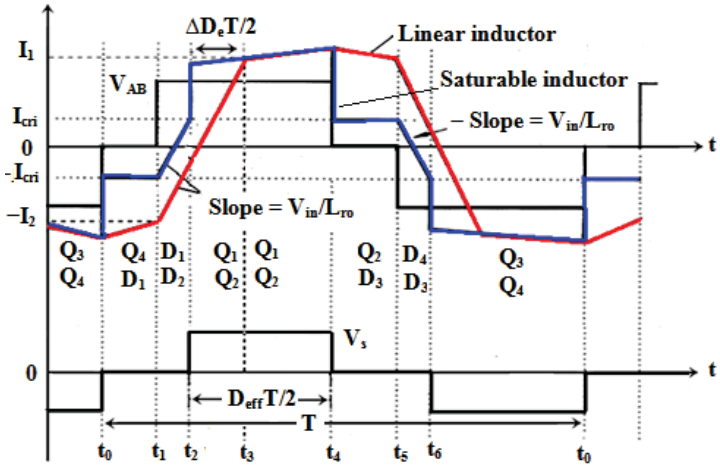

Fig. 8 Key waveforms of ZVS PS converter using saturable inductor

$$V_{out} = \frac{DV_{in}}{N} - \frac{4L_{ro}f_sI_{cri}}{N^2} \tag{28}$$

when $\frac{I_{out}}{N} > I_{cri}$

It is seen from (28), that the converter output voltage using saturable inductor become independent of the load current when the reflected output current referred to primary is greater than critical current. The circulating energy is greatly reduced by saturable inductor as shown in Fig. 10 which, in turn, reduces duty cycle loss and conduction losses of switches. When saturable inductor is used for ZVS in the converter, the circulating energy is equal to the minimum energy required for ZVS and is given by (29):

$$E_{cir} = E_{min} \tag{29}$$

1) Conduction Losses: From Fig. 8, the primary bridge switches and body diodes conduction losses are obtained and may be written as (30)-(33):

$$P_{Q2,4} = R_{on}[C + D + E] \tag{30}$$

where $C = (\frac{I_1}{\sqrt{3}})^2 \frac{\Delta D}{2}$, $D = (I_{out}^2 + \frac{\Delta I_1^2}{12}) \frac{D_{eff}}{2}$

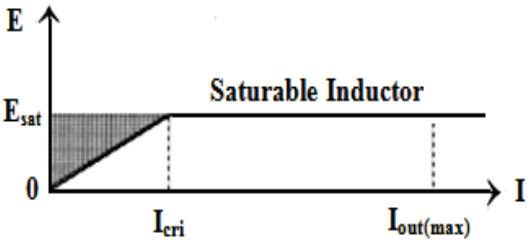

Fig. 9 Inductor energy versus current

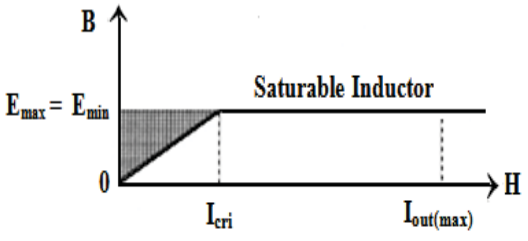

Fig. 10 Saturable inductor energy after saturation

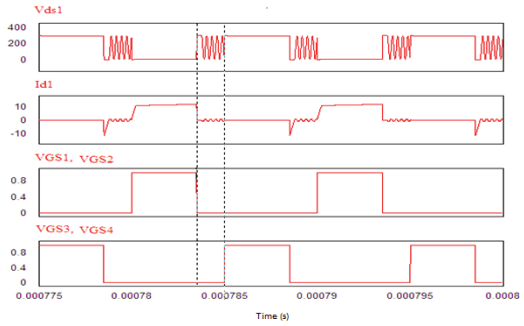

Fig. 11 Switch current and voltage waveforms when all gate signals are low

$and\ E = \frac{I_{cri}^2 D^{'}}{2}$

$$P_{Q1,3} = R_{on}[(\frac{I_{cri}}{\sqrt{3}})^2 \frac{\Delta D}{2} + (I_{out}^2 + \frac{\Delta I_1^2}{12})\frac{D_{eff}}{2}] \quad (31)$$

$$P_{D1,3} = V_{diode}(\frac{D^{'}}{2} I_{cri} + \frac{\Delta D}{8} I_{cri}) \quad (32)$$

$$P_{D2,4} = V_{diode}(I_{cir} \frac{\Delta D}{8}) \quad (33)$$

where the first and second term used in the brackets of (30) and (31) are the rms currents during states (t_3 - t_4) and (t_4 - t_5), respectively. The third term in the bracket of (30) is the rms current during state (t_1 - t_2) or (t_5 - t_6) and depends upon the critical current not upon the output current.

C. Zero PS ZVS PWM FB Converter Using Leakage Inductance

In zero PS converter, there is no phase shift between the diagonal switches in Fig. 2. The gate signals, switch current and voltage waveforms of zero PS ZVS converter are shown in Fig. 11, with D = 0.7 and f_s = 100 KHz. When this converter operates on small primary duty cycle and all the MOSFETs are turned off, then the stored energy in L_{lk} causes ringing with output capacitances of MOSFETs. This will increases the conduction losses of the switches. This is a big disadvantage of this converter.

IV. Design of Converters

The discussed three ZVS FB PWM converters are designed for the following given specifications: Input voltage, V_{in} = 300 V, output voltage, V_{out} = 180 V, switching frequency, f_s = 100 kHz, output power, P_{out} = 2 kW and output inductor current ripple, ΔI= 10% of I_{out}. To make the discussion more easy, the ZVS PS PWM converter with leakage inductance will be consider as approach A, the converter with saturable inductor is consider as approach B and Zero PS converter with leakage inductance will be referred to as approach C. Based on the given specifications, power components in the primary bridge are $IRFP460$ and $BYV54V200$ for the secondary rectifier were selected. The output filter inductance was measured about 324 μH and the output capacitor about 1.54 μF.

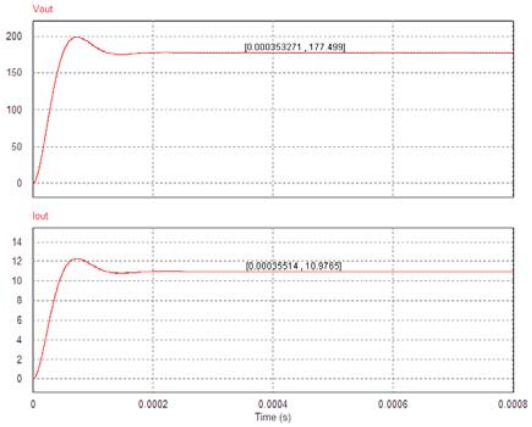

Fig. 12 Output voltage at full load current for approach A

In approach A, a leakage/resonant inductance with a value of 13.5 μH is selected with a duty cycle of 0.8 and secondary effective is 0.6 to achieve ZVS from 20.34% of load to full load. The phase shift between switch Q_1 and Q_2 is 35.46°.

In approach B, the linear external inductor is replaced with saturable inductor with a value of 13.5 μH for the same ZVS range as given in approach A. To get the required output voltage, the primary duty cycle is 0.64 and secondary effective duty cycle is 0.6. The phase shift between switch Q_1 and Q_2 is 63.54°.

In approach C, the leakage/resonant inductance with a value of 23.62 μH is selected to achieve ZVS from 21.78% of load to full load. To get the required output voltage, the primary duty cycle is 0.9 and secondary effective duty cycle is 0.6. The phase shift between the switch Q_1 and Q_2 is zero.

V. Simulation Results and Comparison of Converters

All the discussed three converters are simulated in PSIM software. After the successful simulations in PSIM, the generated waveforms of output voltages and currents waveforms, primary, secondary voltages and currents waveforms, and switch voltages and currents waveforms have been shown in Figs. 12-20. The purpose of these waveforms shows duty cycle loss, circulating current stresses and switching loss. From the simulation results, it is clear that the desired output voltage and current is achieved for each converter. These results also show that converter with saturable inductor produces low duty cycle loss and operated the converter with less conduction losses, while the other two converters with leakage inductances produces higher duty cycle loss which increases the conduction losses. ZVS is achieved for switch Q_2 using approach A, B and C as shown in Figs. 14, 17 and 20.

The ZVS range, dead times of the switches, duty cycle loss, circulating energy, circulating current stresses, conduction losses of primary bridge switches, body diodes and rectifier diodes are the main parameters for each ZVS PWM FB converter. The comparison of the converters in this paper are based on the same primary bridge switches, rectifier circuits,

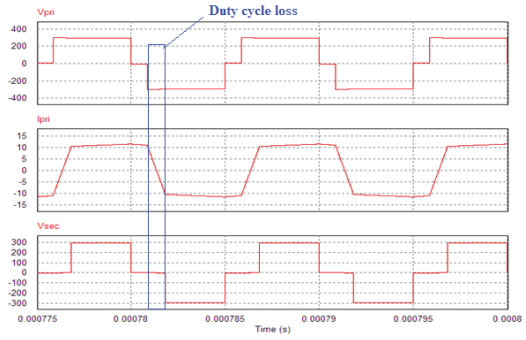

Fig. 13 Primary voltage, current and secondary voltage for approach A

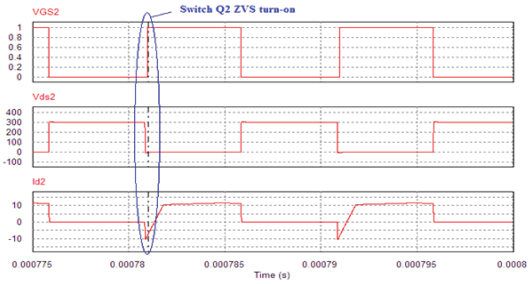

Fig. 14 Switch Q_2, gate voltage, drain to source voltage and current at full load for approach A

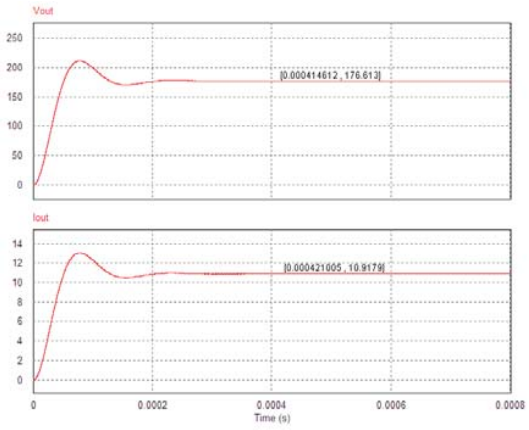

Fig. 15 Output voltage at full load current for approach B

frequency, filter inductances and capacitances, transformer and transformer turns ratio. A detail comparison of the parameters of the discussed and simulated converters is given in Table I.

Table I shows that ZVS PS PWM FB converter using leakage inductor and ZVS PS PWM FB converter using saturable inductor have the same ZVS range, which is 20.34% of full load current for the same value of inductance. To obtain ZVS in zero PS ZVS converter which is 21.78% of full load current the L_{lk} is increased which increases the circulating energy. The circulating energy of the converter with saturable inductor is $34.48\ \mu J$, which is lower than that of $821.65\ \mu J$ of ZVS PS PWM converter and $1456.80\ \mu J$ of zero PS ZVS converter. The saturable inductor after saturation does not store much more circulating energy.

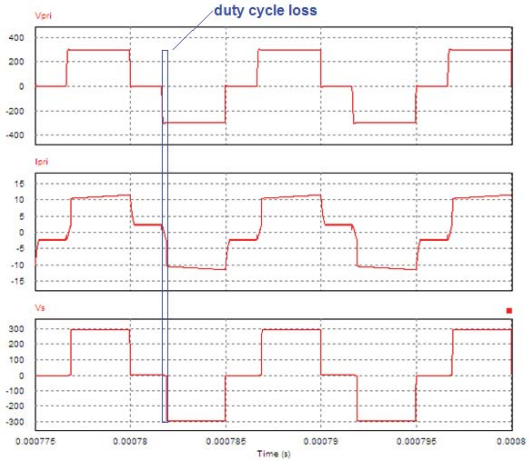

Fig. 16 Primary voltage, current and secondary voltage for approach B

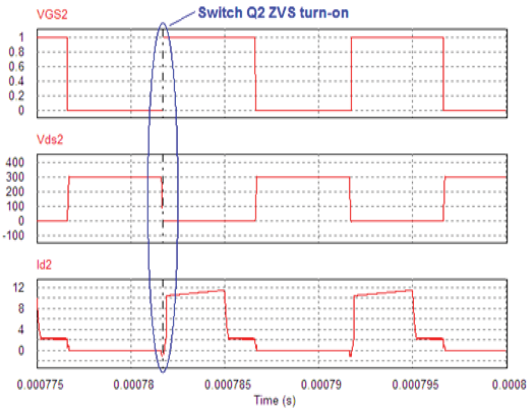

Fig. 17 Switch Q_2, gate voltage, drain to source voltage and current at full load for approach B

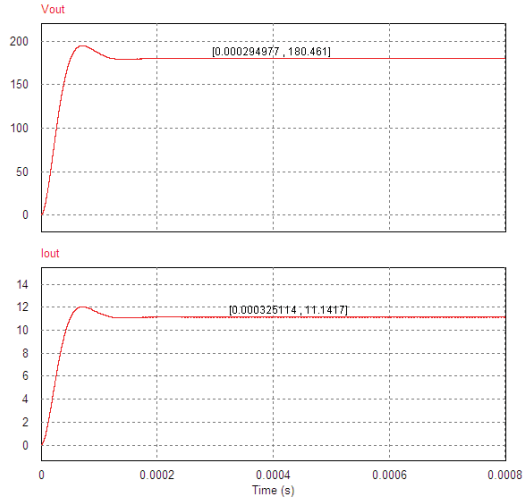

Fig. 18 Output voltage at full load current for approach C

The converter duty cycle loss increases with high circulating energy. The duty cycle loss of the converter with saturable inductor is 0.04, which is much smaller than that of 0.2 and

TABLE I
COMPARISONS OF CONVERTERS PARAMETERS AT 100 KHz FREQUENCY

Parameters	ZVS PS Converter with Leakage Inductance	ZVS PS Converter with Saturable Inductance	Zero PS ZVS Converter with Leakage Inductance
Dead time, t_{d13}	0.03 μs	0.03 μs	0.25 μs
Dead time, t_{d24}	0.14 μs	0.14 μs	0.25 μs
ZVS range	20.34% of full Load current	20.34% of full Load current	21.78% of full Load current
Duty cycle loss, ΔD	0.2	0.04	0.35
Efficiency	94.11%	9.60%	94.31%
Circulating energy, E_{cir}	821.65 μJ	34.48 μJ	1456.80 μJ
Circulating current stress	11.66 A	2.26 A	N/A
Conduction losses	72.42 W	61.67 W	78.25 W

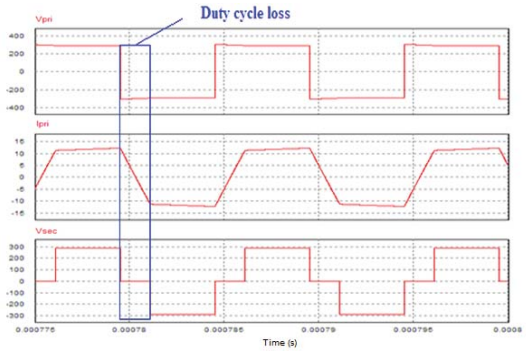

Fig. 19 Primary voltage, current and secondary voltage for approach C

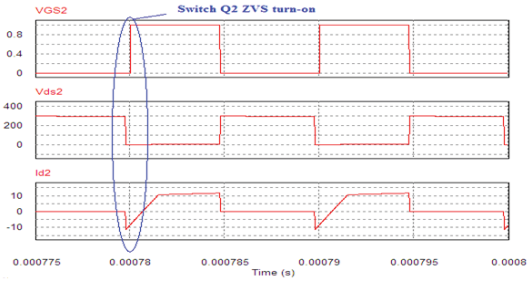

Fig. 20 Switch Q_2, gate voltage, drain to source voltage and current at full load for approach C

0.35 of ZVS PS PWM and zero PS ZVS PWM converters using leakage inductances, respectively. There is no circulating current stress on primary bridge switches in zero PS ZVS PWM converter. The circulating current stress in ZVS PS PWM FB converter using leakage inductance is 11.66 A, which is greater than that of 2.26 A of ZVS PS PWM FB converter using saturable inductor.

The conduction losses with saturable inductor at full load are smaller as compared to other two converters because the conduction losses of primary bridge switch and its body diodes of the converter with saturable inductor depends upon only on critical current not upon the output current. The efficiency of the circuit with saturable inductor is 94.60%, which is higher than that of 94.11% of ZVS PS circuit with leakage inductance and 94.31% of zero PS circuit with leakage inductance.

VI. CONCLUSIONS AND FUTURE WORK

Three isolated 2 kW ZVS PWM FB converters have been studied for battery charger applications of EV. The PS PWM and zero PS PWM converters with leakage inductances are not suitable for battery charger applications of EV with wider ZVS range. These converters have higher circulating energy, duty cycle loss, and lower efficiency. However, the converter employing saturable inductor with wider ZVS rang has lower circulating energy, duty cycle loss, conduction losses, and high efficiency. Because of these characteristics, the ZVS PS PWM FB converter with saturable inductor is preferable for the battery charger applications of EV.

In future work, we will perform AC analysis of the converters to get more accurate results. Since ZVS of the converters is required from no load to full load in order to reduce switching losses, it also needs to be analyzed in future.

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REFERENCES

[1] G. Y. Choe, J. S. Kim, B. K. Lee, C.-Y. Won, and T.-W. Lee, "A bi-directional battery charger for electric vehicles using photovoltaic pcs systems," in *2010 IEEE Vehicle Power and Propulsion Conference*, Sept 2010, pp. 1–6.

[2] C. C. Chan and K. T. Chau, "An overview of power electronics in electric vehicles," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 1, pp. 3–13, Feb 1997.

[3] I. A. Khan, "Battery chargers for electric and hybrid vehicles," in *Power Electronics in Transportation, 1994. [Proceedings]*, Oct 1994, pp. 103–112.

[4] K. Jin, X. Ruan, M. Yang, and M. Xu, "A hybrid fuel cell power system," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 4, pp. 1212–1222, April 2009.

[5] H. Aksoy and M. T. Aydemir, "Comparison of zero voltage switching phase-shifted PWM full bridge dc-dc converter topologies," in *2015 Intl Aegean Conference on Electrical Machines Power Electronics (ACEMP)*, Sept 2015, pp. 818–824.

[6] M. K. Yang, H. S. Cho, S. J. Lee, and W. Y. Choi, "High-efficiency pulse-width modulated full-bridge converter for low-voltage battery charging applications," in *Transportation Electrification Conference and Expo (ITEC), 2014 IEEE*, June 2014, pp. 1–6.

[7] X. Ruan and L. Zhang, "Voltage oscillation elimination in output rectifier diodes in zero-voltage-switching PWM full-bridge converter: An overview," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 6328–6335.

[8] M. K. Yang, H. S. Cho, S. J. Lee, and W. Y. Choi, "High-efficiency low-cost soft-swtiching DC-DC converter for ev on-board battery chargers," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 2050–2055.

[9] I. O. Lee and G. W. Moon, "Phase-shifted PWM converter with a wide zvs range and reduced circulating current," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 908–919, Feb 2013.

[10] J. C. Maragao-Schmidt and J. Renes-Pinheiro, "Comparative study of full-bridge and double half-bridge converters," in *2015 CHILEAN Conference on Electrical, Electronics Engineering, Information and Communication Technologies (CHILECON)*, Oct 2015, pp. 453–460.

[11] A. J. B. Bottion and I. Barbi, "Full bridge zero-voltage-switching PWM DC-DC converter with output capacitive filter," in *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, Nov 2015, pp. 1–6.

[12] A. Ali, R. Ullah, and Z. Ullah, "DC-to-DC converters for low-voltage high-power renewable energy systems," *World Academy of Science, Engineering and Technology, International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, vol. 9, no. 12, pp. 1299–1304, 2015.

[13] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990., Fifth Annual*, March 1990, pp. 275–284.

[14] X. Ruan, J. Wang, and Q. Chen, "Am improved current-doubler-rectifier ZVS PWM full-bridge converter," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 4, 2001, pp. 1749–1754 vol. 4.

[15] Y. Jang, M. M. Jovanovic, and Y.-M. Chang, "A new ZVS-PWM full-bridge converter," in *Telecommunications Energy Conference, 2002. INTELEC. 24th Annual International*, 2002, pp. 232–239.

[16] C. Liu, B. Gu, J. S. Lai, M. Wang, Y. Ji, G. Cai, Z. Zhao, C. L. Chen, C. Zheng, and P. Sun, "High-efficiency hybrid full-bridge-half-bridge converter with shared ZVS lagging leg and dual outputs in series," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 849–861, Feb 2013.

[17] Y. Jang and M. M. Jovanovic, "A new family of full-bridge ZVS converters," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 2, Feb 2003, pp. 622–628 vol.2.

[18] G. Hua, F. C. Lee, and M. M. Jovanovic, "An improved full-bridge zero-voltage-switched PWM converter using a saturable inductor," *IEEE Transactions on Power Electronics*, vol. 8, no. 4, pp. 530–534, Oct 1993.

[19] R. Redl, N. O. Sokal, and L. Balogh, "A novel soft-switching full-bridge DC/DC converter: Analysis, design considerations, and experimental results at 1.5 kw, 100 khz," in *Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE*, 1990, pp. 162–172.

[20] R. Redl, L. Balogh, and D. W. Edwards, "Switch transitions in the soft-switching full-bridge PWM phase-shift DC/DC converter: analysis and improvements," in *Telecommunications Energy Conference, INTELEC '93. 15th International*, vol. 1, Sep 1993, pp. 350–357 vol.1.

[21] X. Ruan and F. Liu, "An improved ZVS PWM full-bridge converter with clamping diodes," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 2, June 2004, pp. 1476–1481 Vol.2.

[22] W. Chen, X. Ruan, Q. Chen, and J. Ge, "A novel clamping diode current reset scheme for ZVS PWM full-bridge converter," in *2010 IEEE Energy Conversion Congress and Exposition*, Sept 2010, pp. 1932–1937.

[23] T. Mishima, K. Akamatsu, and M. Nakaoka, "A high frequency-link secondary-side phase-shifted full-range soft-switching PWM DC-DC converter with ZCS active rectifier for ev battery chargers," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5758–5773, Dec 2013.