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High-Efficiency Comparator for Low-Power Application

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***Abstract*—**In this paper, dynamic comparator structure employing two methods for power consumption reduction with applications in low-power high-speed analog-to-digital converters have been presented. The proposed comparator has low consumption thanks to power reduction methods. They have the ability for offset adjustment. The comparator consumes 14.3 μW at 100 MHz which is equal to 11.8 fJ. The comparator has been designed and simulated in 180 nm CMOS. Layouts occupy 210 μm^2.

***Keywords*—**Comparator, low, power, efficiency.

I. Introduction

GLOBAL demand in design of the electronic systems is toward manufacturing systems which have high speed and accuracy, with low area and power consumption. In modern electronic systems such as mobile communications and data processing units, analog to digital conversion is one of the most important blocks of the digital system [1]-[4]. Speed, accuracy and power consumption of comparator has critical role at overall and proper performance of the ADC. Power consumption, input referred offset and evaluation time are important specifications of the comparators. Generally, comparators are divided into two major classes: dynamic and static comparators [5]. Because of their higher speed and lower power consumption, dynamic comparators are widely used in the design of high speed ADCs. The input offset problem due to static mismatch between threshold voltages, the value of μnCox and mismatch between parasitic capacitances of the internal nodes, is an important challenge in design of comparators in modern technologies with small feature sizes. On the other hand, using offset reduction methods increases power consumption. Decreasing input-referred offset without increasing power consumption is a great challenge in design of comparators [6]-[8].

Lewis Gray structure is widely used in ADC design [9]. It has a preamplifier stage and a cross-coupled latch pair. In this structure, power consumption is increased to achieve high speed and low input offset. In dynamic comparator shown in Fig. 1, input offset can be adjusted by the delay generated in clock pulse driving the latch stage [10].

Section II describes the structure and the basic operation of the comparator. In Section III, power reduction technique is discussed to improve energy consumption of the proposed comparator. Simulation results of the proposed comparator are summarized in Section IV.

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II. Structure and Basic Operation of the Comparator

Fig. 1 shows the structure of the comparator which is composed of two stages [10]. These are the decision stage and hold stage. Comparator operation has three different phases. Phase 1 is reset, phase 2 is decision or evaluation and third phase is hold phase which stores the evaluation result for a specific time interval. In reset phase when clk1 is high, transistors M9 and M10 are off while M7 and M8 are on. As a result, nodes Vi-n and Vi-p are shorted to ground through M7 and M8. When clk1 is low, decision (evaluation) phase is started. In this phase, input signals Vi-n and Vi-p increase the node voltages Vo-n and Vo-p. Considering the signal levels of Vip - Vref+ and Vin – Vref-, output voltages Vout+ and Vout- will have different speeds. Of two voltages, one that approaches the threshold voltage of the NMOS transistor earlier connects to Vdd through two cross-coupled inverters and other node will be connected to ground. As a result, one of the Vo-p and Vo-n are connected to Vdd or Gnd. After this phase (evaluation time), input signal fluctuations cannot change the output state unless output nodes are reset for the next comparison. In this structure, input offset can be managed by the timing of the clock pulse clk2. In this structure, power is dissipated in hold phase while CMOS inverters do not need power consumption at this phase. First stage has power dissipation while with modifying the structure, power consumption in hold phase can be reduced. With this assumption that after evaluation phase, output node Vo-p equals to Vdd, a current will be drawn from Vr-p. The current path is shown in Fig. 3. In this path, transistors M1, M4 and M9 are on. While in hold phase there is no need for this current. With this description about the operation of the comparator, two methods are proposed to alleviate this problem.

III. Power Reduction Method

The structure of the proposed comparator is shown in Fig. 4. This is based on using another clock pulse for triggering M9 and M10 transistors. It goes low at the same time with clk1 but after the state of the latch is determined it goes to high, again. In this condition, M9 and M10 are off and no current drawn from Vr-n and Vr-p and no power is dissipated in evaluation phase. Power is dissipated when clk3 is low, and in reset and evaluation no power is dissipated. Overall power consumption is decreased and energy efficiency can be improved. The important point in the proposed comparator is the length of

time that it is in low state. It must be long enough for comparator to finish its decision.

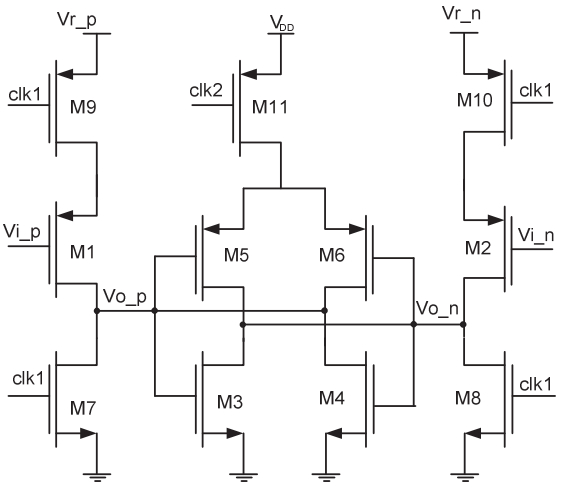

Fig. 1 The structure of the basic dynamic comparator

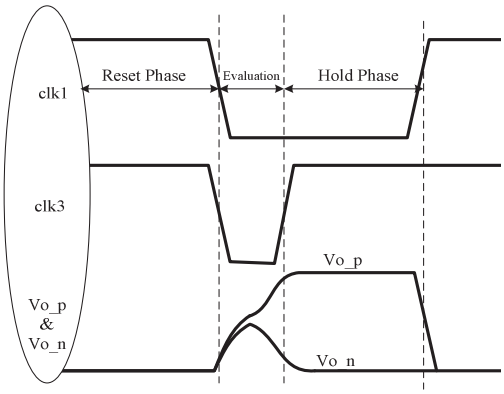

Fig. 2 Time diagrams of clock pulses of the dynamic comparator

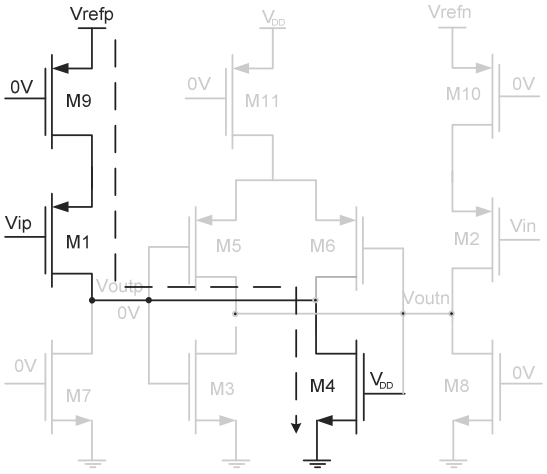

Fig. 3 Power consumption path in comparator when evaluation is finished (Vin>Vip)

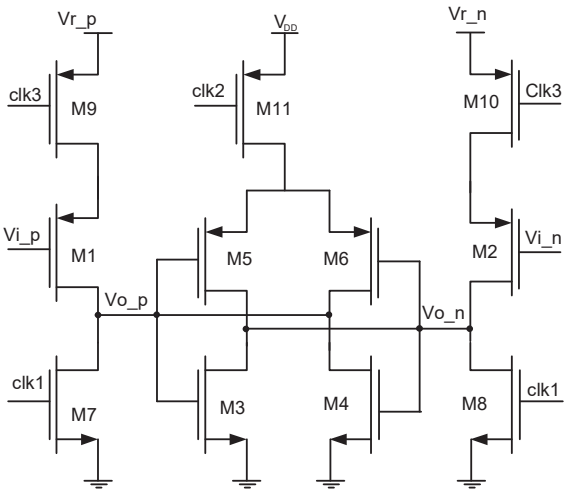

Fig. 4 The circuitry of the proposed comparator using technique

IV. Simulation Results

The proposed comparator has been designed and simulated in 180 nm CMOS process. Table I summarizes the size of the devices.

Considering the input offset analysis of the comparator in previous sections and the monte-carlo (1000 points) simulation results which is shown in Fig. 5, input offset resulting from manual calculation is 1.9 mV.

TABLE I
The Size of the Devices of the Proposed Comparator

Size	W/L
M1,M2	5μm/180nm
M3,M4	220nm/180nm
M5,M6	1μm/180nm
M7,M8	7μm/180nm
M9,M10	1μm/180nm

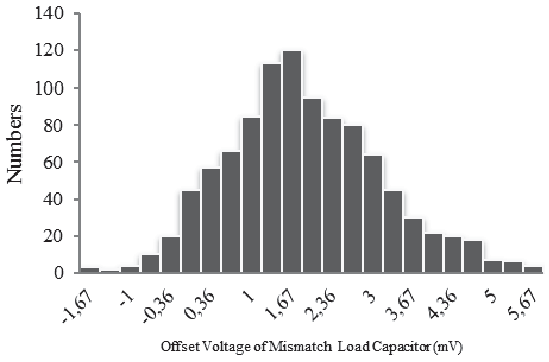

Fig. 5 Histogram of the input offset voltage versus capacitance mismatch for comparator

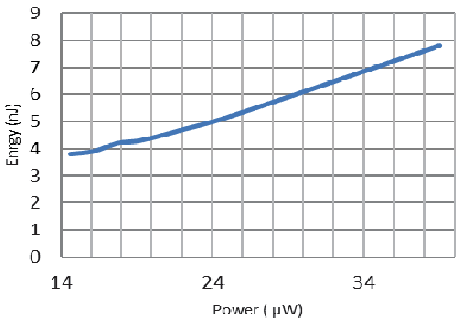

Fig. 6 Energy efficiency of the proposed comparators versus dissipated power

In Fig. 6, energy consumption of proposed techniques is shown. The improvement achieved by first techniques is better than the second one. In Fig. 7, the effect of clk3 pulse width on power consumption and energy efficiency has been shown. Fig. 8 shows the layout of two proposed comparators. Comparator 1 occupies 210 µm^2 same as the basic comparator.

TABLE II
COMPARISON OF POWER AND ENERGY OF DIFFERENT COMPARATORS

REFERENCE	POWER(µW)	DELAY(PS)	TECH.(NM)	ENERGY(FJ)
[11]	82	130	180	10.7
[10]	51	152	90	7.8
[8]	116	170	180	19.7
THIS WORK	14.3	258	180	3.7

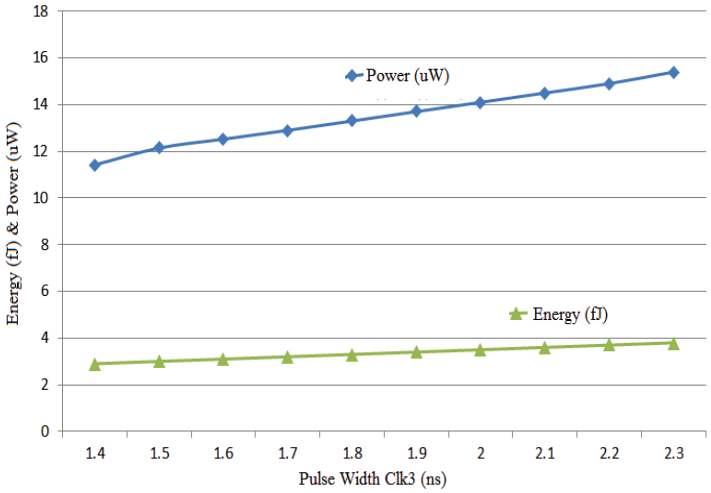

Fig. 7 Energy and power consumption versus clk3 pulse width in proposed technique

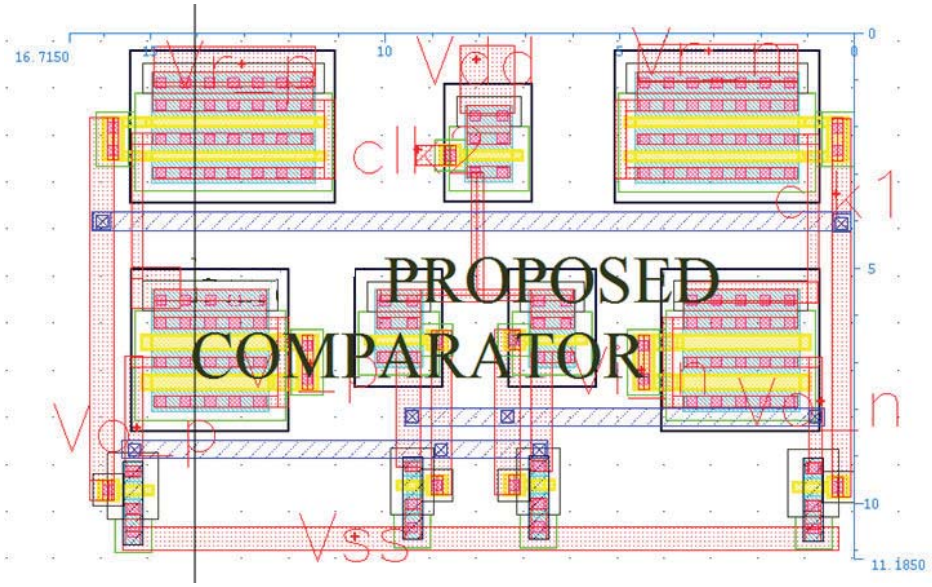

Fig. 8 Layout of the proposed comparator

V. Conclusions

In this paper, the basic structure of dynamic comparators employing two techniques for power consumption reduction and energy efficiency improvement has been presented. This comparator is designed and simulated in 180 nm CMOS process. Simulations show that power consumption for the proposed technique is 14.3 µW. Energy efficiency at 100 MHz is 3.7 nJ.

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