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A Simple and Efficient Method for Accurate Measurement and Control of Power Frequency Deviation

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***Abstract*—**In the presented technique, a simple method is given for accurate measurement and control of power frequency deviation. The sinusoidal signal for which the frequency deviation measurement is required is transformed to a low voltage level and passed through a zero crossing detector to convert it into a pulse train. Another stable square wave signal of 10 KHz is obtained using a crystal oscillator and decade dividing assemblies (DDA). These signals are combined digitally and then passed through decade counters to give a unique combination of pulses or levels, which are further encoded to make them equally suitable for both control applications and display units. The developed circuit using discrete components has a resolution of 0.5 Hz and completes measurement within 20 ms. The realized circuit is simulated and synthesized using Verilog HDL and subsequently implemented on FPGA. The results of measurement on FPGA are observed on a very high resolution logic analyzer. These results accurately match the simulation results as well as the results of same circuit implemented with discrete components. The proposed system is suitable for accurate measurement and control of power frequency deviation.

***Keywords*—**Digital encoder for frequency measurement, frequency deviation measurement, measurement and control systems, power systems.

I. Introduction

FREQUENCY is one of the most important parameter in power system and its apparatus. A lot of care is taken for its control as its variation affects the system performance quite considerably. A bulk of load in power system is constituted of induction motors, synchronous motors, transformers and other inductive and capacitive impedances. The power drawn by all these equipment is very much related to the frequency of supply source. For the same load torque, the stable operating speed of induction motor is changed with the deviation of frequency, consequently, changing the mechanical power output. For a synchronous motor running only on the synchronous speed which is directly proportional to supply frequency, the change in speed and hence, the change in mechanical load is quite evident. Capacitances are often used in power systems for series and parallel compensation and power factor improvement. The impedance of these capacitances often vary with deviation of frequency, disturbing the whole adjustment. A number of techniques have been proposed in the literature to measure the frequency deviation [1]-[6]. The scheme proposed in [5] gives high measurement resolution, but the delay introduced by the filtering operation is approximately two signal cycles. A cost effective microcontroller based measurement system has also been reported [6], which measures the frequency with an accuracy of three decimal places. However, the measurement range of frequency deviation is limited to ± 1 Hz. In a three-level discrete Fourier transform method the power frequency has been measured accurately [7]. However, the algorithms used are very complex and intricate. Some frequency deviation measurement techniques have also been reported using BCD up/down counter [8], an electronic bridge [9], or a mono-stable multi-vibrator [10]. In these methods, loss of one pulse over a fixed duration of measurement time causes a significant error [8]-[10]. Moreover, these methods require a stable high frequency signal and give the final output in the form of a number (counter′s output) which represents the frequency deviation from its nominal value. In this paper a circuit is developed using discrete components for frequency deviation measurement. A 10 KHz stable pulse is taken from a crystal oscillator and DDA. This signal is ANDed with signal under test (SUT), whose frequency deviation measurement is required. A train of pulses is produced at the output of AND gate, whenever SUT is high. The SUT is also inverted to clear the contents of counters. The train of pulses is counted by the counters and subsequently passed through a combinational logic circuit to give a unique combination of pulses/levels, which may be used directly to control the power system frequency deviation. The results of developed circuit are verified by behavioral model of Verilog HDL simulation as well as FPGA implementation.

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II. Realization

In the proposed method a sinusoidal signal whose frequency deviation measurement is required, is reduced to a low voltage level (2 volts). This signal is then passed through a zero crossing detector (ZCD) to convert it into a square wave signal A, which is applied to an AND gate (G_0) with another 10 KHz stable pulse train B. Signal A is also applied to an inverter (I_0) whose output is used to clear three decade counters whenever signal A is low. These decade counters (DC-1 to DC-3) are cascaded together (Fig. 1). The output of G_0 is applied to the first decade counter. For a 50 Hz sinusoidal signal, 100 pulses are passed through the counters whenever signal A is high (10 ms duration), as shown in Fig. 2. The Least Significant Bit (LSB) of third counter (DC-3) will be high and all other

outputs of all the three counters will be low (Table I). One pulse appears in every 10 ms duration if the output is taken from (LSB) of third counter (pin no.12 of DC-3). This pulse remains present for frequencies below 50 Hz and disappears for frequencies above 50 Hz (Table II). If the frequency of the signal A is deviated from its nominal value (increases), its duration decreases. Less than 100 pulses of signal B are passed through G_0 and counted by counters. Whereas if the frequency of signal A decreases, its duration increases. More than 100 pulses of signal B will be passed through G_0 and counted by counters. The outputs of the counters will be 1 or 0 accordingly as shown in Table I. If all the high state outputs of the three counters are applied to AND gates (G-46 to G-54) as shown in Fig. 1, then a unique combination of pulses is obtained at their outputs for each one Hz deviation (whenever signal A is HIGH) as shown in Table II.

Table I shows the output of three counters for deviation of 4 Hz above and below the nominal value (50 Hz).

Table II shows the output of different AND gates G-46 to G-54. The inputs of these gates are numbered according to connection of pin number of three decade counters, corresponding to a frequency deviation from 46 Hz to 54 Hz. It is clear from Table II that when the frequency is 46 Hz, a single pulse appears at gate no. G-46, G-47, G-48, pin no. 12, G-51, G-52, G-53 and 2 pulses appear at gate number G-49 and G-54. When the frequency of signal A is 47 Hz (time period of A is reduced) pulse of gate G-46 disappears. The pulses at the outputs of the other gates remain present. When the frequency increases to 54 Hz, the gate time is so much reduced that only a single pulse appears at gate number G-54, whereas no pulse appears at any other gate.

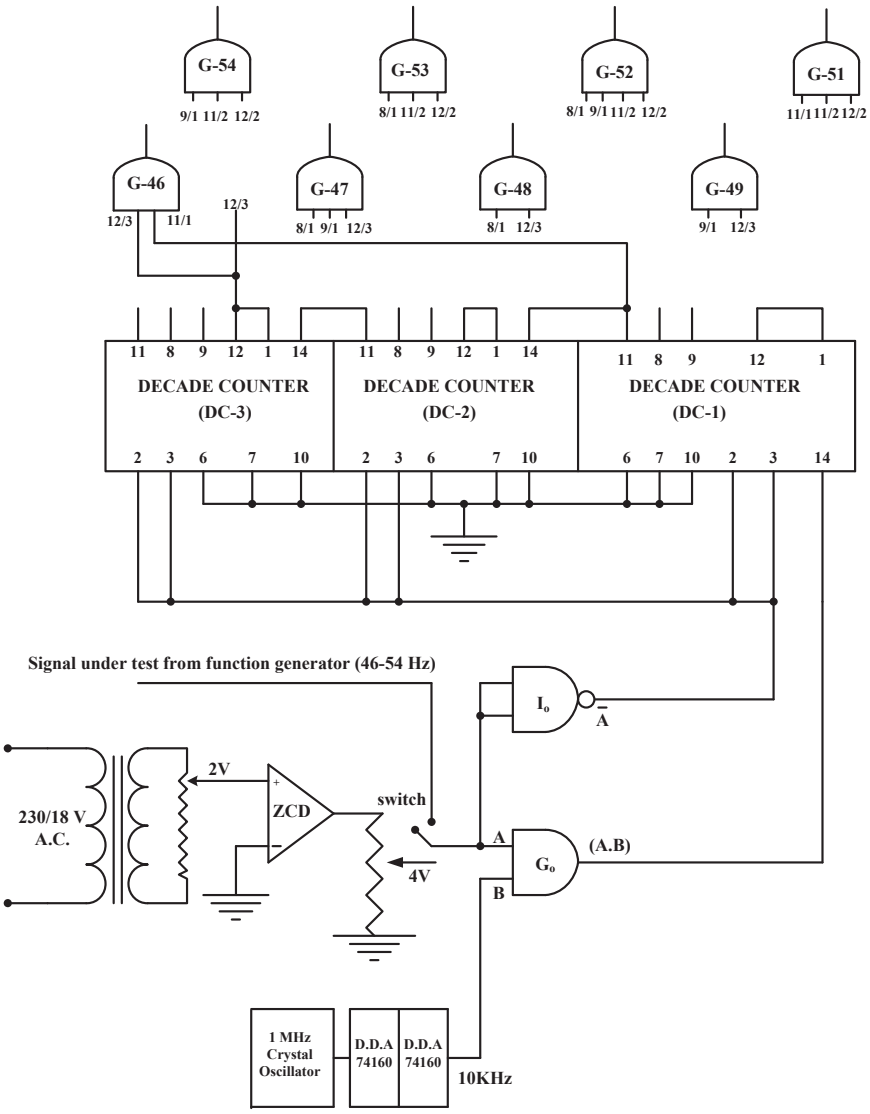

Fig. 1 A setup for frequency deviation measurement

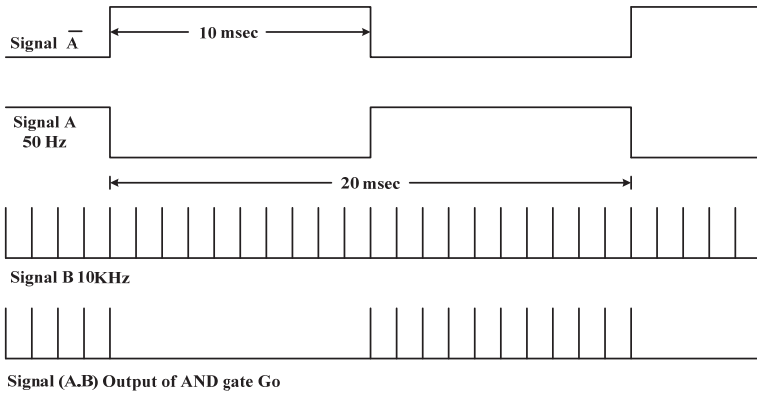

Fig. 2 Wave shapes of signals in the setup for frequency deviation measurement

TABLE I
OUTPUTS OF COUNTER

Frequency of signal A(Hz)	Decade CounterDC-3 Pin Nos. 11 8 9 12	Decade CounterDC-2 Pin Nos. 11 8 9 12	Decade CounterDC-1 Pin Nos. 11 8 9 12	No. of pulses passed through AND gate Go when A is high
46	0 0 0 1	0 0 0 0	1 0 0 0	108
47	0 0 0 1	0 0 0 0	0 1 1 0	106
48	0 0 0 1	0 0 0 0	0 1 0 0	104
49	0 0 0 1	0 0 0 0	0 0 1 0	102
50	0 0 0 1	0 0 0 0	0 0 0 0	100
51	0 0 0 0	1 0 0 1	1 0 0 0	98
52	0 0 0 0	1 0 0 1	0 1 1 0	96
53	0 0 0 0	1 0 0 1	0 1 0 0	94
54	0 0 0 0	1 0 0 1	0 0 1 0	92

TABLE II
OUTPUTS OF AND GATES

Frequency of signal A in Hz	G-46	G-47	G-48	G-49	50 Pin No.12	G-51	G-52	G-53	G-54
46	1	1	1	2	1	1	1	1	2
47	0	1	1	2	1	1	1	1	2
48	0	0	1	1	1	1	1	1	2
49	0	0	0	1	1	1	1	1	2
50	0	0	0	0	1	1	1	1	2
51	0	0	0	0	0	1	1	1	2
52	0	0	0	0	0	0	1	1	2
53	0	0	0	0	0	0	0	1	1
54	0	0	0	0	0	0	0	0	1

In the proposed method, the outputs are taken from the counters through AND gates so that unique combination of pulses is obtained. When the outputs are taken through latches, then stable high or low levels are obtained at the output of the AND gates. These voltages are directly applicable to drive display units for deviation conditions. The same voltages can be also used for control applications.

The functionality of the developed circuit is also verified by Verilog HDL simulation using Xilinx ISE tools. The results of simulation for frequency deviation with encoded bit stream are shown in Fig. 3. These results match with the results of hardware implementation of the circuit using discrete components (Table II). The behavioral Verilog model is also synthesized into a functional gate level netlist and the generated bit stream is transferred on an FPGA kit to realize the circuit shown in Fig. 1. The results of the implemented circuit on FPGA for frequency deviation are recorded on a very high resolution logic analyzer (Fig. 4). These results accurately match with the simulation results (Fig. 3) as well as the results of same circuit realized with discrete components (Table II).

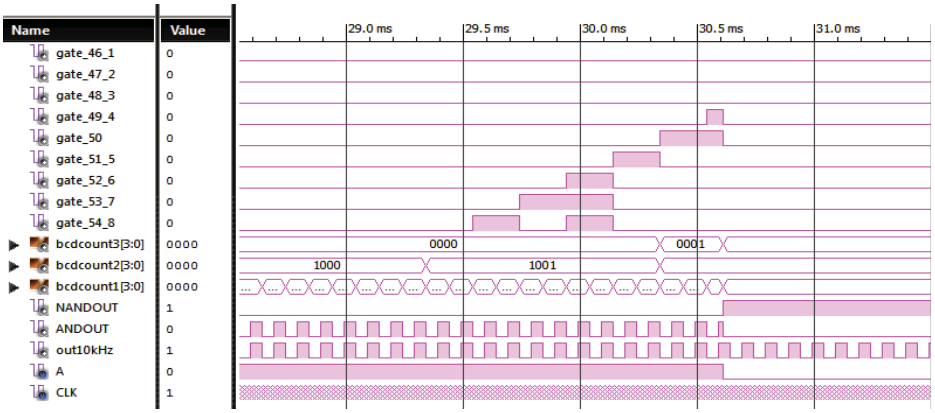

Fig. 3 (a) Simulation result at 49 Hz with encoded pulse stream 00011112

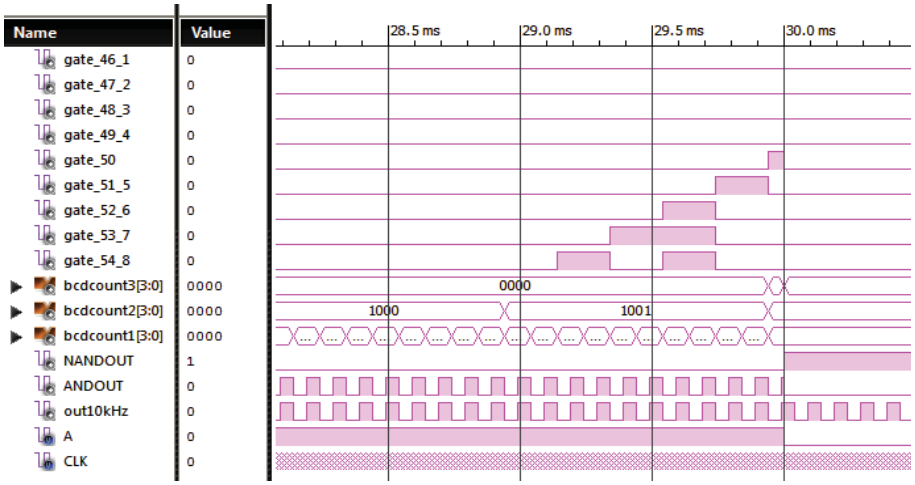

Fig. 3 (b) Simulation result at 50 Hz with encoded pulse stream 00001112

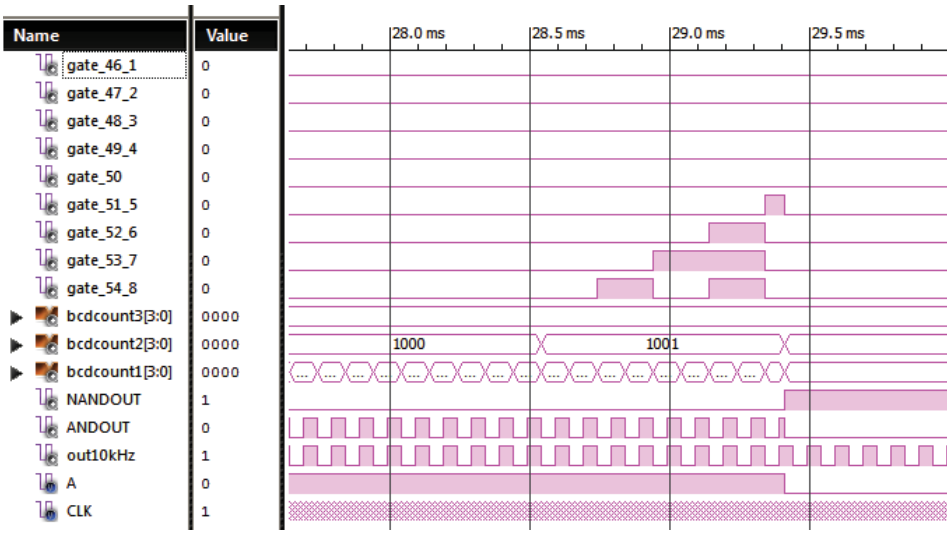

Fig. 3 (c) Simulation result at 51 Hz with encoded pulse stream 00000112

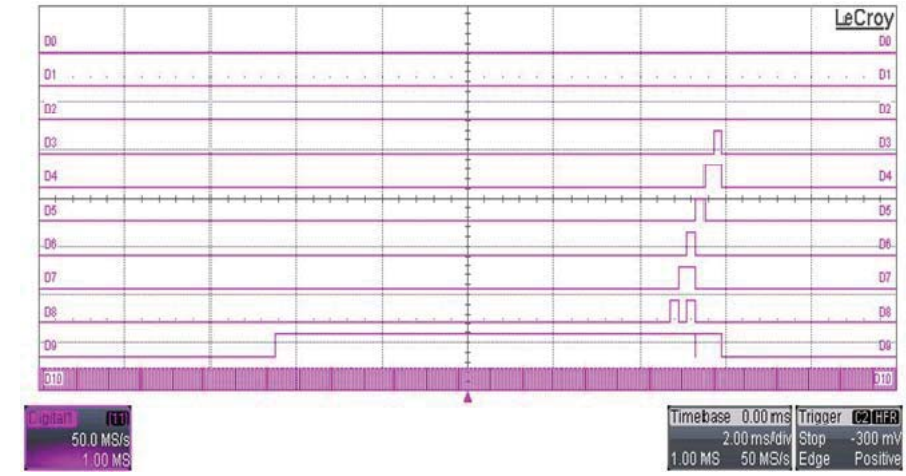

Fig. 4 (a) Results of the FPGA at 49 Hz recorded on a high resolution logic analyzer

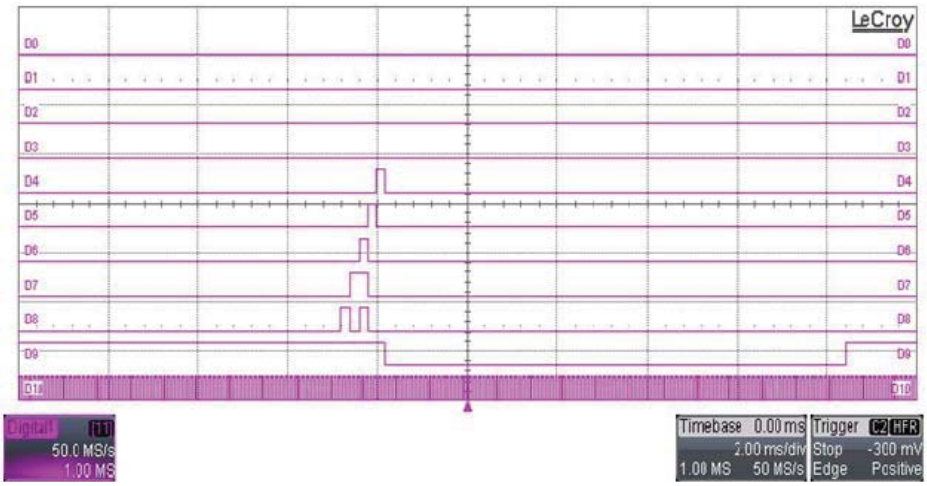

Fig. 4 (b) Results of the FPGA at 50 Hz recorded on a high resolution logic analyzer

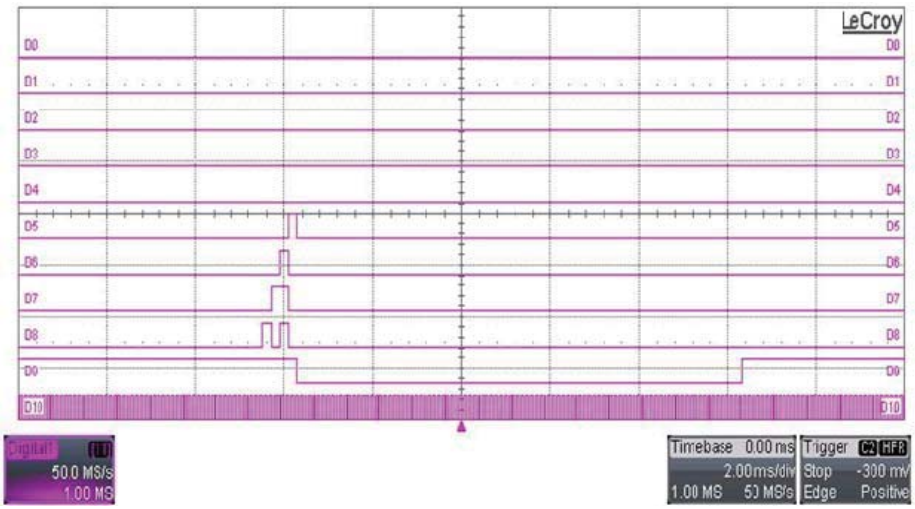

Fig. 4 (c) Results of the FPGA at 51 Hz recorded on a high resolution logic analyzer

III. Conclusion

The developed circuit is tested experimentally and give satisfactory results. For testing the circuit, the SUT is taken from a function generator through a switch to obtain the known frequency deviation above and below the nominal value of 50 Hz. With three counters used at the output stage, the proposed scheme gives a resolution of 0.5 Hz within 20 ms of the measurement period. The resolution can be increased by simply increasing the frequency of stable high frequency pulse. However, this requires additional counters and gates at the output stage. The circuit is simulated and synthesized with behavioral model of Verilog HDL and successfully realized using FPGA. The measured results on FPGA are recorded on a very high resolution logic analyzer. These results match with the simulation results as well as the results obtained on hardware using discrete components.

Acknowledgment

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