International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:8, No:8, 2014

Performance Analysis of BPJLT with Different Gate and Spacer Materials

Porag Jyoti Ligira, Gargi Khanna

Abstract**—**The paper presents a simulation study of the electrical characteristic of Bulk Planar Junctionless Transistor (BPJLT) using spacer. The BPJLT is a transistor without any PN junctions in the vertical direction. It is a gate controlled variable resistor. The characteristics of BPJLT are analyzed by varying the oxide material under the gate. It can be shown from the simulation that an ideal subthreshold slope of ~60 mV/decade can be achieved by using high-*k* dielectric. The effects of variation of spacer length and material on the electrical characteristic of BPJLT are also investigated in the paper. The I_{ON} / I_{OFF} ratio improvement is of the order of 10^7 and the OFF current reduction of 10^{-4} is obtained by using gate dielectric of HfO_2 instead of SiO_2.

Keywords**—**BPJLT, double gate, high-k, spacer.

I. Introduction

THE down scaling of transistor requires super steep and ultra shallow doping profile in source, drain and channel region. A new device structure based on Lilienfield's first transistor architecture [1] which doesn't have any junction has been proposed and fabricated called the junctionless transistor [2]. The BPJLT don't have any PN junction in vertical direction but it consists of junction in the horizontal direction. The BPJLT have same doping concentration in source, drain and channel unlike inversion mode transistor which have different doping concentration. The BPLT is an accumulation mode device, where bulk channel conduction takes place instead of surface conduction. During ON state it has large current due to high doping concentration of the channel region. In OFF state the carrier is depleted due to the work function difference between the semiconductor and the gate material [3]. The cross sectional area of the device should be small so that the carriers can be depleted during OFF state. The junctionless transistor has the following advantage compared to the MOSFET 1) deep source/drain implants are avoided 2) low thermal budget 3) better short channel effect [4].

The junctionless transistors already proposed are SOI [4], Bulk Planar [5], Double Gate [6] and Tunnel [7]. A. Kranti et al. has done comparison of conduction mechanism in junctionless, inversion and accumulation devices [4]. R.K. Baruah has analyzed the process induced variability on the electrical characteristic of Double gate junctionless transistor [6]. B. Ghosh et al. have emphasized on tunnel junctionless transistor with low subthreshold slope using low-k spacer [8]. S. Gundapaneni et al. has proposed the idea of Bulk Planar Junctionless Transistor [5]. The BPJLTT is an attractive device for scaling as it fully compatible with CMOS process. The systematic investigation of spacer and different oxide material is still missing in the literature. The paper investigates the impact of different oxide material on the electrical characteristic of BPJLT and suggest best possible candidate. BPJLT with spacer has been proposed for better short channel effects and electrical characteristic. During ON state the spacer has marginal effect on the ON current. But during OFF state current reduces due to the spacer and have better controllability on the Short channel effects. First, the device concept and simulations are outlined in Section II. Device structure and operation is presented in Section III. Results and discussion are presented. Finally, Section IV concludes the work done.

Porag Jyoti Ligira is with the National Institute of Technology, Hamirpur, India, 177005 (phone 9736163564; e-mail: poragligira@gmail.com).
Gargi Khanna is with the National Institute of Technology, Hamirpur, India, 177005 (phone 9805870101; e-mail: gargikhanna20@gmail.com).

II. Device Structure

The device structure corresponds to n channel Junctionless transistor is shown in Fig. 1. The workfunction of the metal are considered to be 5.1eV with aluminum. Here the device layer is deposited above the bulk silicon, both bulk silicon and device layer have opposite polarity. There is a junction depth of X_j between the device layer and bulk silicon. The device do not have junction in vertical direction but there is junction in horizontal direction. Due to absence of vertical junction, the JLT results in better scalability and ease of fabrication. Thin gate dielectric and metal is present above the device layer with workfunction of 5.1eV. The gate should have opposite workfunction with respect to the device layer. There is no conduction between source and drain when we apply zero bias as the device layer is depleted from top and bottom due to the work function difference between gate and device layer at top and due opposite doping device layer and bulk at bottom. Device layer will come out of depletion as we apply positive bias to the gate. The oxide material is varied to see its effect on the electrical characteristic of the device. The materials considered are SiO_2 (3.9eV), Si_3N_4 (7.5eV), Al_2O_3 (9.6eV) and HfO_2 (21eV) and ZrO_2 (25eV). Fig. 2 shows BPJLT structure with spacer, spacer is taken on both side of the oxide, the effect on the electrical characteristic is observed by varying its length. The spacer material is varied and its effect on different electrical characteristics is studied.

III. Results & Discussions

Three-dimensional simulations of the bulk JLT are carried out using the Sentaurus 3-D device simulator. This solves the self-consistent drift-diffusion equations for electrons and

holes. In the simulation the mobility model is used, which take care of doping and transverse field dependence, Schottky-Read-Hall mechanisms. Due to high doping concentration band gap narrowing model is also included [9]. Fig. 3 shows I_d and V_g for bulk planar junctionless transistor with and without spacer. The junctionless transistor shows nearly same ON current as the inversion mode transistor. But junctionless transistor have better OFF current then Inversion mode transistor. The better OFF current is due to depletion of carrier from the channel when we apply zero bias to junctionless due to workfunction difference. In case of inversion mode transistor the carriers not fully depleted which is responsible for less OFF current. Thus in junctionless transistor the gate have better control over the channel then in case of Inversion mode transistor. The doping concentration of junctionless transistor degrades the mobility to some extent but low surface field in ON state enhances the mobility, overall we have a comparable ON current with respect Inversion mode devices.

TABLE I
PARAMETER FOR DEVICE SIMULATION

Parameter	Value
Device layer Thickness	5nm
Gate Dielectric	1nm
Donor doping concentration device layer	2.0e+19
Well Doping	5.0e+18
Channel Length	20nm
Supply voltage	1V

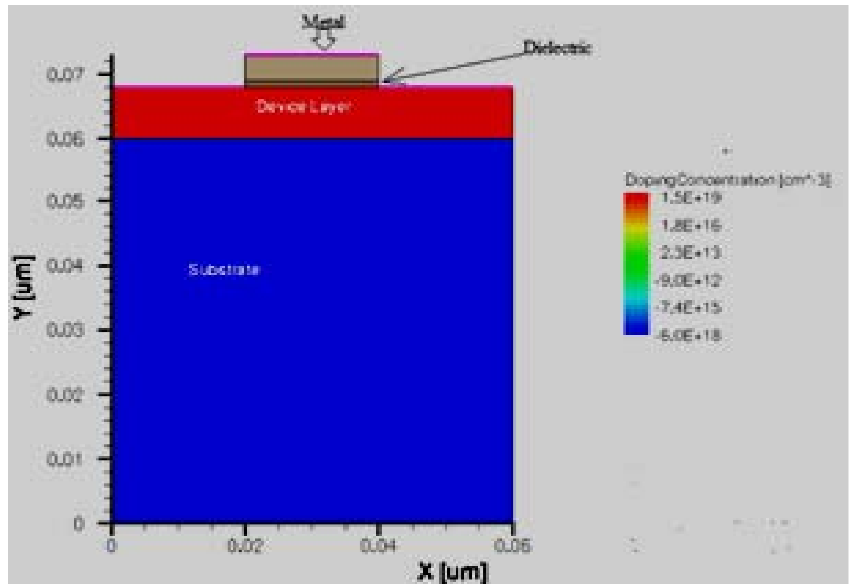

Fig. 1 Bulk planar junctionless transistor

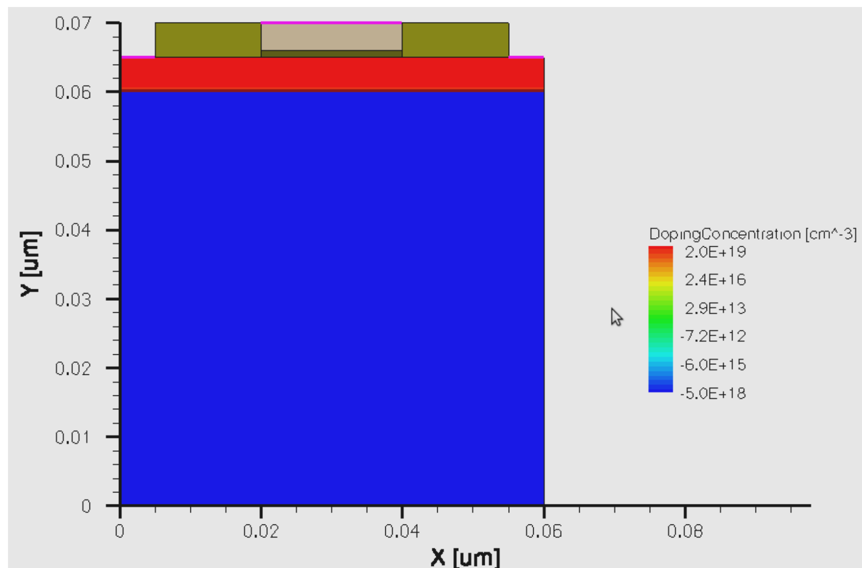

Fig. 2 Bulk planar junctionless transistor with spacer

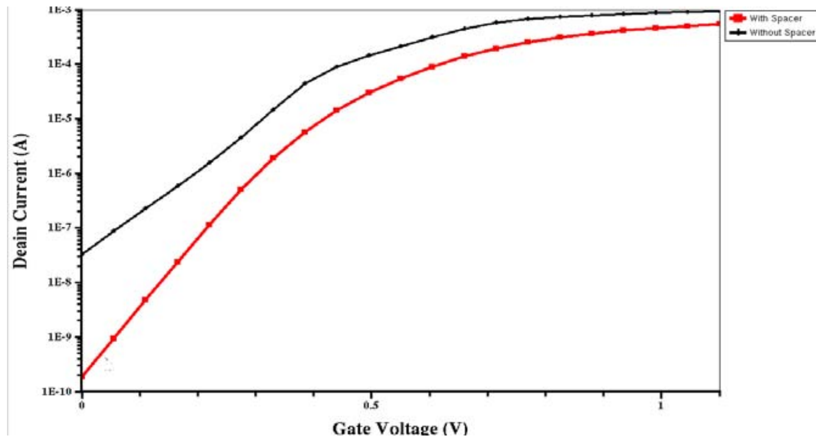

Fig. 3 I_d and V_g for bulk planar junctionless transistor with and without spacer

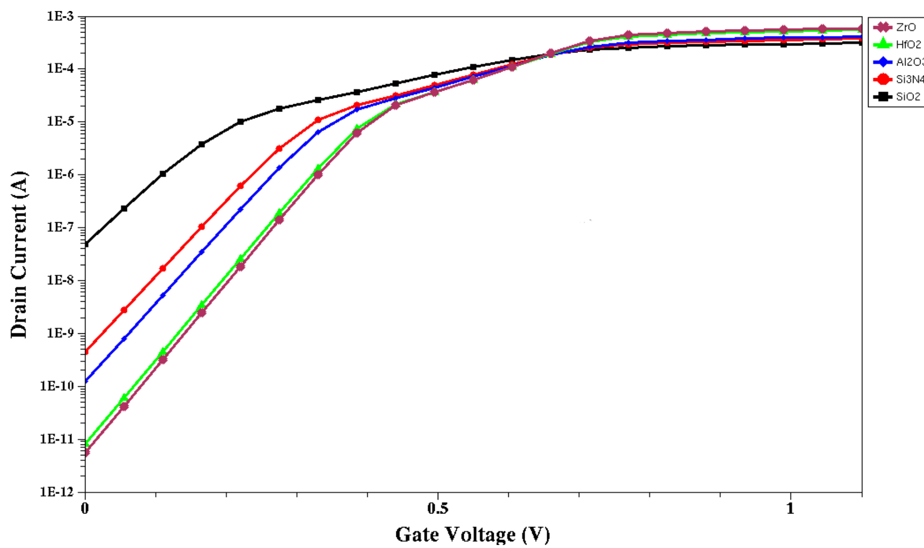

Fig. 4 I_d vs. V_g of BPJLT for different oxide material

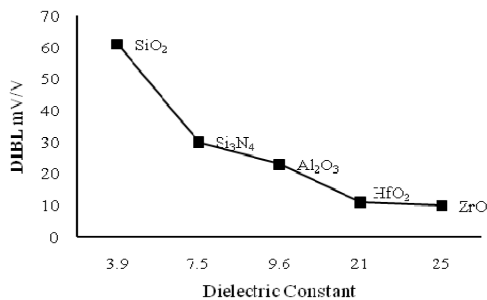

Fig. 5 Variation of DIBL for different Oxide material

Fig. 4 shows the variation of I_d and V_g of BPJLT for different gate oxide material. The high-k material shows better electrical characteristic then *low-k* material. The materials with *high-k* are more preferable because it reduces the leakage current during the OFF state as compared to the *low-k* dielectric. The leakage current increases as the gate loses the control over the channel. Fig. 5 shows the variation DIBL for different Oxide material. As the graph moves from low-k to *high-k* an optimum DIBL can be achieved. Fig. 6 shows I_{ON}/I_{OFF} and subthreshold slope variation for different Oxide material. A nearly ideal subthreshold slope can be achieved. Due to the increment in the capacitance value the gate tunneling current reduces with the use of *high-k* dielectric.

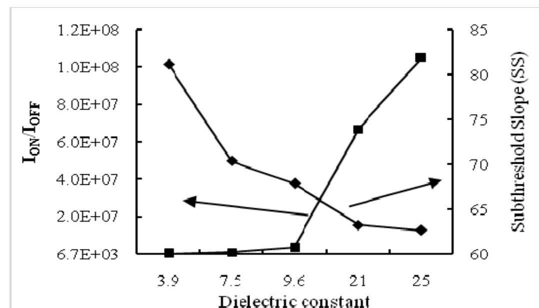

Fig. 6 I_{ON}/I_{OFF} and Subthreshold slope variation for different Oxide material

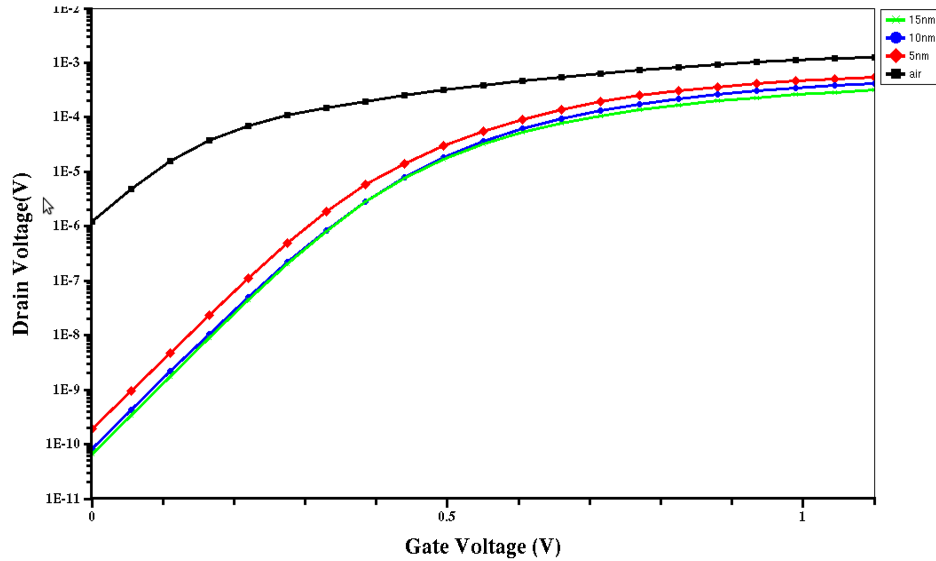

Fig. 7 I_d and V_g for bulk planar junctionless transistor for different spacer length

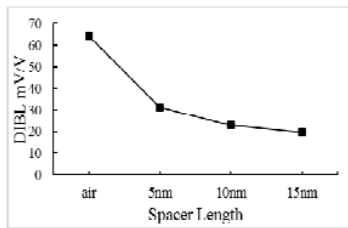

Fig. 8 DIBL variation for different spacer length

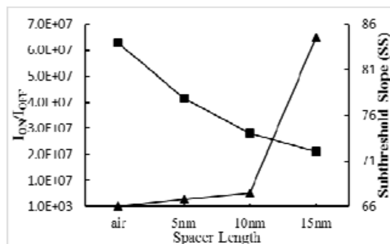

Fig. 9 I_{ON}/I_{OFF} and subthreshold slope variation for different spacer length

The use of *high-k* dielectric reduces the short channel effects and increases the control of gate on the channel. Fig. 7 shows I_D and V_G for bulk planar junctionless transistor for different spacer length. The other parameter is taken constant and spacer length is varied from 0 to 15 nm. There is 99% reduction in OFF current as we increase the spacer length from 0 to 15nm. It is observed that the increment of spacer layer reduces the OFF state current. Fig. 8 shows DIBL variation for different spacer length. As we increase the spacer length an optimum DIBL can be obtained. Fig. 9 shows I_{ON}/I_{OFF} and Subthreshold slope variation for different spacer length. A nearly ideal subthreshold can be obtained. As we increase the spacer length the leakage current decreases as the OFF state channel length increases. But during ON state there is less variation on current as spacer does effect the vertical electric field of the device. So for better performance of the device spacer length of 15nm is preferable to reduce short channel effect.

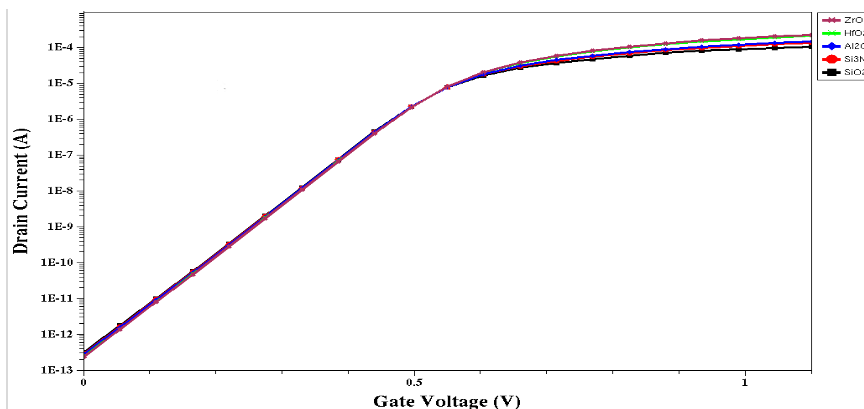

Fig. 10 I_d and V_g of for bulk planar junctionless transistor with different spacer material

Fig. 10 shows the I_d and V_g for bulk planar junctionless transistor for different spacer material. The spacer length is kept constant at 15 nm and spacer material is varied. The *high-k* spacer shows better electrical characteristic then *low-k*. Fig. 11 shows DIBL variation for different spacer material. A low DIBL value can be obtained for *high-k* dielectric. Fig. 12 shows I_{ON}/I_{OFF} and Subthreshold slope variation for different Oxide material. For *high-k* material a nearly ideal subthreshold slope can be achieved due because of reduction fringing electric field in the OFF state. During ON state the spacer has no effect on the device electrical characteristic but in OFF state it reduces Fringing electric field and as a result reduces the leakage current.

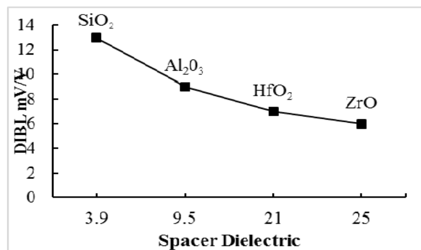

Fig. 11 DIBL variation for different spacer material

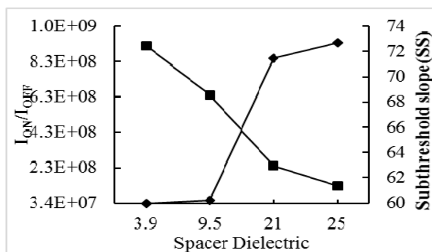

Fig. 12 I_{ON}/I_{OFF} and Subthreshold slope variation for different spacer material

IV. Conclusion

Bulk planar junctionless transistor exhibits better device characteristic then Inversion mode transistor. The junctionless transistor removes the problem of high doping source and drain. The oxide material should be *high-k* for better electrical characteristic. The length of spacer should be maximum for reduction of short channel effects. It is concluded that in OFF state current can be reduced by the use of *high-k* dielectric spacer layer. Since the device dimensions are very less there is need for more variability study in case of junctionless transistor. Thus bulk planar junctionless transistor can serve as the better replacement of MOS devices.

References

[1] J. E. Lilienfeld, "Method and apparatus for controlling electric current,"U.S. Patent 1 745 175, Oct. 22, 1925.

[2] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junctionless multigate field-effect transistor," Appl. Phys. Lett., vol. 94, no. 5, pp. 053511-1–053511-2, Feb. 2009.

[3] J.-P. Colinge et al., "Nanowire resistors without junctions," Nat. Nanotechnology., vol. 5, no. 3, pp. 225–229, Mar. 2010.

[4] A. Kranti et al., "Junctionless nanowire transistor: Properties and design guidelines," IEEE 34th Eur. Solid-State Device Res. Conf., pp. 357–360, Aug. 2010.

[5] S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. Murali,S. Ganguly, and A. Kottantharayil, "Effect of band-to-band tunneling on Junctionless transistors," IEEE Trans. Electron Devices, vol. 59, no. 4,pp. 1023–1029, Apr. 2012.

[6] R.K. Baruah, R.P. Paily, "Estimation of process-induced variations in double-gate Junctionless transistor", CODEC, IEEE International Conference, pp.1-4, 2012.

[7] B. Ghosh and M. W. Akram, "Junctionless Tunnel Field Effect Transistor", IEEE electron device letters, vol. 34, no. 5, 2013.

[8] B. Ghosh, P. Bal, P. Mondol, "A junctionless tunnel field effect transistor with low subthreshold slope", Springer , Journal of Computational Electronics, vol. 12, no. 3, pp.428-436, 2013.

[9] Sentaurus Device User Guide, Synopsys, Inc. Mountain View, CA, 2008.

Porag Jyoti Ligira obtained the B.E degree in Electronics and Communication from RMNU University, Nagpur, India in 2011. He is presently working toward the M. Tech degree in VLSI design and automation technique at Department of Electronics & Communication, National Institute of Technology, Hamirpur, India. His current research interests include nanoscale devices and modeling.

Gargi Khanna obtained her B.Tech. Degree in Electronics & Comm. Engineering from REC Hamirpur, India in 1997. She did her M.E. from PEC Chandigarh, India in 2002. She was awarded Ph.D. degree from NIT Hamirpur ,India in year 2012.

Presently Dr. Khanna is working as Assistant Professor in Electronics and Communication Engg. Department at NIT Hamirpur HP. Her area of research is Low Power VLSI Design. Dr. Khanna is member of ISTE and IEEE. She has 10 research papers in international journal of repute and over 40 papers in national and international conferences.