International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:8, No:8, 2014

SiC Merged PiN and Schottky (MPS) Power Diodes Electrothermal Modeling in SPICE

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***Abstract*—**This paper sets out a behavioral macro-model of a Merged PiN and Schottky (MPS) diode based on silicon carbide (SiC). This model holds good for both static and dynamic electro-thermal simulations for industrial applications. Its parameters have been worked out from datasheets curves by drawing on the optimization method: Simulated Annealing (SA) for the SiC MPS diodes made available in the industry. The model also adopts the Analog Behavioral Model (ABM) of PSPICE in which it has been implemented. The thermal behavior of the devices was also taken into consideration by making use of Foster' canonical network as figured out from electro-thermal measurement provided by the manufacturer of the device.

***Keywords*—**SiC MPS Diode, electro-thermal, SPICE Model.

I. Introduction

THE silicon carbide power devices are the most promising semiconductor devices for industrial power applications, for they are characterized by a high heat resistance, excellent thermal properties and effective performance at high switching frequencies and power levels. Nowadays, the MPS diodes are the most widely used, and provide a better adjustment between the forward voltage drops and reverse bias leakage current, following a voltage drop at the junction level [1], [2].

Nevertheless; untill now no excellent model has been conjured up, which will be qualified to predict the characteristics of the semiconductor device in a relatively wide-ranging operating temperature. Moreover; the accurate forecasting of the device behavior is still necessarily entailed for a vigorous supply design and for predicting electromagnetic interferences (EMI). And while there are classical models of SPICE based on physics of semiconductor [3]-[6], and others provided by manufacturers, none of them, however, can produce precise characteristics of a temperature-dependent device.

II. Behavioral Macro Model of MPS Diodes in Spice

Although several macro-model of MPS diode power have been proposed in Spice [7]-[9], they are, however, rather complex in the extraction of their parameters, unlike the proposed model which is quite simple, flexible and very much practical for all types of semiconductor. This model is made up of two parts; one electrical consisting, in the static state, of forward voltage drop and reverse bias leakage current; and in the dynamic state, of the reverse bias charge; the other is thermal and takes the form of an RC Foster network [10], [11]. This model is represented in the Fig. 1.

A. The Electrical Part of the Model

1. The Forward Voltage Drop

On our part we propose a simpler way to modelize the characteristics of the diode's forward voltage drop by using the ABM blocks of the SPICE; i.e. by having recourse to a voltage controlled voltage source (VCVS) controlled by the appropriate equation. In order to clearly distinguish between forward and reverse bias conditions, the forward voltage drop model includes a "reference diode" series with the VSCV E4 and in which the parameters N and Temp are set to specific values, "N = 0.5" and "Temp=27ºC" [12]-[14].

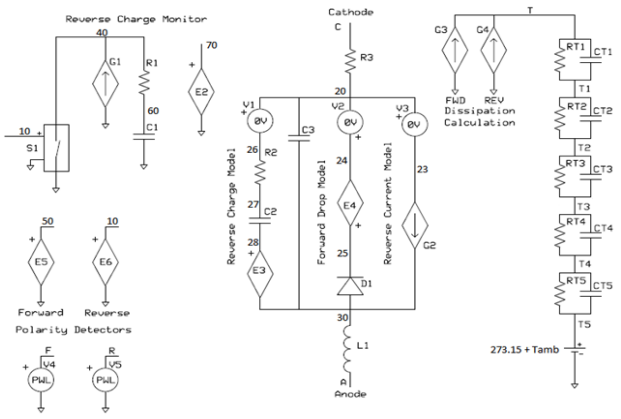

Fig. 1 The Subcircuit Diagram proposed model

The parameters of the diode change in the course of the time, while the parameters of the reference diode retain their default values unchanged. The forward voltage drop of the reference diode, shown in Fig. 2, has an approximately constant and low variation, depending on the current; whereas taking account of temperature is provided by the VCVS E4 in series with the reference diode.

The forward Voltage drop can be represented by the logarithmic component (2) plus the reference diode's constant drop voltage component ID * RS (3) which is due to an Rs resistance that represents the sum of both the diffusion substrate resistance and contact resistance [15].

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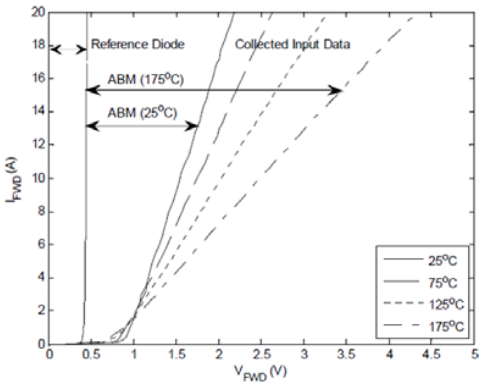

Fig. 2 Voltage drop contributions with current

$$I_D = I_S\left(\exp\left(\frac{q.V_j}{K.T}\right)+1\right) \quad (1)$$

$$Vj = \log\left(\frac{ID}{Is}+1\right)\times\left(VF10+VF11\times V(T)+VF12\times V(T)^2\right)\times 0.0257 \quad (2)$$

$$Vc = I(V2)\times\left(VF20+VF21\times V(T)+VF22\times V(T)^2\right) \quad (3)$$

here VF10, VF11, VF12, VF20, VF21, and VF22 (see Table I) are the coefficients of the interpolation polynomial of the curve (temperature-dependent forward voltage drop) provided by the manufacturer.

2. The Leakage Current in Reverse

It is well known that modeling the reverse bias leakage current and breakdown voltage has evoked much attention in power electronic literature such as in Mantooth for example [16] where five reverse bias effects were added to the saturation current of the diode in Saber platform; while Maxim [17] proposed in turn a model based on the physics of semiconductor, with SPICE ABM blocks, including the reverse bias leakage current and avalanche effects.

The effects of leakage current and breakdown voltage may be either significant or otherwise in accordance with the voltage and power levels of the converter. In cases when one of these characteristics is insignificant, the model can be further simplified (by reducing complexity and the time of simulation).

However; if the leakage current vastly contributes to dissipation then it can be modeled by G2 which is an ABM source current controlled by an equation determined on the basis of the manufacturer's data. The control equation of the G2 is:

$$IR = (Eq1)\times\left(\frac{V(A)^2}{Eq2}\right)^{(Eq3)}$$
$$Eq1 = IR10+IR11\times V(T)+IR12\times V(T)^2$$
$$Eq2 = IR20+IR21\times V(T)+IR22\times V(T)^2 \quad (4)$$
$$Eq3 = IR30+IR31\times V(T)+IR32\times V(T)^2$$

The above IR10, IR11, IR12, IR20, IR21, F22, IR30, IR31, and IR32 are the coefficients of the interpolation polynomial of the curve (reverse bias leakage current as a function of temperature) given by the manufacturer.

3. The Reverse Bias

The reverse recovery phenomenon takes place when a negative voltage is applied to the terminals of a conductive diode, yielding up the curves shown in Fig. 3. The curve of the current is split into three phases [18]:

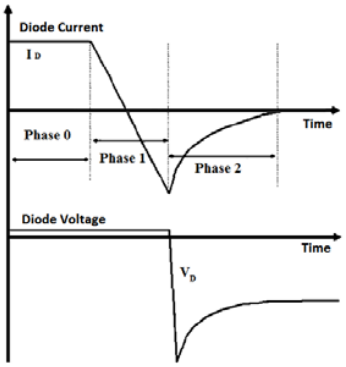

Fig. 3 The tree phases of reverse recovery

Phase 0: ends when the diode begins to turn off.

Phase 1: is the charge storing stage during which excessive charges in the P region evacuated out. The charge control equation for minority carriers in the turn-off process is written as follows:

$$\frac{dQ(t)}{dt}+\frac{Q(t)}{\tau_F} = -i_n(0,t) = -i(t) \quad (5)$$

If we consider the current through the depletion capacity as well, (5) can be rewritten as follows:

$$\frac{dQ(t)}{dt}+\frac{Q(t)}{\tau_F}-C_{jn}\frac{dv(t)}{dt} = -i(t) \quad (6)$$

Phase 2: During this phase, the control and variation of the charge are non-linear (see Fig. 3), and in this case, the latter is described by (7) [17].

$$|Q(t)| = |i(t).\tau_R| \quad (7)$$

The current through Cjn cannot be overlooked since a junction voltage is about to be generated. So we use (6) as a charge control equation.

By applying this reasoning to our model:

It follows that the turn-off of the diode starts when the switch S1 is turned on and results in the G1 current flow through the R1-C1 circuit (Fig. 1). The E2 source (VCVS) controlled by a voltage V(60) across C1, generates at its output a voltage V(70), which is the control voltage source E3 (VCVS). Initially, this voltage (V(70)) has a negative value which allows a linear storage of the charges in the capacitor C3 (5). As soon as the voltage E3 (8) becomes positive, reverse recovery phase (phase 2) starts and instigates removal

of C3 charges through the R2 resistor. Once V (E3) reaches its maximum value, the capacitor C2 obtains the same potential across its terminals; Then the I(V1) current vanishes, cancels G1 input and sets its output current to 0 value, so that the output voltages of E2 and E3 sources automatically reaches zero (Fig. 1).

$$V = V(70) \times \left(QR10 + QR11 \times V(70) + QR12 \times V(70)^2 \right) \quad (8)$$

QR10, QR11, and QR12 are the coefficients of the interpolation polynomial of the curve (variation of the C capacitor as a function of Vrev reverse voltage) given by the manufacturer.

B. The Thermal Part Model

The thermal impedance provided by the manufacturer's datasheet represents the instantaneous increase in the junction temperature of the device as a function of time [19]. It is represented by the RC pair of cells [20]-[23], and is dependent on the size of the semiconductor, the number and type of layers between the semiconductor and its case, and also the electrical insulation material. For our model we used 5 cells RC parallel.

The values of Ri and Ci are derived from the datasheet curve [19], [25]-[28], and calculated depending on Zth values (column Y) and τi (column X) for each n RC pairs according to (9).

$$Z_{Th}(t) = \sum_{i=1}^{n} R_i \left(1 - \exp\left(\frac{-t}{\tau_i} \right) \right) \quad (9)$$

We first determine ZThmax maximum value (in permanent state), and then the approximate values of the first pole position which are defined by ZTh and its corresponding τ (x-axis) (10). The remained values of Rn and τn are respectively determined according to (11) and (12).

$$Z_{Th} = 0.7 \times Z_{Thmax} \quad (10)$$

$$R_n = R_1 \times 0.5^n \quad (11)$$

$$\tau_n = \frac{\tau_1}{n} \left(0.1^{n-1} \right) \quad (12)$$

We use the Simulated Annealing (SA) [24], technique to browse randomly (starting from an initialization) the pair values Zth and τ. Then, we compare the error of the current iteration with the best error formerly found. The latter is calculated by the least squares (LS) method for each time step (i) (13).

$$\text{Erreur} = \sum_{1}^{i} \left(\frac{R_\theta(i) - R_\theta(i)\text{best}}{R_\theta(i)\text{best}} \right)^2 \quad (13)$$

III. Results

To assess the accuracy of the proposed model described in II, we performed simulations of some SiC MPS Diodes models (C3D04060E [19], CSD04060 [25], CSD10030 [26], SDP04S60 [27], SDP10S30 [28]), by using Orcad 16.6 Spice simulator. The values of model parameters obtained for all the tested devices are summarized in the below table as follows:

TABLE I
THE CAPITALS, ASSETS AND REVENUE IN LISTED BANKS

	C3D04060E	CSD04060	CSD10030	SDP04S60	SDP10S30
Thermal Parameters					
TR1	2.432e-01	5.654e-01	5.838e-01	3.459e-02	1.450e-01
TR2	9.938e-01	1.353e+00	4.679e-01	6.801e-01	3.305e-01
TR TR3	1.211e+00	4.806e-01	7.535e-01	2.115e+00	9.898e-01
TR4	2.675e-01	7.073e-02	7.535e-01	1.613e-01	1.067e-01
TR5	4.541e-02	1.874e-02	2.107e-02	3.287e-01	1.816e-01
TC1	4.363e-01	5.609e-01	2.484e-01	6.597e+01	5.359e-01
TC2	1.890e-02	3.401e-03	2.955e-02	3.550e-02	4.597e-02
TC TC3	1.674e-03	8.970e-04	2.058e-03	1.230e-03	4.028e-03
TC4	1.671e-03	1.341e-04	4.246e-04	2.679e-04	1.141e-03
TC5	1.337e-03	3.021e-05	4.309e-05	1.375e-08	2.031e-07
Forward Voltage Drop					
VF10	5.871e-01	8.862e-01	7.123e-01	8.659e-01	9.548e-01
VF11	9.642e-04	-8.151e-05	-1.721e-03	1.398e-04	-8.042e-04
VF12	-2.991e-06	-1.729e-06	5.297e-07	-2.238e-06	-6.598e-07
VF20	2.885e-01	2.957e-01	9.332e-02	3.963e-01	1.001e-01
VF21	-1.426e-03	-1.732e-03	-3.877e-04	-1.967e-03	-3.816e-04
VF22	2.847e-06	3.794e-06	8.559e-07	3.956e-06	6.596e-07
Reverse Bias Charge					
QR10	8.894e-03	7.124e-03	2.449e-03	1.331e-02	2.750e-03
QR11	4.072e-04	2.804e-04	2.166e-04	5.901e-04	2.178e-04
QR12	-1.223e-06	- 4.905e-07	-6.314e-07	-6.917e-07	-5.722e-07
Reverse Bias Leakage Current					
IR10	9.452e+00	4.131e+00	9.443e+02	1.080e+03	-5.312e+03
IR11	-4.458e-02	-1.024e-02	-5.433e+00	-6.624e+00	1.179e+01
IR12	5.279e-05	1.499e-05	7.720e-03	1.011e-02	1.899e-02
IR20	-6.145e+01	3.139e+02	4.282e+02	8.983e+02	2.593e+03
IR21	5.100e+00	1.285e+00	5.984e-01	1.376e+00	-9.529e+00
IR22	-9.340e-03	-2.328e-03	-3.170e-03	-2.876e-03	1.403e-02
IR30	-1.070e+02	-8.821e+00	9.213e+00	6.234e+00	-2.737e+01
IR31	6.884e-01	1.222e-01	7.580e-02	-2.149e-02	1.679e-01
IR32	-9.643e-04	-1.824e-04	-2.087e-04	4.070e-05	-2.159e-04

The external environment is presented by a voltage source whose value is the ambient temperature (Fig. 1). This model is valid for the 2nd and 3rd generation SiC MPS diodes.

The simulation results showed excellent correspondence to the measured curves provided by the manufacturer's datasheets for all voltages and currents in both forward and reverse bias, and in a wide range of operating temperature. An example of the obtained results for the simulations of CSD04060 diode in forward and reverse bias is shown respectively in Figs. 4 and 5, and all the curves of these figures correspond to the 25°C, 75°C, 125°C and 150°C temperature values. The thermal impedance curve is shown in Fig. 6 and the reverse recovery charge in Fig. 7. All these curves are presented with error bars of 5%.

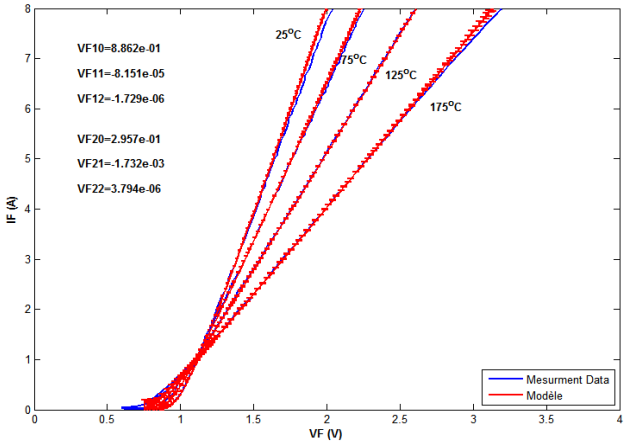

Fig. 4 Measured and simulated static forward characteristics of the CSD04060 MPS SiC diode

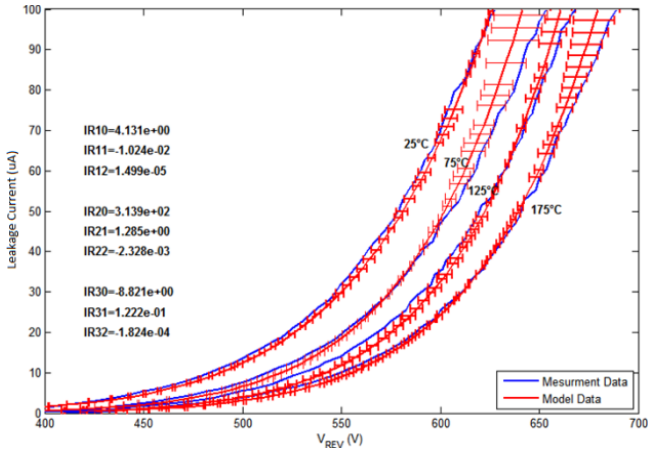

Fig. 5 Measured and simulated static reverse characteristics of the CSD04060 MPS SiC diode

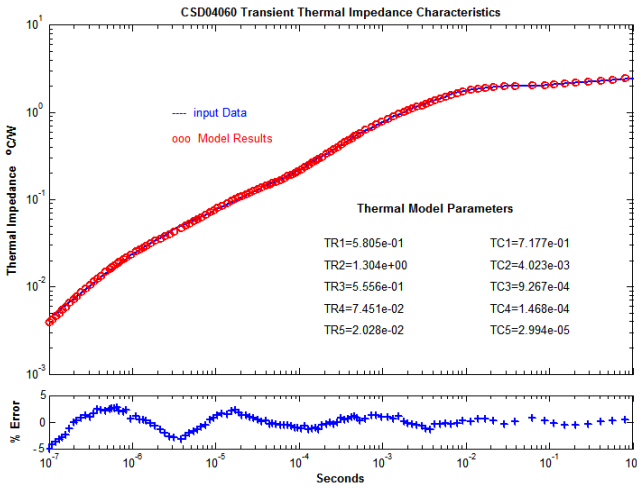

Fig. 6 Measured and simulated thermal impedance characteristics of the CSD04060 MPS SiC diode

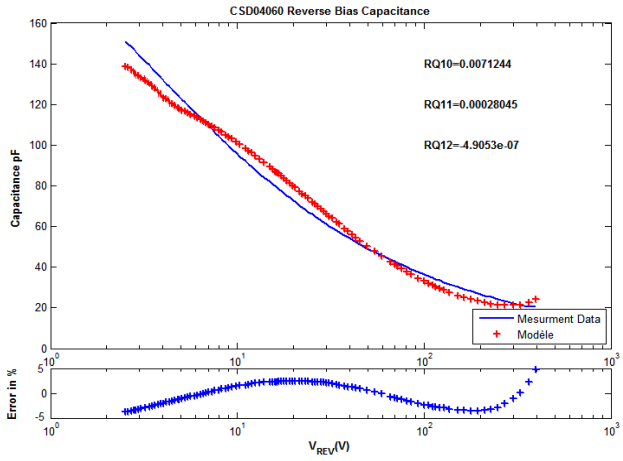

Fig. 7 Measured and simulated reverse recovery charge characteristics of the CSD04060 MPS SiC diode

The SiC MPS diode's (CSD04060) simulation of the dynamic behavior shown in Figs. 8 and 9 shows that the elimination of the stored charge starts when the voltage becomes negative. However; the final verification of the dynamic model has yet to be carried out in a cell of a switching power converter.

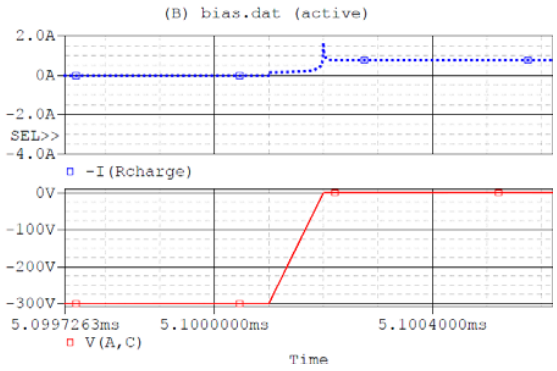

Fig. 8 Simulated dynamic behavior of the C3D04060 diode (turn-on)

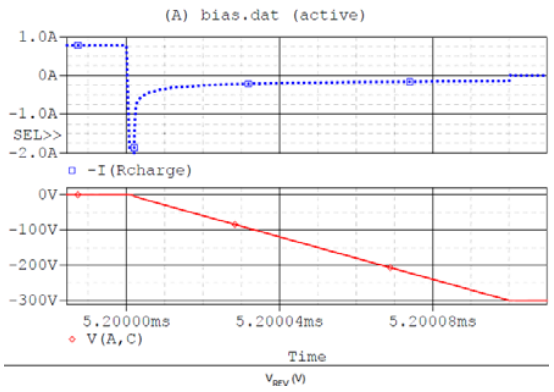

Fig. 9 Simulated dynamic behavior of the C3D04060 diode (turn-off)

IV. Conclusion

The proposed SiC MPS diodes behavioral electro-thermal model demonstrates excellent correspondence between the simulated forward and reverse bias and the curves provided by the devices' manufacturers. The estimation process of parameters which is based on two methods (i.e. weighted least square (WLS) and simulated annealing (SA)) has yielded satisfactory results. The basic advantage of the proposed model lies in its immanent simplicity and flexibility as to be implemented in modern simulators, adopting Spice programming (such as Berkeley SPICE, PSPICE).

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