Dynamic Power Reduction in Sequential Circuits Using Look Ahead Clock Gating Technique

R. Manjith, C. Muthukumari

Abstract—In this paper, a novel Linear Feedback Shift Register (LFSR) with Look Ahead Clock Gating (LACG) technique is presented to reduce the power consumption in modern processors and System-on-Chip. Clock gating is a predominant technique used to reduce unwanted switching of clock signals. Several clock gating techniques to reduce the dynamic power have been developed, of which LACG is predominant. LACG computes the clock enabling signals of each flip-flop (FF) one cycle ahead of time, based on the present cycle data of the flip-flops on which it depends. It overcomes the timing problems in the existing clock gating methods like data-driven clock gating and Auto-Gated flip-flops (AGFF) by allotting a full clock cycle for the determination of the clock enabling signals. Further to reduce the power consumption in LACG technique, FFs can be grouped so that they share a common clock enabling signal. Simulation results show that the novel grouped LFSR with LACG achieves 15.03% power savings than conventional LFSR with LACG and 44.87% than data-driven clock gating.

Keywords—AGFF, data-driven, LACG, LFSR.

I. INTRODUCTION

THE sequential circuits in a system are considered major contributors to the dynamic power consumption since one input of sequential circuits is the clock, which is the only signal that switches all the time. In addition, the clock signal tends to be highly loaded [1]. One of the major dynamic power consumers in computing and consumer electronics products is the system's clock signal, which is responsible for 30% - 70% of the total dynamic power consumption [2]. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal, regardless of whether or not they will toggle in the next cycle. With clock gating, the clock signals ANDed with explicitly predefined enable signals [3], [4]. Clock gating is employed at all levels like system architecture, block design, logic design, and gates [5].

LFSR is a sequential circuit commonly used in Built In Self Test (BIST), Signature analysis and in Spread spectrum communications. In the applications like pseudo-random bit generators (PRBGs), linear feedback shift register is used to produce a random sequence. A good PRBG must be characterized by repeatability (i.e. giving the same output sequence when the same seed is used) and randomness (i.e., passing the most common standard tests and giving good statistical properties) [6]. Today, hardware implementation of the PRBGs is almost always made up of the well-known

linear-feedback shift register whose generic circuit is reported in Fig. 1. This circuit is very simple to be implemented, but since the clock-path of all flip-flops (FFs) toggle at every clock cycle, they consume a significant amount of power. This problem was extensively addressed in [7]. The scheme based on gated clock design for LFSR is proposed in [6]. This design achieves better power result but due to hardware overhead involved this may not work for large applications.

Different clock gating techniques have been used to minimize the clock power consumption, as it is the main source of chip power consumption. Deactivating the clock signal leads to reduced power consumptions of both its internal nodes and clock lines, but the overhead involved limits its use in low data switching situations. The main purpose of this project is to reduce the clock gated flip-flop overhead and make it applicable to data signals with higher switching activity.

In conventional synchronous designs, all one-bit FFs are considered as independent components. In the recent years, as the technology advances the minimum size of the clock drivers can trigger more than one FF. As a result, grouping 1-bit FFs can reduce the total clock dynamic power consumption. FFs are grouped to reduce the hardware overhead so that clock enabling signal is shared between them. It is done by adding the enabling signals of the individual FFs [3] using OR gate. Finding the optimal grouping is the key for maximizing the power savings. To make LACG a more successful one, flip-flops are grouped which makes better power reduction.

II. LINEAR FEEDBACK SHIFT REGISTER

LFSR is a well-known circuit for pseudo-random number generation, which consists of N registers connected together as a shift register. The input to the LFSR comes from the XOR of particular bits of the register. On reset, the registers must be initialized to a non-zero value (e.g. all 1's). At each clock tick, the feedback function is evaluated using the input from tapped bits. The result is shifted into the leftmost bit of the register and the rightmost bit is shifted into the output [8].

The LFSR is an example of maximal length shift register because its output sequences through all 2^N-1 combinations (excluding all 0's) which is shown in Fig. 1. The inputs fed to the XOR are called the tap sequence and are often specified with a characteristic polynomial. For example, 4 – bit LFSR has characteristic polynomial $1+x^3+x^4$ because the taps come after the 3rd and 4th registers. LFSR sequences have been widely used in many important applications, such as wireless communications, bit error rate measurements, radar, error-

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correcting codes, and stream ciphers. There are two main advantages for using linear feedback shift register sequences: they are extremely fast and easy to implement both in hardware and software, and they can be readily analyzed using algebraic techniques [9].
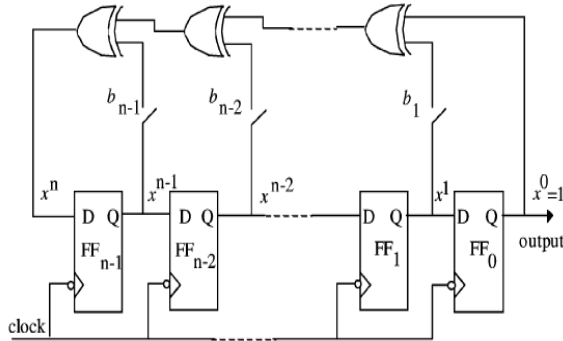

Fig. 1 Schematic of N-bit traditional LFSR

III. COMMON CLOCK GATING METHODS

When the FF input is not toggling, then effectively shutting off the clock to that FF for particular instant of time and reduce dynamic power consumption. Clock gating is very useful for reducing the power consumed by the sequential circuits. Some commonly used clock gating techniques are described below,

A. Synthesis Based Clock Gating
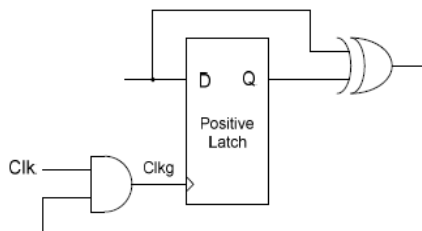
Gated positive latch is shown in Fig. 2.

Fig. 2 Clock gated positive latch

The comparison between input D and output Q is done by an XOR gate which feeds the AND gate to produce the required gated clock signal (Clkg) for the latch. When both D and Q are the same, the gated clock signal will remain low and will not consume power for switching [9]. When they differ, the gated clock signal will copy the original clock and may make a necessary transition to change the state of the latch. The same technique can be used for gated negative latch by using XNOR gate and OR gate.

Advantages

The gated flip-flop is implemented by cascading two clock-gated latches in a master-slave configuration and this design overcomes the timing constraints.

The power consumption of the presented circuit is lower when the D input has a reduced switching activity.

Disadvantages

The design needs two gating overhead circuits for each flip-flop. This double overhead limits the use of flip-flop on data signals with low switching activity.

B. Data Driven Clock Gating

A Flip-Flop finds out that its clock can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next cycle. The data-driven clock gating is shown in Fig. 3. The outputs of k XOR gates are ORed to generate a joint gating signal for k FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools and is called integrated clock gate (ICG) [10]. Such data-driven gating is used for a digital filter in an ultralow-power design. A single ICG is amortized over k FFs. There is a clear tradeoff between the number of saved (disabled) clock pulses and the hardware overhead. With an increase in k, the hardware overhead decreases but so does the probability of disabling, obtained by ORing the k enable signals.
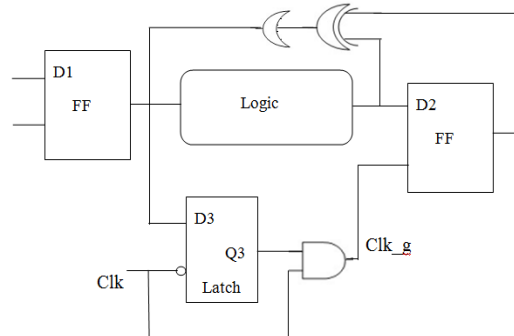

Fig. 3 Data driven clock gating

Advantages

Data-driven gating aims to disable large amount of redundant clock pulses. To reduce the hardware overhead, flip-flops are grouped so that they share a common clock enabling signal [3].

Disadvantages

Data-driven gating suffers from a very short time-window where the gating circuitry can properly work. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the FF.

C. Auto-Gated Flip-Flops

The basic circuit used for Auto-Gated Flip-Flip (AGFF) illustrated in Fig. 4. The FF's master D latch becomes transparent on the falling edge of the clock, where its output must stabilize no later than a setup time prior to the arrival of the clock's rising edge, when the master D latch becomes opaque and the XOR gate indicates whether or not the slave D latch should change its state [5]. If it does not, its clock pulse is stopped and otherwise it is passed. A significant power reduction was reported for register-based small circuits, such

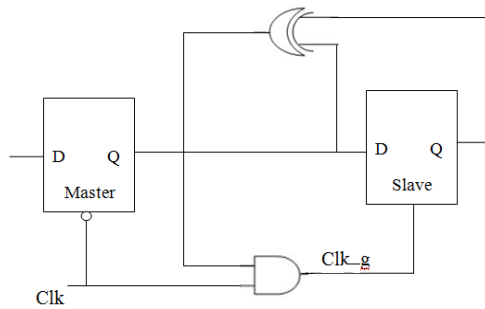as counters, where the input of each FF depends on the output of its predecessor in the register.

Fig. 4 Auto gated Flip-Flops

Advantages

Auto-Gated Flip-Flip (AGFF) method is very simple to implement and can be used for general logic by allotting a full clock cycle for the computation of the enabling signals and their propagation.

Disadvantages

AGFF has two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

IV. LOOK AHEAD CLOCK GATING TECHNIQUE

Look Ahead Clock Gating (LACG) overcomes all the disadvantages of previous clock gating technique which is shown in Fig. 5. LACG computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It avoids the tight timing constraints of AGFF and data-driven by allotting a full clock cycle for the computation of the enabling signals and their propagation [4].

LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. LACG is based on using the XOR output in to generate clock enabling signals of other FFs in the system, whose data depend on that FF.

The full clock cycle is allotted for the computation of the clock enabling signals and their propagation. The glitches occur in the previous clock gating methods like data-driven clock gating, auto gated flip-flops can be eliminated with the help of the look ahead clock gating technique.

LACG is independent of the knowledge of the flip-flops data toggling vectors and it is capable of stopping the majority of redundant clock pulses. The LACG logic can be easily derived from the underlying RTL functional code as it significantly simplifies the gating implementation.

The gating logic of the sequential circuit can be further reduced by matching target FFs for joint clock gating; this will reduce the extra hardware involved. Here, the power dissipation is reduced by deactivating (disabling) the clock signal on both master and slave latches when there are no data transitions.
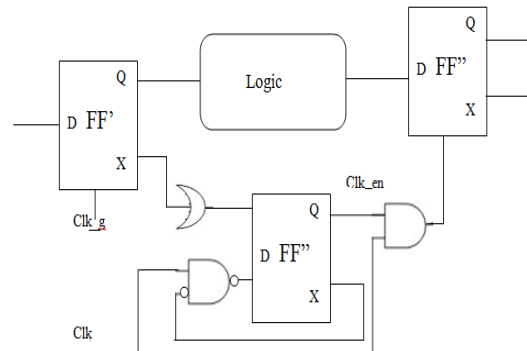

Fig. 5 Look Ahead Clock Gating Technique

V. PROPOSED LFSR WITH LACG TECHNIQUE

Clock signal is a great source of power consumption because of high frequency and load. Clock signal is not carrying any information. Gating the clocks can lead to save the power by reducing unnecessary clock. AND gate is hardly used to gate a clock that is active on the rising edge.

LFSR is the most used topology to implement PRBG. It is obtained with an array of FFs with a linear feedback performed by several XOR gates. This project presents the look ahead gated clock design approach for LFSRs [11],[12] which can lead to power reduction without unduly complicating the traditionally simple topology.

To show LACG technique in the LFSR without FF grouping (conventional LFSR with LACG) is best, the comparison is made between LFSR with data-driven clock gating and LFSR with LACG technique. The power values are also compared to the conventional LFSR. In data-driven clock gating there exist a serious timing problem for large applications but in LACG technique, the timing problem doesn't exist because of the full clock cycle allocation to determine the clock enable signal.

The schematic of the conventional 16-bit LFSR with LACG technique is shown in Fig. 6. The proposed technique consists of two inputs namely enable and reset. The input to the LFSR is denoted as D[n] and the output is denoted as Q[n]. The clock input is given to the integrated clock gating cell and the gated clock is given to the clock input of all flip-flops. The enable signal is given to the AND input which is then given as input to the D-latch.

In normal D flip-flop, the output Q reflects back the input D. The basic D – Flip flop works based on the clock. When the clock signal is enabled, the input of the D flip-flop is given to the output. Due to this reason even for the same value of input, the clock signal is repeatedly doing its function, thus makes more consumption of dynamic power.

In LACG technique, the comparison between input D and output Q is done by an XOR gate which feeds the AND gate to produce the required gated clock (GC) signal for the latch. When both D and Q are the same, the gated clock signal will remain low and will not consume power for switching. When

they differ, the gated clock signal will copy the original clock and may make a necessary transition to change the state of the latch.

LACG achieves better reduction in dynamic power by reducing the switching activity of clock signal. A normal 4-bit LFSR output say 1100, needs four clock cycles to get the four bit inputs. But in LACG technique, it needs only 2 clock cycle because it compares the adjacent bits using XOR gate. If the input and output bits are same then there is no clock signal but in case if the input and the output bits are different then the clock signal is applied to the circuit.

From Fig. 6, it can be inferred that the XOR operation is performed between 4th, 13th, 15th and 16th registers because the characteristic polynomial of 4 – bit linear feedback shift register is $1+x^4+x^{13}+x^{15}+x^{16}$. For 16–bit LFSR, the maximal length sequence is $2^{16}-1=65535$ hence this shifting operation is performed up to 65535 clock cycles and after 65535 cycles the operation restarts.

To further reduce the power consumption of the proposed LFSR with LACG technique, the FFs in the LFSR can be grouped so that common clock enable signal is shared between grouped FFs [2]. Extra logic and interconnections are needed to generate the clock enabling signals, and resulting area and power overhead must be considered. It is therefore beneficial to group FFs whose switching activities are highly correlated and derive a joint enabling signal. The optimal fan out of a clock gater yielding maximal power savings is derived based on the average toggling statistics of the individual FFs.
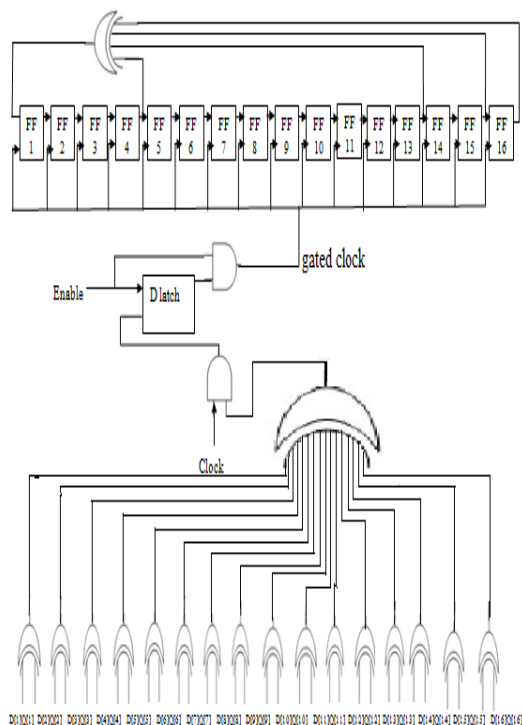

Fig. 6 Schematic of 16-bit conventional LFSR with LACG Technique

TABLE I
TRUTH TABLE FOR SINGLE D FLIP-FLOP WITH LACG

Clk	D	Q	Y (output of XOR)	GC (output of AND)
+ve	0	0	0	0
+ve	0	1	1	1
+ve	1	0	1	1
+ve	1	1	0	0

To show much better reduction of power, FFs are grouped. If we knew which flip-flops act simultaneously we could group them and a gated clock could be provided to them. Dozens of flip-flops can be grouped together and thus power can be reduced to a considerable extent. Suppose k number of clock enabling signals are grouped together, then they are provided as inputs to an OR gate. This signal is given as an input to a negative edge triggered latch and the output is obtained.

The conventional LFSR with LACG technique together with FF grouping (Grouped LFSR with LACG) achieves much better power improvement when compared to the conventional LFSR with LACG technique. The schematic diagram for the 32-bit grouped LFSR with LACG technique together with grouping size k = 8 is shown in Fig. 7.

From Fig. 7 it is inferred that for 32-bit grouped LFSR with LACG technique and with grouping size k=8, the XOR output of eight 1-bit FFs are grouped and the LACG technique is applied to all those FFs. In 32-bit LFSR with LACG technique and without FF grouping, there exists only one gated clock (gc) signal but with FF grouping there are four gated clock signals namely gc1, gc2, gc3 and gc4 as shown in Fig. 7.

VI. SIMULATION RESULTS

A novel Linear Feedback Shift Register (LFSR) with Look – Ahead Clock Gating (LACG) is designed to reduce the dynamic power consumption. The simulation results and the power consumption values for the proposed technique are achieved using the simulation tool called CADENCE. A CADENCE design system is Electronic Design Automation (EDA) software which produces software and hardware for designing integrated circuits, System-On Chip (SOC) and printed circuit boards [13].
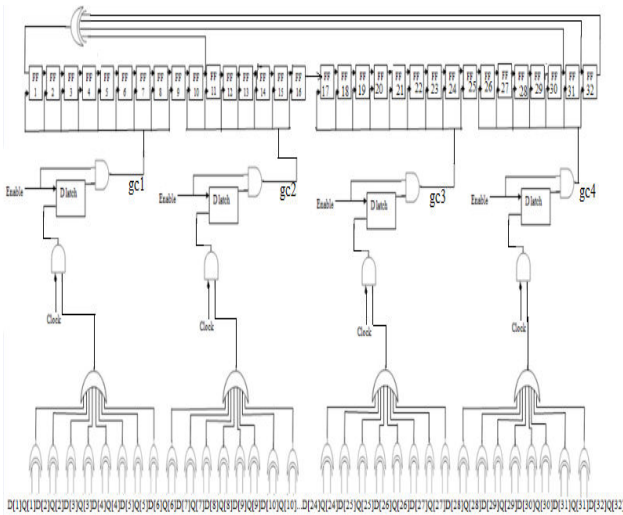
Fig. 7 Schematic of 32-bit grouped LFSR with LACG technique with grouping size k = 8

The LACG technique is initially applied to single D flip-flop and the better power reduction is achieved. Then, the LACG technique is further applied to 4-bit, 8-bit, 16-bit, 32-bit and 64-bit LFSR. The power consumption values for the various bits of conventional LFSR's with LACG are compared with the LFSR without clock gating and LFSR with the data-driven clock gating technique to show better power savings. The simulation results for the above different bits of LFSR with different combination of FF grouping (i.e grouping size k = 4, 8, 16, 32) is also discussed to show further power reduction in the LFSR with LACG technique. The Simulation result for the conventional 4-bit LFSR with LACG is given in Fig. 8.
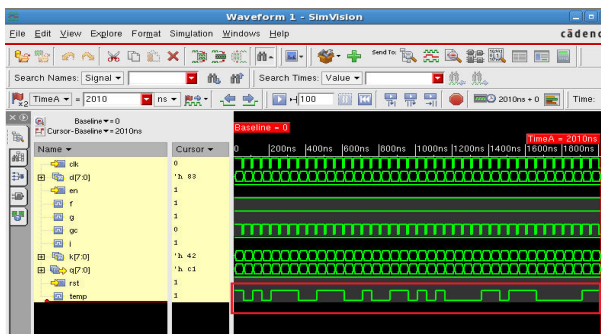

Fig. 8 Simulation result for 4-bit LFSR with LACG

The input and output to the LFSR is denoted as d [3:0] and q [3:0]. The other two inputs given to the LFSR are clock and reset signal which is denoted as clk and en. K [3:0] represents the output of XORs which is used for comparing the input and the output. The output of OR is denoted as g, which is used to group the output of all XORs. The output from the ICG cell together with the AND gate is denoted as gc, which is the gated clock signal. The term temp is used to denote the switching activity of clock which is very low compared to the ordinary clock signal. It indicates that after applying LACG technique, the activity of clock signal gets reduced thus achieving reduction of dynamic power. Similarly, the simulation results for the conventional 8-bit, 16-bit, 32-bit and 64-bit LFSR with LACG is shown in Figs. 9-12. The power consumption values for conventional LFSR, LFSR with data-driven clock gating and LFSR with LACG technique for different bits is shown in Table II.
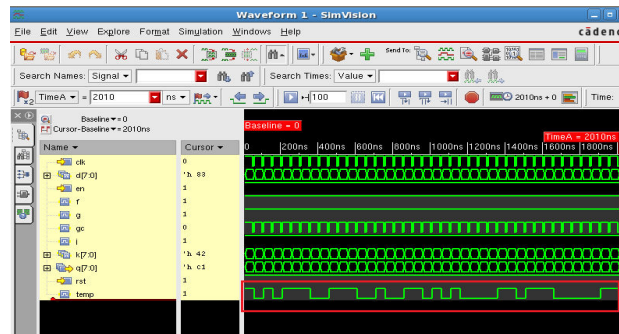

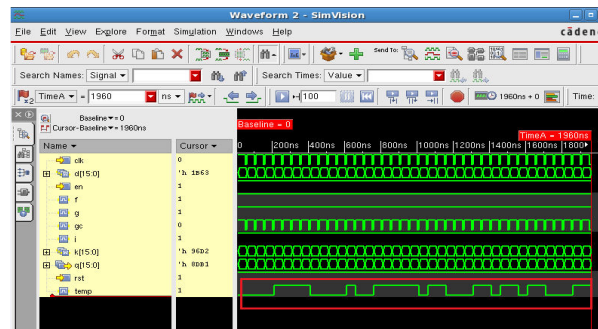Fig. 9 Simulation result for 8-bit LFSR with LACG

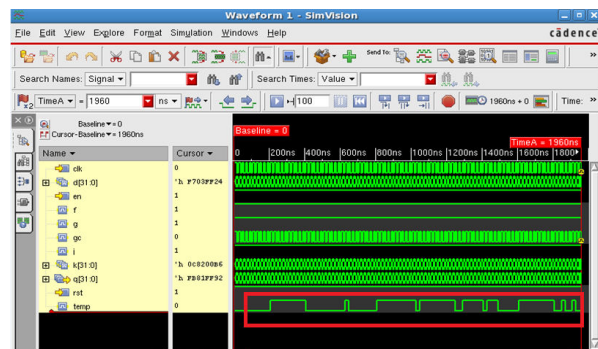Fig. 10 Simulation result for 16-bit LFSR with LACG

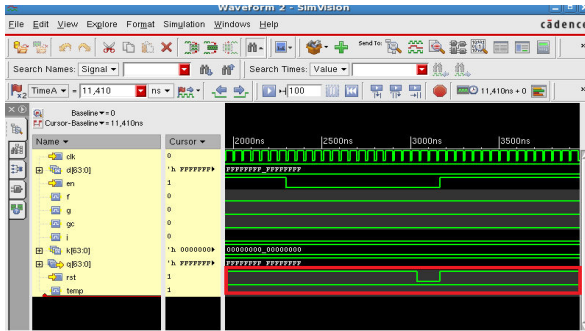Fig. 11 Simulation result for 32-bit LFSR with LACG

Fig. 12 Simulation result for 64-bit LFSR with LACG

TABLE II
COMPARISON OF POWER CONSUMPTION VALUES OF VARIOUS LFSR WITH DIFFERENT CLOCK GATING TECHNIQUES

No. of. Bits	LFSR Without Any Clock Gating	LFSR with Data Driven Clock Gating	Conventional LFSR with LACG	Power Savings (%)
1	6581.85nW	8253.161nW	5958.673nW	27.8
4	30109.909nW	43516.238nW	25120.25nW	42.21
8	69645.476nW	84701.377nW	56589.673nW	33.19
16	128452.666nW	163685.692nW	104681.463nW	36.05
32	257788.967nW	343043.317nW	205150.688nW	40.19
64	508663.435nW	507418.725nW	348694.379nW	31.28

From Table II, the first column represents the LFSR without any clock gating technique. For 64-bit LFSR, the proposed LFSR with LACG technique achieves 31.45% when compared to the LFSR without any clock gating technique. Hence it is proved that the proposed technique achieves power reduction on an average of 35.12% for different bits when compared to the LFSR without any clock gating technique. From Table II, it is also observed that when compared to 1-bit FF with data-driven clock gating the proposed 1-bit FF with LACG technique achieves power savings on an average of 27.8%. Similarly, when compared to 4-bit LFSR with data-driven clock gating the proposed LACG technique achieves power savings of 42.21%. For 8-bit LFSR, proposed LACG technique achieves power savings on an average of 33.19%. For 16-bit LFSR, power savings of 36.05% is achieved using LACG technique. For 32-bit LFSR, power savings of 40.19% is achieved using LACG technique. Similarly, for 64-bit LFSR power savings of 31.28% is achieved for the proposed LFSR with LACG technique.

The power comparison values for the different bits of conventional LFSR with LACG, LFSR without LACG and LFSR with data-driven clock gating using CADENCE is shown in Fig. 13.

From Fig. 13, it is clear that the proposed conventional LFSR with LACG achieves better power reduction compared to the LFSR without clock gating and LFSR with data-driven clock gating. The power consumption of traditional 64-bit LFSR is about 508663.435nW and the power consumption of 64-bit LFSR with data-driven clock gating is about 507418.725nW. Using LACG technique the power consumption has reduced to 348694.379nW. It is also clear from Fig. 12 that, the LFSR with data-driven clock gating has increased power consumption compared to LFSR without clock gating because the data-driven clock gating achieves reduced power consumption only when FFs are grouped. But LFSR with LACG technique achieves power savings even when FFs are not grouped.
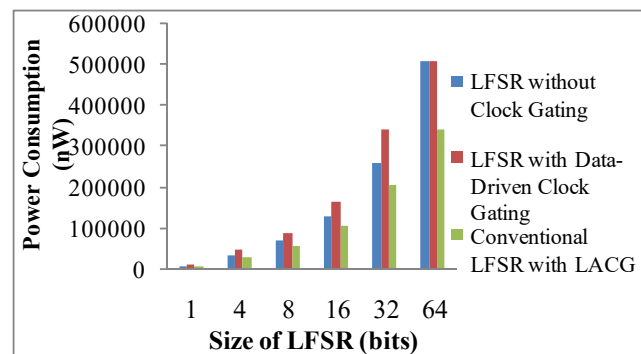

Fig. 13 Power comparison for LFSR

The power consumption values for 4-bit, 8-bit, 16-bit, 32-bit and 64-bit grouped LFSR with LACG technique with different grouping size (k = 4, 8, 16 and 32) are shown in Table III.

From Table III, it is clear that when FFs are grouped with different grouping size (i.e. k = 4, 8, 16, 32) the proposed LFSR with LACG technique achieves much reduction in power consumption compared to the proposed technique without FF grouping. The term – in Table III represent there is no need for FF grouping for small sized bits like 1-bit, 4-bit.

TABLE III
COMPARISON OF POWER CONSUMPTION VALUES OF VARIOUS LFSR WITH DIFFERENT FF GROUPINGS

No. of bits	Conventional LFSR with LACG	Grouped LFSR with LACG			
		K=4 (nW)	K=8 (nW)	K=16 (nW)	K=32 (nW)
1	5958.673nW	-	-	-	-
4	25120.25nW	-	-	-	-
8	56589.673nW	54550.544	-	-	-
16	104681.463nW	74804.259	88521.548	-	-
32	205150.688nW	179838.867	186404.384	201675.083	-
64	348694.379nW	294235.024	301324.36	333459.791	339557.318

In 8-bit grouped LFSR with LACG technique, 3.6% power savings is achieved with grouping size k = 4 compared to the FF without grouping. Similarly, in 16-bit grouped LFSR with LACG technique, 28.54% power savings is achieved with grouping size k = 4 and 15.44% power savings is achieved with grouping size k = 8 compared to the FF without grouping. In 32-bit grouped LFSR with LACG technique, with FF grouping sizes k = 4, 8 and 16 power reduction of 12.34%, 9.12% and 1.69% is achieved correspondingly. Finally, in 64-bit grouped LFSR with LACG technique, with FF grouping sizes k = 4, 8, 16 and 32 power reduction of 15.62%, 13.58%, 4.37% and 2.62% is achieved correspondingly.
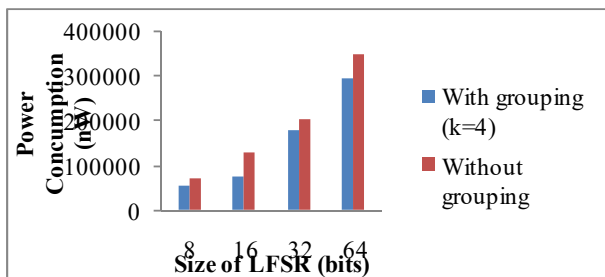

Fig. 14 Power comparison for LFSR with FF grouping

The grouped LFSR with LACG technique achieves much better power reduction when compared to the conventional LFSR with LACG and LFSR with data-driven clock gating. The power consumption values for FF grouping with different combination of bits in the LFSR with LACG technique and the power consumption values for FF without grouping in LFSR with LACG technique are compared in Fig. 14. From Fig. 14, it is proved that in the proposed LFSR with LACG technique FF clustering yields increased power savings when compared to the proposed technique without any grouping. Since FFs are merged, the number of clock cycle gets reduced hence the power consumption of clock signal gets reduced.

VII. CONCLUSION

The simulation results clearly show that the proposed design has much less clock dynamic power consumption compared to the LFSR without clock gating technique and the data-driven clock gating technique. The dynamic power values for the 4-bit, 8-bit, 16-bit, 32-bit and 64-bit conventional LFSR with LACG is simulated using CADENCE. The proposed LFSR with LACG technique achieves much better power reduction when FFs are grouped which is based on their toggling probability. The novel grouped LFSR with LACG technique achieves power reduction on an average of 15.03% with different grouping size (k = 4, 8, 16, 32) compared to the conventional LFSR with LACG technique and it attains power savings of 44.84% when compared to the LFSR with data-driven clock gating. The novel grouped LFSR with LACG will be very effective for the applications like Built-In Self Test

(BIST), cryptography and in spread spectrum communication system.

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