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Novel Approach to Design of a Class-EJ Power Amplifier Using High Power Technology

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***Abstract*—**This article proposes a new method for application in communication circuit systems that increase efficiency, PAE, output power and gain in the circuit. The proposed method is based on a combination of switching class-E and class-J and has been termed class-EJ. This method was investigated using both theory and simulation to confirm ~72% PAE and output power of >39dBm. The combination and design of the proposed power amplifier accrues gain of over 15dB in the 2.9 to 3.5GHz frequency bandwidth. This circuit was designed using MOSFET and high power transistors. The load- and source-pull method achieved the best input and output networks using lumped elements. The proposed technique was investigated for fundamental and second harmonics having desirable amplitudes for the output signal.

***Keywords*—**Power Amplifier (PA), GaN HEMT, Class-J and Class-E, High Efficiency.

I. Introduction

MODERN wireless communication systems have experienced ongoing evolution that employs complex modulation designs that increase information on the high efficiency broadband bandwidth and desirable data rates [1]. The high demand of consumers for smart phones that are cost-effective and preserve battery power has increased progress in broadband bandwidth of systems with lumped elements at radio frequency. Power amplifiers for different classes were investigated using power-consuming components for RF wireless communications and TV transmission [2], [3].

Power amplifiers are usually the last stage of transmitter configuration and are important components of RF circuits. The efficiency, output power and bandwidth of the power amplifier directly affect the components of the system. High power efficiency decreases DC power consumption and dissipates heat which significantly affects the total power consumed, stability, DC power supply and cooling systems. Systems used in modern generation of wireless communication systems handle worldwide mutual communication for microwave access and modulated signals with broadband bandwidth. This means that the design of a broadband amplifier is most important for such systems [1].

Wireless communication systems require high power linear amplifiers to send a signal with minimum phase and amplitude distortion to a receiver. A useful design method is one that improves efficiency and output power simultaneously using single or mixed classes of power amplifier. Most power amplifiers are based on the configurations and performance of such classes, which are classified as A, B, C, AB, D, F, F^{-1}, S, E, J, etc. [5], [6].

The present study selected class-J and class-E to achieve higher efficiency and output power. Class-J has linear properties, because it is designed for the bias point of class-AB or class-B. F. Rahmani [6] and V Carruba [7] investigated mixed class-ABJ. The proposed class-EJ method improves the efficiency and output power at higher frequencies than those of class-ABJ.

II. High Power GaN CGH40010F Transistor

The GaN CGH40010F transistor model was selected for design of the proposed circuit because it has the unique ability for high electron mobility in GaN transistors. This type of transistor was analyzed for a 28V supply that represents general purpose broadband for various RF and microwave applications. GaN HEMT transistors provide higher efficiency and gain with more bandwidth than other transistors. The CGH40010F transistor is made for linear circuits with compact dimensions. Comparisons were carried out between the different substrates of the power amplifier.

TABLE I
The Comparison between Different Substrates for Selecting the Best Transistor [8]

	Parameter	Dimension	Comparison
1	Saturated Velocity ($\times 10^7$)	"cm/s"	Si[1.08]<GaAs[1.3]<GaN[2.7]
2	High Electron Mobility ($\times 10^3$)	"cm^2/V/s"	Si[1.5]<GaN[3]<GaAs[6]
3	Breakdown E Field	"MV/cm"	GaAs[0.4]<Si[0.5]< GaN[3]
4	Band Gap Energy	"eV"	Si[1.13]<GaAs[1.4]<GaN[3.4]
5	Output power density	"W/mm"	Si[0.8]<GaAs[1.5]<GaN[7]

Table I [8] shows that the GaN substrate is best for design of high power circuits, which makes it a perfect choice for design of class-EJ. Fig. 1 shows the bias point at I_{DS} = 0.5A and V_{DS}= 28V for the GaN transistor in ADS (Advanced Design System) software. The proposed circuit was designed for a 3.2 GHz central frequency. To determine the central frequency of the class-EJ circuit, as shown in Table II, the stability factors must always be StabFact >1 and StabMeas>0.

TABLE II
Analysis of the Stability Factors

Frequency	StabFact	StabMeas
3.2 GHz	1.032	1.506

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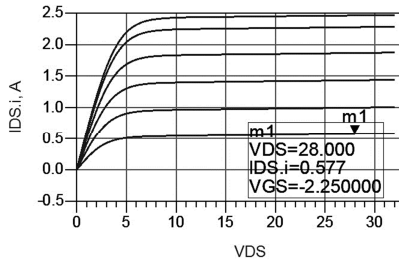

Fig. 1 Definition the bias point of the GaN transistor

Table III shows that the results of analysis of the S-parameter for the selected transistors was S(2,1) > S(1,2). This transistor has desirable parameters. Tables I and II show that the selected transistor is stable and has desirable stability factors for small signal analysis.

TABLE III
S-PARAMETERS ANALYSIS AT THE 3.2GHZ FREQUENCY

$S(1,1) = 0.9\angle 152.801^\circ$	$S(1,2) = 0.018\angle -23.556^\circ$
$S(2,1) = 3.18\angle 29.701^\circ$	$S(2,2) = 0.434\angle -171.179^\circ$

Fig. 2 shows the stability of the transistor based on source and load stability circles. If the source and load lines fall outside the Smith chart, the transistor will be stable. If the Smith chart includes these lines, the transistor will be unstable. The transistor in Fig. 2 is unstable at 1 to 3.2 GHz and is stable at 3.2 to 8 GHz. This indicates that the central frequency was selected properly, because of lines fall outside the Smith chart.

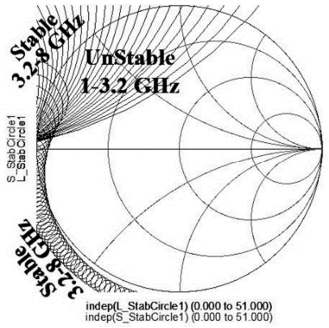

Fig. 2 Display stability of the transistor according to the load and source stability circles

III. DESIGN OF CLASS-EJ

A. Class-EJ Power Amplifier

Class-E is a switching class. The results of simulation show analog waveforms that can approximately support a device with fewer switching characteristics in a linear region. Class-E decreases the conduction angle to deliver higher efficiency without a complex circuit, such as an advanced class-F design. One advantage of a switching mode power amplifier such as class-E is its high performance on a low bias voltage supply. This class decreases power dissipation over other switching mode power amplifiers at similar frequencies. Class-E is designed to provide a circuit with smaller dimensions [4].

The basic theory of class-J is an ideal waveform formed by controlled termination of fundamental impedance and harmonic impedances. Cripps [9] stated that class-J is a short circuit up to termination of the third harmonic impedance; this class has its own bandwidth and the output capacitor can be used as a short circuit in upper harmonics and also remain fundamental and second harmonics. The output matching network in the fundamental harmonic is slightly inductive and in the second harmonic is capacitive. The output stage of the class-EJ power amplifier uses class-J, because class-J is more efficient than class-E in the first stage. Fundamental and second harmonic impedances in class-J is a complex number with real and imaginary parts, such as $\alpha+j\beta$.

To improve the performance of the proposed circuit and obtain maximum efficiency, output power and gain, class-E and class-J were merged to produce the proposed design of class-EJ. This new class was designed with class-E and class-J having less input power and greater output power. The main purpose of the two-stage power amplifier is to increase gain and decrease input power (P_{in}) in the circuit.

B. Bias Circuit

The bias circuit was designed using a MOSFET transistor in the output and input class-EJ circuit. The bias circuit increases the input voltage on the gate of the GaN transistor. Fig. 3 shows that the gate voltage was 6.8 V with bias circuit but for a class-EJ without a bias circuit, the gate voltage decreased to 5.5 V and the gate current was 0.62 A.

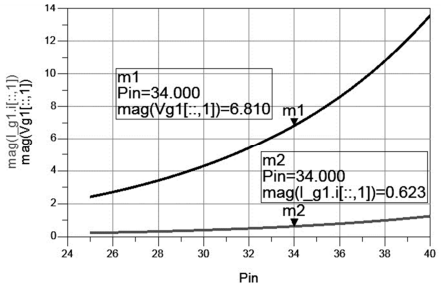

Fig. 3 Current and voltage of gate diagrams of the transistor for class-EJ

Fig. 4 indicates that the input bias circuit increased the gate supply voltage in the first stage of the class-EJ power amplifier. Fig. 5 shows that the output bias circuit in the second stage consisted of a 20nH choke inductor. One choke inductor was used in the output bias circuit to decrease DC power in the drain of the GaN transistor. The 1 Ω internal resistance from the circuit was an ideal form and approached a real circuit. Each stage of the class-EJ power amplifier consisted of two bias circuits at the gate and drain of the transistors. Two of the four bias circuits require explanation in this study.

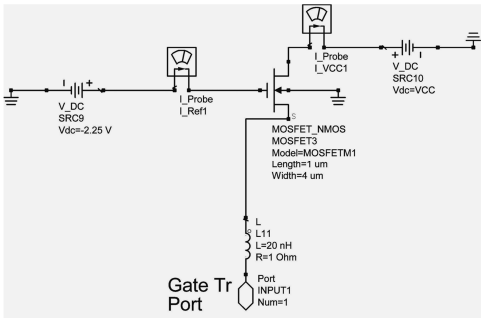

Fig. 4 The proposed input bias circuit of class-E which is first stage of class-EJ power amplifier

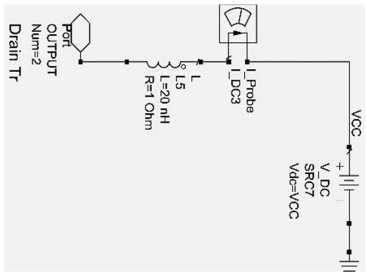

Fig. 5 The proposed output bias circuit of class-J which is second stage of class-EJ power amplifier

C. Input and Output Matching Circuit

Load- and source-pull techniques are the best methods to determine input and output matching circuits and obtain optimum impedance of the input and output of the power amplifier. The power-added-efficiency (PAE) and power delivered to the load was obtained by harmonic balance analysis considering the $50\,\Omega$ output resistance. Matching circuit was done with lumped elements based on the configuration of two classes of power amplifier. Table IV shows the optimum impedance for the input and output of the first and second stages of the class-EJ power amplifier and the values for output power and PAE from the simulation results for the load- and source-pull methods.

TABLE IV
OPTIMUM INPUT AND OUTPUT IMPEDANCE USING LOAD- AND SOURCE-PULL TECHNIQUE

Class	Z_{In}	Z_{Out}	P_{out} (dBm)	PAE
Class-E	8.64+j36.09	-	39.79	51.49%
	-	10.99+j5.71	40.05	52.12%
Class-J	9.60-j1.33	-	40.33	47.84%
	-	14.08+j7.01	39.42	47.55%

After obtaining the optimum impedances for the input and output of the two-stage class-EJ power amplifier, the best circuits with the smallest dimensions were designed using the Smith chart and the lumped elements were determined based on the configurations of class-E and class-J. The following points must be considered for the design of the class-EJ circuit:

1. As shown in Fig. 6, input resistance (R_1) is considered as far as possible small in the input matching circuit of the first stage, because it plays a major role in determining efficiency.
2. As shown in Fig. 7, a series inductor (L_{15}) is required at the beginning of the output matching design to create the highest harmonic impedance for design of first stage output matching for the class-EJ power amplifier.
3. Fig. 7 also shows that the parallel capacitor must be placed at the end of the second stage (class-J) because the impedance of the capacitor (C_6), inductor (L_1) and resistor (R_4) are calculated in parallel with C_4, decreasing input impedance and input power.

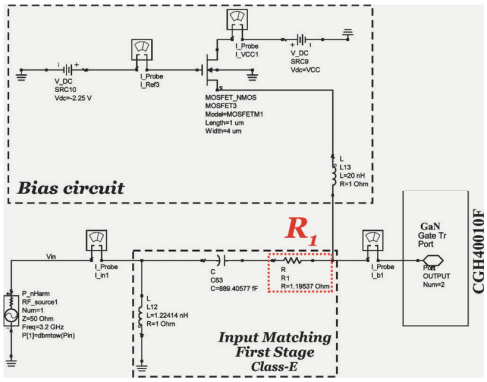

Fig. 6 The input first stage class-EJ power amplifier

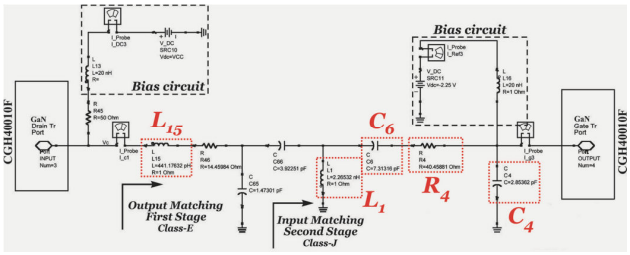

Fig. 7 The output first stage and the input second stage of the class-EJ

4. Fig. 8 indicates that there is a parallel capacitor (C_3) in output class-J causing impedance to short-circuit at higher frequencies. According to the equation $Z = \frac{1}{jC_3 \times 2\pi f}$, the upper second harmonics becomes ineffective. It is important to determine the output capacitor in the class-J of the class-EJ power amplifier. The ratio of capacitive reactance to load resistance should be equal to or less than unity. In this paper, (1) and $R_L = 50\,\Omega$ make the ratio:

$$\frac{X_{C_{ds}}}{R_L} = 0.62 \rightarrow 0.62 \langle 1 \qquad (1)$$

5. In Fig. 8, efficiency increased and DC power decreased by resistance (R_2) in the output bias of the second stage class-EJ, because there was a loss in the series resistor that decreased the DC supply voltage and increased efficiency.

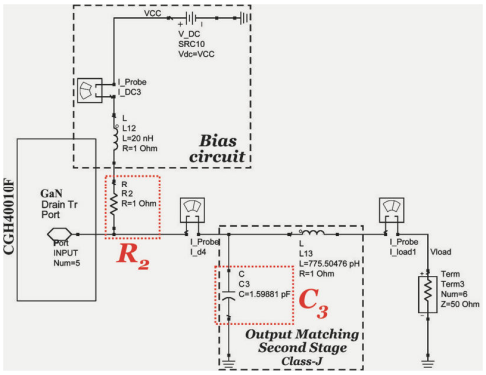

Fig. 8 The output second stage class-EJ power amplifier

After finding the knee voltage and according to the following equations, load impedance was calculated for the first and second harmonics. In these equations, $V_k = 5.6$ V and $I_{max} = 0.933$ A.

$$Z_{F_1} = R_{opt} + jR_{opt} = 48.01 + j\ 48.01 \quad (2)$$

$$Z_{F_2} = -j\frac{3\pi}{8}R_{opt} = -j\ 56.5 \quad (3)$$

$$R_{opt} = \frac{2\times(V_{DC} - V_k)}{I_{max}} = 48.01\ \Omega \quad (4)$$

IV. Simulation Results for Class-EJ

A. Simulation Results

When calculating the PAE, all the DC current of the circuit and drain efficiency is the supposed output DC current. The simulation results are listed in Table V and show the results obtained from the proposed class-EJ power amplifier. The goal of the proposed PA is to decrease the input power to obtain maximum PAE, efficiency and output power. The desired results were achieved using the proposed two-stage PA circuit and by increasing the gain of the proposed circuit.

TABLE V
Comparison of Simulation Results between the First Stage, Second Stage and Final Circuit

Parameter	First Stage (Class-E)	Second Stage (Class-J)	Class-*EJ*
P_{in} *(dBm)*	34	28	20
PAE *(%)*	74.8	77.9	80.8
P_{out} *(dBm)*	40.55	39.86	38.2
Gain *(dB)*	6.55	11.86	17.24

The best results for the proposed power amplifier obtained the highest output power, drain efficiency and PAE for high power technologies with the lowest input power. Table V indicates that the class-EJ increased PAE and gain but decreased output power. Table VI compares the simulation results for the class-EJ power amplifier and done previous works and indicates that the proposed circuit is performed better than the other works.

TABLE VI
Comparison of Simulation Results between the Class-EJ Power Amplifiers with Done Previous Works

Class	Frequency	Technology	Voltage Supply	Efficiency	Year[Ref]
E	2GHz	GaN HEMT	50V	74.4%	2007[10]
E	2.14GHz	GaN HEMT	40V	74%	2009[10]
J	2.14GHz	GaN HEMT	30V	77.3%	2010[10]
J	1.15GHz	CGH40010	31V	50-69%	2012[11]
J	2.3GHz	CGH40010F	28V	60-75%	2013[5]
E	3.2GHz	CGH40010F	28V	84.3%	This Work
J	3.2GHz	CGH40010F	28V	85.9%	This Work
EJ	3.2GHz	CGH40010F	28V	87.8%	This Work

B. Analysis of Simulation Results

The output parameters were analyzed and the results are investigated using the determined bandwidth. Fig. 9 shows that analysis of the first and third harmonics indicate very desirable output power at the 2.9 to 3.5GHz bandwidth. The first harmonic of the output spectrum at the fundamental frequency was 39.242dBm and the third harmonic at the same frequency was -166.748dBm. The more negative the numerical value of the harmonics becomes, the better the performance of the circuit.

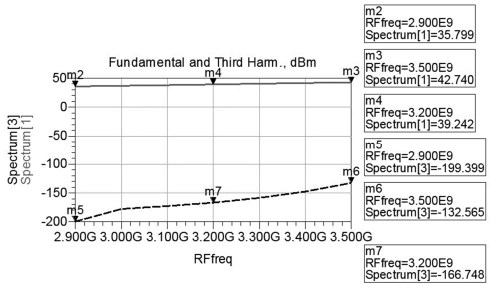

Fig. 9 Analysis of the output spectrum parameter in the fundamental and third harmonics

Fig. 10 (b) shows that the output voltage waveform is similar to the sinusoidal input voltage waveform; if the output spectrum at the higher harmonics decreases, the output waveform is similar to the sine wave. Fig. 10 (a) indicates a downtrend of the output spectrum from the fundamental harmonic to the third harmonic and shows suitable matching in the input and output of the proposed circuit.

If the output capacitor is considered to change, because it plays a major role in the design of the second stage (class-J), the values of the capacitor can be changed to a value in the range of 0.5 pF to 5pF. Fig. 11 shows the results for the gain and output power, after which the best value for the output capacitor could be specified. The best value for the output capacitor (C_3) is 1.5 pF because of the output power (P_{out} = 39.487 dBm) and gain (G_{RF} = 19.4 dB) obtained. The output circuit of class-J was designed using the load-pull method, making the value of the output capacitor equal to 1.598 pF; the accuracy of the output matching design was confirmed in this manner.

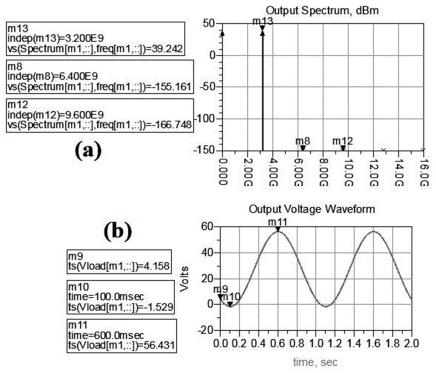

Fig. 10 (a) Output spectrum at the fundamental, second and third harmonic frequencies (b) The output voltage sinusoidal waveform

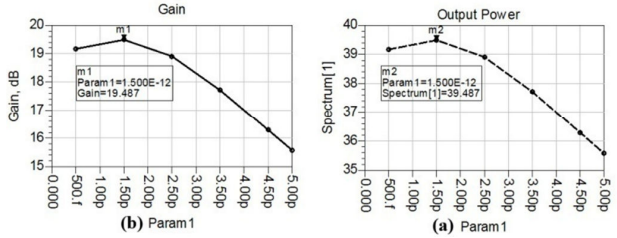

Fig. 11 (a) Output voltage parameter to variations of the output capacitor (b) Gain parameter to variations of the output capacitor

If the output power does not increase properly for the input power, the amplifier is in compression mode, so the gain compression point must be calculated to limit the level of input power that will cause nonlinear harmonic distortion. This point is usually the input power that decreases the gain (1 dB) to that of normal linear gain. Fig. 12 shows the output spectrum of the class-EJ power amplifier at the 1dB gain compression point.

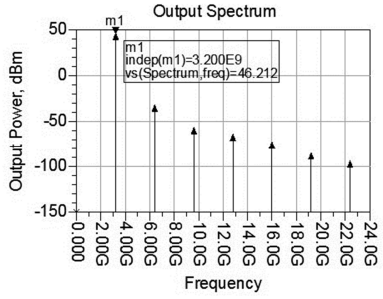

Fig. 12 Output spectrum at the 1dB gain compression point

The following graphs and equation illustrate the extraction of meaningful results from the simulation. To determine the input power leading to a gain compression point of ~1dB, a marker is placed on each trace and they are moved so that their difference approaches 1dB. The following plot shows the input and output power at about 1dB for the gain compression point.

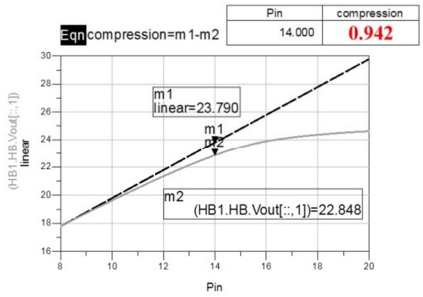

Fig. 13 Output and input power at the 1dB gain compression point

The 27.5 dBm input power must be chosen from a range of Pin = 20 to 30dBm to increase PAE to 70%. Fig. 14 and Table VII shows that output parameters such as PAE, P_gain_transducer, P_{DC}, I_{max} and P_{out} are specified based on the 0.6 GHz bandwidth in the proposed circuit.

TABLE VII
OUTPUT PARAMETERS ARE SPECIFIED BASED ON 0.6GHZ BANDWIDTH

Frequency (GHz)	Output Power (dBm)	Output Power (dBm)	Max current (A)
2.9	38.4	12.2	0.437
3.0	38.7	12.2	0.437
3.1	39.1	12.2	0.437
3.2	39.5	12.2	0.437
3.3	40.1	12.2	0.437
3.4	40.6	12.2	0.437

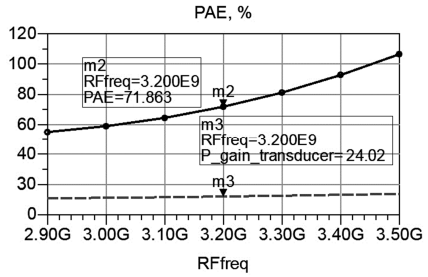

Fig. 14 PAE and P_gain_transducer at the 0.6GHz bandwidth

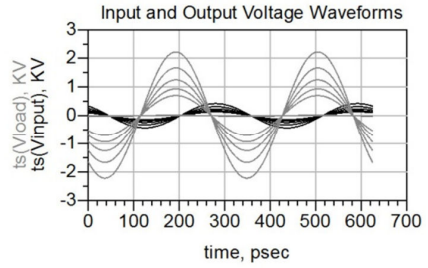

Fig. 15 The input and output voltage waveforms

Fig. 15 shows the input and output voltage waveforms and Fig. 16 shows the load current waveform of the class-EJ power amplifier. Current and voltage waveforms at the output stage of the class-EJ power amplifier should have a phase difference of 45°.

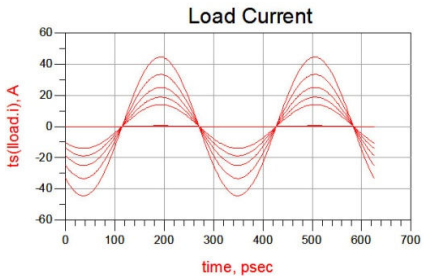

Fig. 16 The load current waveform

V. Conclusion

This study developed a new approach called the two-stage class-EJ circuit and analyzed it using ADS software. As gain increased to 17.2dB, the input power decreased 20dBm that is less than each stage. The proposed power amplifier was designed for minimum input power and maximum efficiency, so the input power of each power amplifier must have acceptable performance. The 87% efficiency and 38.2dBm output power was obtained at the 2.9 to 3.5GHz frequency range for the class-EJ power amplifier.

Matching circuit was done based on the load- and source-pull methods using lumped elements for the best input and output networks to increase drain efficiency and PAE. This new approach was evaluated using a GaN CGH40010F transistor, because GaN substrates produce high output power in the proposed circuit. This novel method was implemented using the class-E and class-J to achieve better performance than previous works. The proposed approach will be able to use different substrates of transistors and is designed by choosing classes having the greatest frequency bandwidth.

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