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Stable Delta-Sigma Modulator with Signal Dependent Forward Path Gain for Industrial Applications

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***Abstract*—**Higher order ΔΣ Modulator (DSM) is basically an unstable system. The approximate conditions for stability cannot be used for the design of a DSM for industrial applications where risk is involved. The existing second order, single stage, single bit, unity feedback gain , discrete DSM cannot be used for the normalized full range (-1 to +1) of an input signal since the DSM becomes unstable when the input signal is above ±0.55. The stability is also not guaranteed for input signals of amplitude less than ±0.55. In the present paper, the above mentioned second order DSM is modified with input signal dependent forward path gain. The proposed DSM is suitable for industrial applications where one needs the digital representation of the analog input signal, during each sampling period. The proposed DSM can operate almost for the full range of input signals (-0.95 to +0.95) without causing instability, assuming that the second integrator output should not exceed the circuit supply voltage, ±15 Volts.

***Keywords*—**DSM, stability, SNR, state variables.

I. Introduction

THE second order, single stage, discrete, single bit quantizer and unity feedback gain ΔΣ Modulator (DSM) is shown Fig. 1, and is a typical (conventional) DSM where x_{analog} is the analog input signal. The Sample and Hold (S/H) circuit samples the input signal at a sampling period which is same as the clock period of DSM circuit, T_C. The delay unit D gives a delay of one clock period and Q is the binary quantizer and the output can be +1 or -1. The conventional DSM becomes unstable when the normalized input signal is above $\pm$ 0.55. Let *x(i)* is the sampled analog input signal to the DSM circuit during the i^{th} sampling period. The average value of the output of quantizer during k^{th}, update period T_U ($T_U >> T_C$), is denoted as *y(k)*. The normalized input signal during the k^{th} update period, $x_{nor}(k)$, is the ratio of average value of input samples to the feedback gain. For a typical DSM with unity or greater than unity feedback gain, *y(k)* is equal to $x_{nor}(k)$ during the k^{th} update period [1]-[3].

Hein and Zahor [4] stated that in a typical DSM, with dc inputs satisfying $|x_{nor}|<1$, the following bounds apply.

$$|x_1(k)| \le |x_{nor}| + 2 \quad 0 \le |x_{nor}| < 1 \tag{1}$$

$$|x_2(k)| \le \frac{(5 - |x_{nor}|)^2}{8(1 - |x_{nor}|)} \quad 0 \le |x_{nor}| < 1 \tag{2}$$

From (2), as $|x_{nor}| \to 1$, $|x_2(k)| \to \infty$. The analytic bound on $|x_2(k)|$ is fairly tight for $|x_{nor}| \le 0.7$ but increases quickly as $|x_{nor}|>0.7$. If the absolute value of the normalized input exceeds 0.7, then the input to the quantizer saturates the operational amplifier, which is used as comparator, and thus the DSM becomes unstable.

Bourdopoulos G. I. proposed a method for achieving adaptive reduction in the order of the loop filter of usual high-order, single-stage, single-bit DSM in order to improve the stability range and SNR [5]. The resulting DSM recovers from instability, with extended input range when compared to the corresponding conventional DSM.

The loop stability is obtained by feed forward coefficients and feedback coefficients are added to optimize quantization noise response in base band [1], [3]. By using multiple feed forward and feedback features into second order structure, more flexibility is obtained for improving stability and improving dynamic range.

Normally used DSM structures are high order modulator with single loop and MASH structure [6]. The single loop high order DSM is likely to be unstable but can provide high SNR with relaxed circuit specifications. The input range depends on the quantizer and number of levels used in DAC.

Jiaxin Ju, Wanrong Haolin Du, Yanfeng Jiang and Yamin Zhang presented a low voltage switching capacitor DSM and focused on the implementation of unity gain and conventional DSM which could reduce the requirement of operational amplifier DC gain and was able to reduce the circuit complexity, power consumption and area. However, the SNR falls when the normalized input signal exceeds -3dB [7].

Yavari M., Shoaei O. and Rodriguez-Vazquez A. described single loop double sampling DSM topologies. To lessen the quantization noise folding effect into the signal band, a FIR NTF with an additional zero at $f_s/2$ was used [8]. Unity-gain STF (signal transfer function) was employed to decrease the modulator's sensitivity to the circuit non-idealities. The proposed fifth order structure is more sensitive to the sampling paths mismatch compared to the third and fourth order structures. This is because in fifth order structure the out-of band quantization noise is larger with a lower OSR.

In [9] is presented, a single-loop DSM with extended dynamic range. It employs an auxiliary quantizer to process the quantization error of the main quantizer. This simple

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addition guarantees improved stability over a wider signal input range and also reduces the sensitivity to the front-end DAC nonlinearity.

A low-voltage and low – power Delta Sigma modulator is presented in [10]. The modulator employs a third-order single-loop topology with feed-forward path and a single-bit quantizer. It saves power and improves SNR but the dynamic range is limited.

The key feature of the modulator which is proposed in [11] is that it makes use of the advantages of 2-2 MASH delta-sigma modulator compared to other conventional cascaded delta-sigma-pipeline modulators. This architecture offers the possibility of implementation of a power efficient, fourth-order cascaded delta-sigma-pipeline modulator without having the stability or DAC non-linearity problems but is complex in design.

In [12] is presented, the design and FPGA implementation of a 2nd order all-digital Adaptive Delta Sigma modulator with one bit quantization. The 2nd order adaptive ΔΣ modulator presented, exhibits an average SQNR improvement. It also exhibits an increased dynamic range of approximately 24 dB over the 2nd order non-adaptive ΔΣ modulator but it is complex in design.

In [13] is presented, a delta-sigma modulator which is based on a 4th-order single loop switched-capacitor architecture with a 4-bit quantizer. Due to the power and area overheads an adder-less input-feed forward delta-sigma architecture is used. As a result, the designed architecture eliminates the extra power consumption and silicon area required by the adder. The modulator achieves a dynamic range of 76 dB and a peak signal-to-noise plus- distortion ratio of 72.3 dB in a signal bandwidth of 6 MHz. In the proposed DSM, the dynamic input range of positive SNR is 85dB and the maximum SNR is 77.7 dB.

This paper proposes a DSM with input signal dependent forward path gain that is suitable for industrial applications, where one needs highly stable DSM operation for a wide range of amplitude of normalized input signal(-0.95 to +0.95). The range restriction is arrived assuming the supply voltage of the operational amplifiers which are used in the design of DSM as ±15 Volts. If the supply voltage can be increased to ±30 Volts, the normalized input signal can be increased to ±0.98. The application demands that the net (positive pulses-negative pulses) number of pulses at the output of DSM is proportional to the average of sampled analog input signal during each data update period. The net number of pulses at the output is used to control the stepper motors, switching converters etc., during each update period through the interface circuit. In Section II *A*, the linearity of the proposed DSM is proved. In Section II *B,* the stability of the proposed DSM is proved.

II. Proposed DSM with Signal Dependent Forward Path Gain

The instability occurs due to the non-linear nature of the quantizer. The gain of the quantizer which minimizes the error signal power needs to be found. If both S/H circuit and DSM circuit are operated by the clock with period T_C and if the outputs of the first integrator, second integrator and quantizer are denoted as $x_1(n)$, $x_2(n)$ and $y(n)$ respectively during n^{th} clock period then the optimum value of the quantizer gain, k_{opt} for N number of samples in typical DSM, is given by

$$k_{opt} = \frac{\lim_{N \to \infty} \sum_{n=0}^{N} x_2(n) y(n)}{\sum_{n=0}^{N} x_2^2(n)} \tag{3}$$

Equation (3) clearly shows that k_{opt} depends on $x_2(n)$, which in turn depends on the modulator input x_{analog}. Consequently one must have a prior knowledge of signal statistics in order to find k_{opt} [2]. The fact that there should be signal dependent gain element in the circuit to compensate the non-linear characteristics of the quantizer remains unsolved.

A. Block Diagram of Proposed DSM and Its Linearity

One possible solution is to use input signal dependent gain unit in the forward path as shown in Fig. 2. The signal dependent gain unit ($|x|$) is inserted between the first summing unit and the first integrator. X_{analog} is the low frequency control signal and is over sampled at a sampling period T_C.

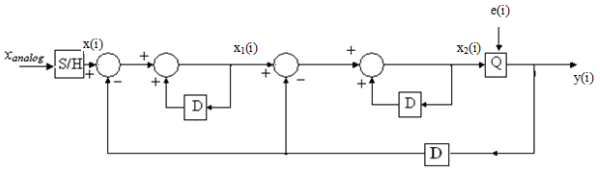

Fig. 1 Conventional DSM

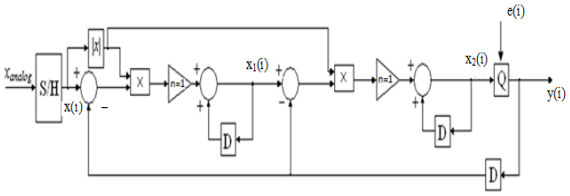

Fig. 2 Proposed DSM with signal dependent forward path gain

The proposed modulator increases the input signal range, keeping the upper bounds on the output of integrators ($x_1(i)_{max}$, $x_2(i)_{max}$) well within the safe limits and making the DSM more stable.

The linearity of the proposed DSM can be proved, considering the linear model which is shown in Fig. 2. In a linear model the quantizer is not overloaded which means that $|x_2(i)_{max}| \leq 2$. Let $e(i)$ is the quantization error signal (white noise) in i^{th} sampling period. The equation connecting $x(i)$, $y(i)$ and $e(i)$ in z-domain, in a sampling period is given by;

$$\left[\left[(X(z)-Y(z))n\,|X(z)|\left(\frac{1}{1-z^{-1}}\right)\right]-Y(z)\right] \tag{4}$$
$$\frac{n\,|X(z)|}{1-z^{-1}} + E(z) = Y(z)$$

Equation (4) can be written as,

$$\begin{aligned} &X(z)n^2 \mid X(z)\mid^2 - Y(z)n^2 \mid X(z)\mid^2 \\ &- Y(z)n \mid X(z)\mid (1-z^{-1}) + E(z)(1-z^{-1})^2 \\ &= Y(z)(1-z^{-1})^2 \end{aligned} \quad (5)$$

The average values of $x(i)$ and $y(i)$ can be obtained by setting z=1 in (5). If the dc value of $e(i)$ is finite then from (5),

$$X(1) = Y(1) \text{ or } x(k) = y(k) \text{ or } x = y \quad (6)$$

By definition, the average value of the output signal in each sampling period is given by

$$|y| = \frac{|N_p| \times T_C}{T_U} \quad (7)$$

where N_P is the net number of pulses at the output. But $|x| = |y|$ and therefore,

$$|x| = \frac{|N_p| \times T_C}{T_U} \quad (8)$$

$$|N_p| = \frac{|x| \times T_U}{T_C} \quad (9)$$

From (9), it is clear that during each update period $|N_p| \propto |x|$, which means that during each update period, the net number of pulses at the output gives the digital representation of the input signal.

B. Stability of Proposed DSM for DC Input Signal

To find the upper bounds on the state variables, $x_1(i)$ and $x_2(i)$ for dc input signal, the difference equations of proposed DSM circuit need to be solved for each clock period. At the start of the first clock period, $x_1(0) = x_2(0) = y(0) = 0$. Assuming $x(i)$ (for dc input signal $x(i)$ can be represented by x) is positive, for the first clock period the difference equation for the first integrator is given by

$$x_1(i+1) = x_1(i) + x^2 \quad (10)$$

The difference equation for the second integrator is given by

$$x_2(i+1) = x_1(i) + x_2(i) + x^2 \quad (11)$$

with initial conditions $x_1(0) = x_2(0) = 0$, the solutions of (10) and (11), which are valid during the first clock period, are given by

$$x_1(i) = ix^2 \quad (12)$$

$$x_2(i) = x^2 \frac{i(i-1)}{2} + ix^2 \quad (13)$$

Equations (12) and (13) are valid only for i=1 because during each clock period $x_1(i)$, $x_2(i)$, $y(i)$ and the feedback signal changes, resulting in new set of difference equations. Substituting k=1 in (12) and (13), result in $x_1(1)=x^2$ and $x_2(1)=x^2$. If x is positive, $y(1)$=1. The procedure is to be repeated till one limit cycle is completed.

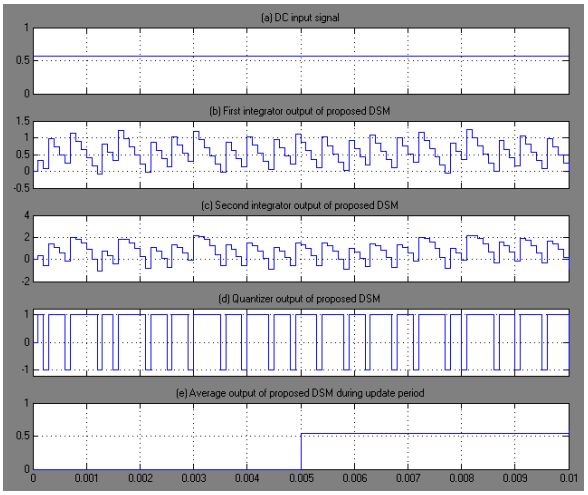

Fig. 3 Outputs of proposed DSM for dc signal. (T_U = 5ms and T_C = 0.1ms) [Horizontal axis – Time in sec. Vertical axis – Voltage in Volts for (a) to (e)]

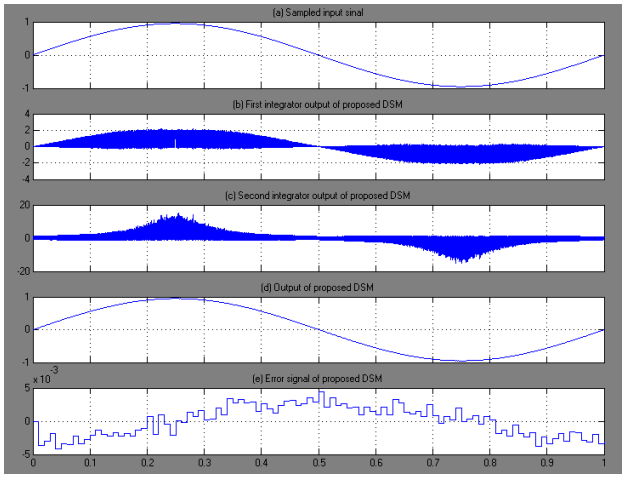

Fig. 4 Outputs of proposed DSM for sine signal. T_U = 1ms and T_C = 1μsec.) [Horizontal axis - Time in sec. Vertical axis – Voltage in Volts for (a) to (e)]

III. Simulation Results

The software, MATLAB Simulink, is used to simulate the proposed DSM. Fig. 3 shows the simulation results for a dc (0.57V) input signal. The simulation results for $x_1(i)$, $x_2(i)$ and $y(i)$ and the analytical results obtained in section 2.2, are the same. Figs. 4 (b)-(d) show the different outputs of the proposed DSM for sampled analog input signal (x) of peak amplitude 0.95 V and period one sec. which is shown in Fig. 4 (a). In the conventional DSM, when $|x| \rightarrow 0.55$, the second integrator output abruptly increases making the DSM unstable. Fig. 4 (c) shows the second integrator output of the proposed

DSM and the maximum value never exceeds ±15 V which is the supply voltage to the DSM circuit. Fig. 4 (d) shows the demodulated signal of the quantizer output of the proposed DSM, with the delay of one update period. The demodulated signal is the average voltage at the output of the quantizer during each update period. It can be seen that the demodulated signal is nearly equal to the analog input signal. The maximum error signal is about 5mV as seen in Fig. 4 (e). The Power Spectral Density (PSD) of the demodulated output of proposed DSM is shown in Fig. 5. The signal level is -10dB and near the vicinity of signal frequency the noise level is -40dB and the noise bed level is -100dB.

Fig. 5 (a) compares the SNR of conventional second order DSM and the proposed DSM2. In DSM2, the SNR never falls after certain range of input signal. The SNR steadily increases and reaches 77.7dB when x_{norp} is equal to 0dB. The dynamic input range of positive SNR of DSM2 is 85dB, which shown in Fig. 5 (b). The maximum SNR of conventional DSM is 71.5 dB when x_{norp} is equal to -7dB and when x_{norp}>-7dB, the SNR falls. For $x_{norp}\leq$ -7dB, the SNR plot of DSM2 almost follows the SNR plot of conventional DSM. For $x_{norp}>$ -7dB, the SNR continues to increase. Considering the complete input range, the SNR of DSM2 is better than that of conventional DSM.

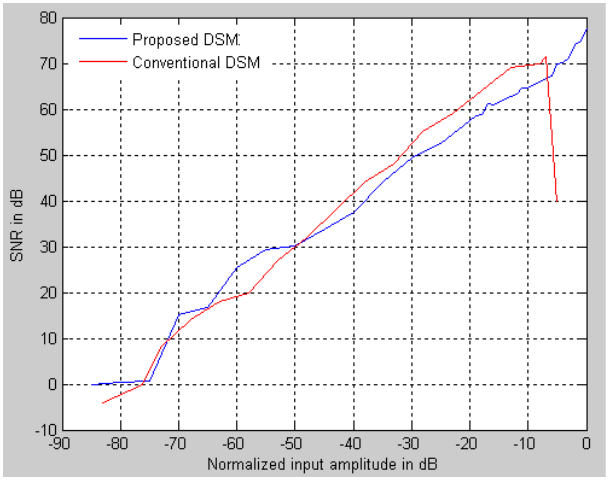

Fig. 5 SNR of Proposed DSM

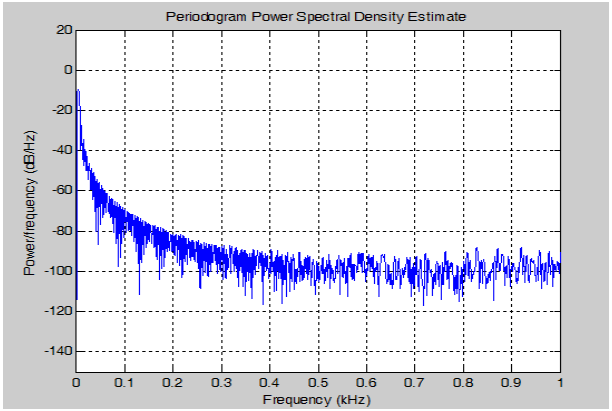

Fig. 6 PSD of Proposed DSM

IV. Conclusion

The proposed DSM, with signal dependent forward path gain, is highly stable and suitable for industrial applications where failure increases the risk. The DSM can operate for input signals with wide variation (-0.95 to +0.95) with the supply voltage of ±15 V. The state variables can never increase abruptly which would make the system unstable. In the demodulated signal, the noise level is well below the signal level.

References

[1] Richard Schreier, Gabor C. Temes, Understanding Delta-Sigma DataConverters, (IEEE Press, 2005).
[2] S.R. Norsworthy, R.Schreier and G.C. Temes, Eds., Delta-Sigma Data Converters, (IEEE Press, 1997).
[3] George I Bourdopoulos, Delta-Sigma Modulators Modeling, Design and Applications, (Imperial College Press, 2003).
[4] S. Hein and A. Zahor, "On the stability of interpolative sigma delta modulators," IEEE Transcations on Signal Processing, Vol.41, No.7, July (1993), pp. 2322-2348.
[5] Bourdopoulos G.I. "*Adaptive order reduction scheme for high-order single-bit ΔΣModulators*" IEEE Transactions on Circuits and Systems, Vol. 51, No. 5, pp. 213- 216,2004.
[6] Maghari N., Kwon S., Temes G.C. and Moon U. "*Mixed – Order Sturdy MASH Δ-Σ Modulator*"IEEE International symposium on Circuits and Systems, pp. 257-260, 2007.
[7] Jiaxin, Wanrong Zhang, Haolin Du, Yanfeng Jiang and YaminZhang) "*New architecture of low voltage Sigma-Delta ADC*" IEEE 8th International Conference on ASIC, pp. 203-206, 2009.
[8] Yavari M, Shoaei O and Rodriguez-Vazquez A "*Double-sampling single-loop Sigma-Delta Modulator topologies for broad- band applications*" IEEE Transactions on Circuits and Systems II, Vol.53, No.4, pp. 314-318,2007.
[9] Maghari N., Temes G.C. and Moon U. "*Single loop ΔΣ modulator with extended dynamic range*" Electronics letters, Vol.44, No.25, pp. 1452-1453,2008.
[10] Yongsheng Wang ; Yuanhong Li ; Mingyan Yu "A 16 bit low voltage low power Delta Sigma modulator", Conference on Electronic and Mechanical Engineering and Information Technology (EMEIT), 2011 Vol. 6, Pages: 3178 – 3181.
[11] Mohammadi, R. , Shamsi, H. , Abedinkhan, M., "On the designof a 2-2-0 MASH delta-sigma-pipeline modulator", IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2012 , Page(s): 348 - 351 .
[12] Athar S., Siddiqi M.A. , Masud S. **"**Design and FPGA Implementation of a 2nd Order Adaptive delta signma modulator with One Bit Quantization", 2010 , Page(s): 388 – 393.
[13] Youngjae Jung, HyungdongRoh, "An Input-Feedforward Multibit Adder-Less Modulator for Ultrasound Imaging Systems", IEEE Transactions on Instrumentation and Measurement, Vol.62, No.8, August 2013, Pages 2215-2227.