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Low Power CNFET SRAM Design

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***Abstract*—**CNFET has emerged as an alternative material to silicon for high performance, high stability and low power SRAM design in recent years. SRAM functions as cache memory in computers and many portable devices. In this paper, a new SRAM cell design based on CNFET technology is proposed. The proposed SRAM cell design for CNFET is compared with SRAM cell designs implemented with the conventional CMOS and FinFET in terms of speed, power consumption, stability, and leakage current. The HSPICE simulation and analysis show that the dynamic power consumption of the proposed 8T CNFET SRAM cell's is reduced about 48% and the SNM is widened up to 56% compared to the conventional CMOS SRAM structure at the expense of 2% leakage power and 3% write delay increase.

***Keywords*—**SRAM cell, CNFET, low power, HSPICE.

I. Introduction

A significantly large segment of modern systems on chips (SoCs) is occupied by Static Random Access Memory (SRAM) for its higher speed and lower power consumption. SRAM is the building unit of the cache memory which is widely used in computer systems and many portable devices. As per the prediction of the International Technology Roadmap for Semiconductors (ITRS), an embedded cache will occupy 90% of a system on chip by 2013 [1]. Therefore, studying stability and power consumption of SRAM is of crucial importance. With the rapid scaling of transistor size, supply voltage scales down. As a result threshold voltage also decreases which increases the leakage current exponentially [2]. Scaling down of transistors below 22nm faced serious limits such as electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping [1]-[3]. Leakage components contribute a significant amount of the processor power consumption. In 65 nm and below technologies, 30-40% of processor power is contributed by leakage components [2]. As a result, various academic and industrial research groups have taken initiatives for incorporating new semiconductors as the channel material. However, a hybrid technology is desired, where silicon remains the handling substrate for fabrication processing, heat transport, and mechanical support. One such system is carbon nanotubes based FET known as carbon nanotube field effect transistor [4]. Carbon nanotube field effect transistors are promising for their unique One-dimensional band-structure which suppresses backscattering and makes near ballistic operation possible [5]. Also, CNFET has a significantly smaller off current which greatly reduce the power consumed at off state of CNFET [6]. Several CNFET based SRAM cell designs have been proposed recently [6], [7], [8]. The proposed designs predict improved performance of CNFET based SRAM over CMOS counterpart in terms of static noise margin (SNM), standby power, access time and write margin. A low leakage CNFET SRAM cell was suggested using forced stack technique [2].

In this paper, the effect of channel length of access transistor on standby power, stability and write time of CNFET based SRAM cell is investigated and reported for the first time. Based on this investigation, a low standby power CNFET SRAM cell is proposed with maximum possible stability and minimum possible write time.

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II. Characteristics of CNFET Structure

Carbon nanotube field effect transistor (CNFET) utilizes one or more semiconducting single wall carbon nanotubes (SWCNTs) as channel material and silicon as the substrate. A SWCNT is a hollow cylindrical structure of carbon atoms with diameter in the nanometer range. It can be visualized as a rolled up graphene sheet and can be semiconducting or metallic depending on the chirality (m,n) i.e. the direction in which graphene sheet is rolled. A CNT is metallic when m-n=3i, where i is an integer otherwise it is semiconducting. The diameter of CNT is dependent on chirality and is given by [9],

$$D_{CNT} = \frac{\sqrt{3}}{\pi} a \sqrt{m^2 + mn + n^2} \quad (1)$$

Here a is carbon-carbon bond length (~1.42˚ A). The bandgap of carbon nanotube is inversely proportional to the diameter [10]. The diameter therefore influences the threshold voltages of carbon nanotube. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap [10]:

$$V_{th} = \frac{F_g}{2e} a = \gamma \frac{a}{eD_{CNT}} \quad (2)$$

Here γ is tight binding energy (3.033eV). Thus, the threshold voltage of the CNFETs using (19, 0) CNTs as channels is 0.289V because the DCNT of a (19, 0) CNT is 1.49nm.

Fig. 1 shows a typical device structure of CNFET used in the Stanford CNFET model [11]. Single or multiple devices can be fabricated using the same CNT and single or multiple CNTs can be placed under the same gate [10]. The segment of CNT under the gate is intrinsic and acts as channel region. The

other regions are heavily doped and act as source/drain extensions region and/or interconnection between two adjacent CNT devices. The gate, source and drain contacts, and interconnects are defined by conventional lithography [12]. The inter CNT distance defined as pitch is determined by the synthesis process.

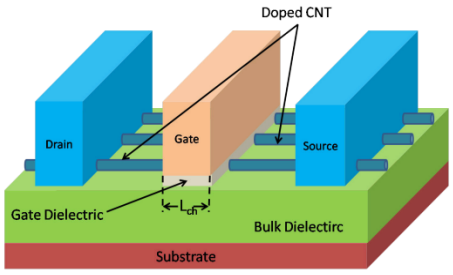

Fig. 1 Device structure of CNFET Low power 8T SRAM Cell

Write/Read operations

In the proposed 8T SRAM, the write and read bits are separated. While bit and bit-bar lines are used for writing data in the traditional 6T SRAM, only the WRITE BIT in Fig. 2 is used in the proposed SRAM cell to write for both ”0” and ”1” data. The writing operation starts by disconnecting the feedback loop of the two inverters. By setting ’Wbar’ signal to”0”, the feedback loop is disconnected. The data that is going to be written is determined by the WRITE BIT voltage. If the feedback connection is disconnected, SRAM cell has just two cascaded inverters. WRITEBIT transfers the complementary of the input data to Q2, cell data, which drives the other inverter (P2 and N2) to develop Q bar. WRITE BIT has to be pre-charged “high” before and right after each write operation. When writing”0” data, negligible writing power is consumed because there is no discharging activity at WRITEBIT. To write ’1’ data at Q2, The WRITE BIT have to be discharged to ground level, just like 6T SRAM cell. In this case, the dynamic power consumed by the discharging is the same as 6T SRAM. The write circuit does not discharge for every write operation but discharges only when the cell writes ”1” data, and the activity factor of the discharging WRITE BIT is less than ”1”, which makes the proposed SRAM cell more power effective during writing operation compared with the conventional ones. All the Read Bit lines are pre-charged before any READ operation. During read operation, transistor N5 is turned on by setting Wbar signal high and the READ ROW(RD) is ”high” to turn on N6. When Q2=”0”, the N4 is off making the READ BIT voltage not change from the pre-charged value, which means the cell data Q2 holds ”0”. On the other hand, If Q2=”1”, the transistors N4 and N6 are turned on. In this case, due to charge sharing, the READBIT voltage will be dropped about 100-200mV, which is enough to be detected in the sense amplifier.

III. Carbon Nanotube Configuration

The operation of writing”1” is stable because NMOS transistor N3 can pass”0“ faithfully. On the other hand, when writing ”0”, WRITE BIT is pre-charged high (VDD) and N5 is turned off. The node voltage at Q1 is less than VDD due to the threshold voltage drop between the gate and source of the transistor N3. To compensate this voltage drop, the transistor N2 and P2 must be designed as a low-skew inverter to ensure Q2 to be solid ground level to represent ”0“ state. A low-skewed inverter has a weaker PMOS transistor. If the PMOS CNFET has only one tube, the current is minimum. Let’s suppose that the cell stores ”0” at Q2 and ”1” at Q bar after WL(Word Line) is deactivated and W bar is activated. In this case, the voltage at Q1 is less than VDD due to the threshold voltage drop across the gate and source of the transistor N5. The degraded voltage at Q1 may turn on the transistor P2 slightly causing short circuit current through transistors P2 and N2. To overcome this problem, the low skewed inverter (N2 and P2) mentioned for writing”0” case is justified again and the Vth of the transistor N5 needs to be controlled low to reduce the voltage difference between Q bar and Q1. To implement a low skewed inverter with transistors N2 and P2, transistor ratio of N2 to P2 should be at least 2 to have a solid ground level at Q2.

However, by increasing the number of tubes, the P2 and N2 area sizes can be same. That is, if P2 has only one tube and N2 has 2 tubes, then the current ratio N2/P2 can be more than 2. This means that the inverter transistor sizes N2/P2 can be smaller than 2 by controlling the number of tubes. Transistor ratio N3/P2 of 1.3, N1/P2 of 3, and low Vth of the transistor N5 guarantees a stable READ operation when Q bar stores ”0”. However, if the similar approach to N2/P2 sizing is used to optimize transistor ratios among N1, N3 and P2, the transistor sizes can be further reduced. If N3 has only one tube, N1 has two tubes and P2 has one tube, the transistor N1 needs to be only 1.5 times larger than transistor P2 to satisfy the relationships among N1, N3, and P2. Combining the threshold voltage controllability F of the CNFET varying the diameter of tubes and transistor sizing techniques, the proposed 8T SRAM cell can accomplish low power consumption due to smaller node capacitance and tuning Vth at the minimal cost of the area overhead.

IV. Simulation Results

In order to compare performances, total 8 different SRAM cells are designed; Each 6T SRAM and 8T SRAM cells are designed using tied FinFETS (front and back gates of the FinFETS are tied together), independent double gates Fin-FETS(front and back gates are independently controlled), CMOS and CNFET. The 6T independent gate FinFET SRAM (6T-Ind) is implemented by using in-dependent gate control which connects the back gates of the NMOS (PMOS) independent-gate FinFET operates in the dual-gate mode transistors to GND (VDD) to reduce the leakage current. An (DGM) when both gates are biased to induce channel inversion. Alternatively, an independent-gate n-FinFET (p-FinFET) operates in the single-gate mode when one of the gates is deactivated by connecting the gate to ground (VDD). Disabling one of the gates in the single-gate mode (SGM) increases the absolute value of the threshold voltage compared to DGM. Therefore, it is possible to modulate the threshold

voltage of the FinFET by biasing the two gates independently [13]. And the proposed 8T SRAM)8T-Ind) configuration is that back gate of PMOS connected to the VDD and front and back gates of N1, N2, N6 are tied together and back gate of N3, N4 are connected together.

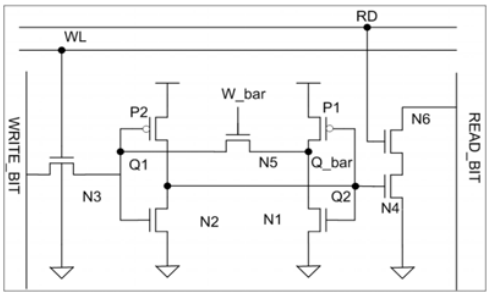

Fig. 2 The 8T SRAM CNFET structure

V. Simulation Setup

The technology parameters for the FinFETs are; channel length (L) = 32nm, fin height (Hfin) = 32nm, fin thickness (tsi) = 8nm, oxide thickness (tox) = 1.6nm, channel doping = 020 cm^{-3}, source/ drain doping = 2x1020cm^{-3}, work functions (N-FinFET)=4.5eV, work functions (P-FinFET) = 4.9eV. The technology parameters for the CNFETs are: physical channel length = 32.0nm, 10nm (this value used in simulations for performances with VDD variations), the length of doped CNT drain-side/source-side extension region =32.0nm, fermi level of the doped S/D tube. =0.6 eV, the thickness of high-k top gate dielectric material =4.0nm, chirality of tube =(19,0), Pitch = 10nm, Vfbn, Vfbp (flatband voltage for n-CNFET and p-CNFET)=0.0eV, 0.0eV, physical gate length=32.0nm, the mean free path in intrinsic CNT=200.0nm, the length of doped CNT source/drain extension region. =32.0nm, the mean free path in p+/n+ doped CNT = 15.0nm, the work function of Source/Drain metal contact = 4.6eV, CNT work function = 4.5eV. The minimum transistor sizes used for those technologies are W=48nm and L = 32nm for bulk CMOS, Hfin=32nm and L=32nm for FinFET, and L=32nm and the number of tubes=1 for CNFET. The HSPICE using the Predictive Technology Model (PTM) model and Stanford University CNFET model is used to simulate the performance of the proposed 8T SRAM and the conventional 6T SRAM cells designed with CMOS, FinFET, and CNFET transistors.

VI. Dynamic Power Consumption

The proposed 8T SRAM achieves 48% writing power saving while maintaining the cell performance, read/write delay, and stability of the conventional cell. The power saving comes from the fact that the cell keeps WRITE BIT "high" instead of discharging when it writes "0", which reduces the activity factor of the WRITE BIT. While conventional 6T SRAM always discharges one of the bit lines to write a data into the cell, the proposed 8T SRAM discharge the WRITE BIT only when it writes "1". As the probability of writing '0' gets higher, the power dissipation due to the bit line discharging is reduced comparing to the conventional case. CNFET shows about 5 times less power consumption compared to CMOS.

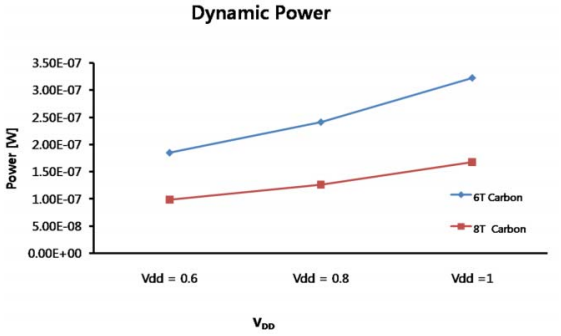

Fig. 3 The Dynamic Power consumption with VDD variation

Fig. 3 shows the dynamic power consumption of the CNFET 8T SRAM cell for different VDD. As shown in the Fig. 3, the power saving of the 8T SRAM on CNFET becomes greater as VDD increases since the dynamic power difference between the 6T SRAM and the proposed 8T SRAM increases exponentially as VDD increases.

VII. Leakage Power Consumption

Fig. 4 shows the leakage power of the 6T and 8T CNFET SRAM cell. The proposed 8T SRAM cell design shows slightly higher leakage power because it has one more leakage current path than the conventional SRAM cell. The READ BIT, N4, N6 constitutes an additional leakage current path. However, N4, N6 has a stack effect that reduces the sub-threshold leakage current a bit. As a result, the leakage current through the READ BIT, N4, and N6 path is relatively small. The difference of the leakage current in all of the four configurations is less than 2%.

VIII. Cell Stability

Fig. 5 shows the Static Noise Margin (SNM) difference between the conventional 6T SRAM and the proposed 8T SRAM. Static Noise Margin is the standard metric to measure the stability in SRAM bit cells [14]. The static noise margin of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. The voltage transfer curves (VTCs) of the back-to-back inverters in a bit-cell are used to measure SNM [15]. Separating the Read and Write bit offers wider SNM during read operation as shown in Fig. 4. When reading the stored data, only READ BIT affects inv1 (N1/P1) output voltage. Consequently, this fact makes the cell hard to flip.

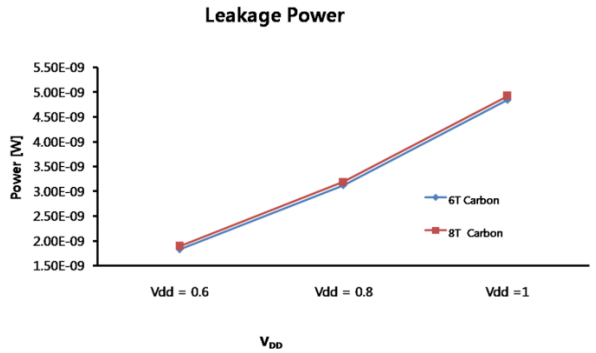

Fig. 4 The Leakage Power consumption with VDD variation

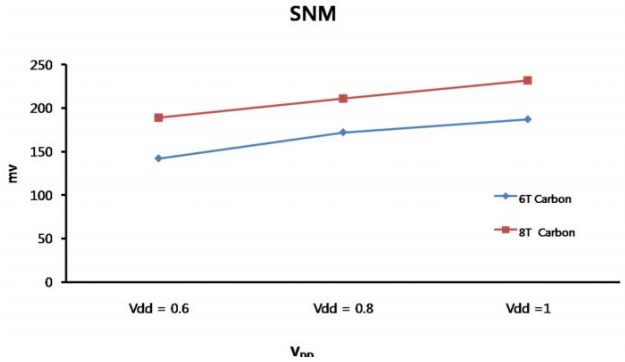

Fig. 5 SNM for 6T and 8T CNFET cell with VDD variation

The READ access time at the cell level is determined by the time taken for the bitlines to develop a potential difference of at least 100mV. The read time depends on the READ path's transistors' sizes. The proposed 8T SRAM cell's READ delay is almost same as the conventional cells since the transistor sizes are very similar. For write operation, the write delay is defined as the time from the 50% activation of the WL to the time when Q bar becomes 90% of its full swing. The write delay is approximately equal to the propagation delay of the inv2 (N2/P2) and inv1. Because the inv1 is only driving the diffusion capacitor of N5, it is desirable to reduce the input capacitance of the inv1 as much as possible to reduce the load capacitance on inv2. The proposed 8T SRAM is slightly slower than 6T SRAM in writing operation because of this reason. Because the device performance based on intrinsic CV/I gate delay metric is 6 time for nFET and 14 times for pFET higher than CMOS, the speed of the write and read operation in CNFET is about 5 or 6 times faster than CMOS and FinFET technologies.

IX. Summary

The new SRAM cell cuts off the feedback connection between the two back-to-back inverters in the SRAM cell when data is written and separates the write and read port with 8 transistors. The proposed technique saves dynamic power by reducing discharging frequency during write operation. Compared to 6T SRAM structure, the proposed 8T SRAM saves power up to 48% and obtains 56% wider SNM during read operation at the minimal cost of 2% leakage power and 3% delay increase. As the cells are more frequently accessed, the dynamic power saving is linearly increased. This paper also compares CMOS, FinFET and CNT6T and 8T SRAM cells using HSPICE simulations. The result demonstrates from 3 to 7 times less dynamic power consumption, from 11 to17 times less leakage power consumption, from 5 to 6 times faster read and write operations, and 1.6 wider SNM than the conventional designs.

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