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Recent Advances in Pulse Width Modulation Techniques and Multilevel Inverters

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Abstract**—**This paper presents advances in pulse width modulation techniques which refers to a method of carrying information on train of pulses and the information be encoded in the width of pulses. Pulse Width Modulation is used to control the inverter output voltage. This is done by exercising the control within the inverter itself by adjusting the ON and OFF periods of inverter. By fixing the DC input voltage we get AC output voltage. In variable speed AC motors the AC output voltage from a constant DC voltage is obtained by using inverter. Recent developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them. A fast space-vector pulse width modulation (SVPWM) method for five-level inverter is also discussed. In this method, the space vector diagram of the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. After decomposition, all the remaining necessary procedures for the three-level SVPWM are done like conventional two-level inverter. The proposed method reduces the algorithm complexity and the execution time. It can be applied to the multilevel inverters above the five-level also. The experimental setup for three-level diode-clamped inverter is developed using TMS320LF2407 DSP controller and the experimental results are analyzed.

Keywords**—**Five-level inverter, Space vector pulse wide modulation, diode clamped inverter.

I. Introduction

PULSE width modulation refers to a method of carrying information on train of pulses and the information be encoded in the width of pulses. The AC voltage is dependent on two parameters i.e. amplitude and frequency. It is essential to control these two parameters. The most efficient to control these parameters are by using Pulse Width Modulation techniques. In order to generate the gating signals using Pulse Width Modulation Techniques. We compare the reference signal amplitude (A_r) with carrier signal amplitude (A_c). The fundamental frequency of output voltage is determined using the reference signal frequency. The inverter output voltage is determined by the following way:

When $A_r > Ac$, $V_{AO} = V_{dc}/2$
When $A_r < Ac$, $V_{AO} = V_{dc}/2$

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The ratio of A_r to A_c is called Modulation index. The Pulse width can be varied from 0 to180 (degrees) by varying A_r from 0 to A_c.

Recent developments in power electronics and semiconductor technology have lead improvements in power electronic systems [1]. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them. Three-level voltage fed PWM inverters are recently showing popularity for multi-megawatt industrial drive applications. The main reason for this popularity is that the output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion and large voltage between the series devices is easily shared. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently [2], [3]. This technique results in higher magnitude of fundamental output voltage available compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states.

II. Basic Pulse Width Modulation Techniques

A. Single Pulse Width Modulation

In Single Pulse Width Modulation control, the width of the pulse is varied to control the inverter output voltage and there is only one pulse half per cycle. By comparing the rectangular reference signal with the triangular carrier wave the gating signals are generated as shown in Fig 1. The frequency of reference signal determines fundamental frequency of output voltage.

The advantages of this technique are the even harmonics are absent due to the symmetry of the output voltage along the x-axis and N^{th} harmonics can be eliminated from inverter output voltage if the pulse width is made equal to $2\pi/n$. But the disadvantages are the output voltage introduces a great deal of harmonic content and at a low output voltage the distortion factors increases significantly.

B. Multiple Pulse Width Modulation

In Multiple Pulse Width Modulation several equidistant pulses per half cycle are generated as shown in Fig 2. By using several pulses in each half cycle of output voltage the harmonic content can be reduced.

In this technique the amplitudes of lower order harmonics are reduced and derating factor is reduced significantly. But the fundamental component of output voltage is less, the amplitudes of higher order harmonics increases significantly

and switching losses are increased.

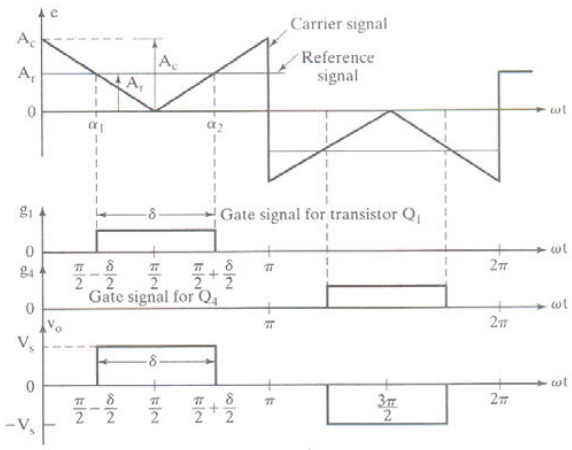

Fig. 1 Single pulse width modulation

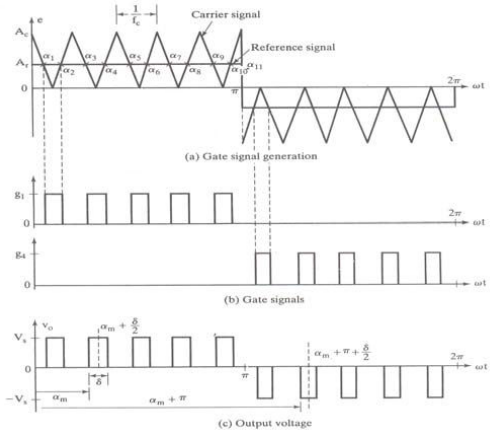

Fig. 2 Multiple pulse width modulation

C. Sinusoidal Pulse Width Modulation

In Multiple Pulse Width Modulation, by varying the width of each pulse in proportion to the amplitude of the reference wave the distortion factor and lower order harmonics can be reduced significantly and the width of all the pulses are maintained the same. This type of modulation is known as Sinusoidal Pulse Width Modulation.

By comparing sinusoidal reference signal with a triangular carrier wave of frequency, f_c, the gating signal is generated. The inverter output frequency, f_o, and its peak amplitude, A_r, determines the frequency of reference signal f_r and controls the modulation index, M, and then in turns the rms output voltage, V_o. The number of pulses per half cycle depends upon the carrier frequency. By varying the modulation index M, the rms output voltage can be varied. Each pulse corresponds approximately to the area under sine wave between the adjacent midpoints of off periods on the gating signals.

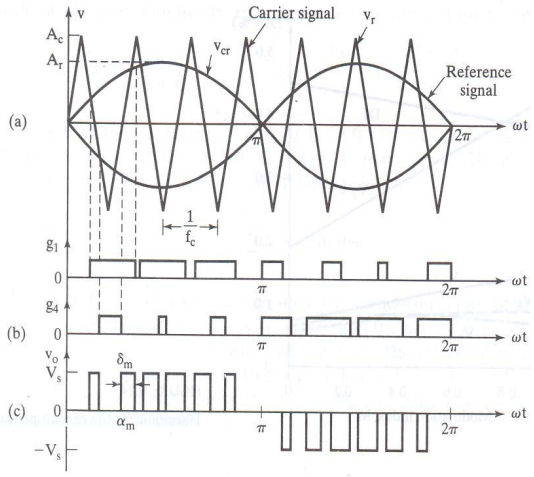

Fig. 3 Sinusoidal pulse width modulation

III. Advanced Modulation Techniques

A. Trapezoidal Modulation

By comparing a triangular carrier wave (V_c) with a reference trapezoidal wave (V_r), the switching instance to semiconductor devices are generated. This type of modulation increases the peak fundamental output voltage up to 1.05Vd, but output voltage contains lower order harmonics.

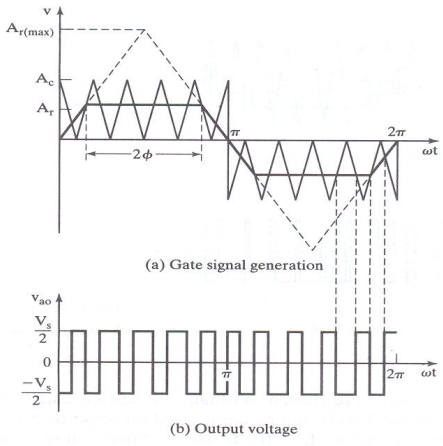

Fig. 4 Trapezoidal modulation

B. Staircase Modulation

In staircase Pulse Width Modulation the modulated wave eliminates specific harmonics. In order to obtain desired quality of output voltage, the modulation frequency ratio m_f and the number of steps are chosen. If the number of pulses is less than 15 per half cycle this is optimized pulse width modulation.

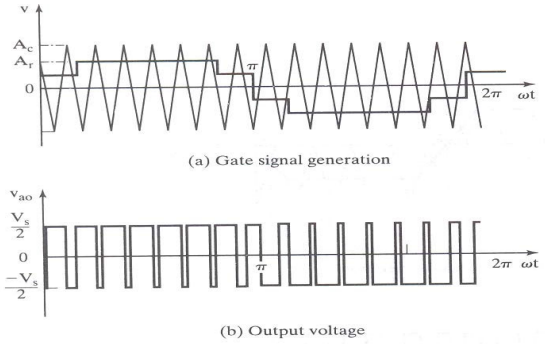

Fig. 5 Staircase modulation

C. Stepped Modulation

In this modulation the signal is stepped wave. In order to control the magnitude of the fundamental component and to eliminate specific harmonics this wave is divided into specific intervals, with each interval being controlled individually. When compared to that of normal Pulse Width Modulation control this type control gives low distortion but higher fundamental amplitude.

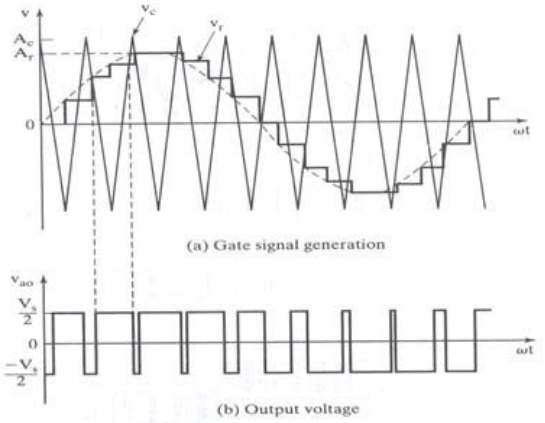

Fig. 6 Stepped modulation

D.Harmonic Injected Modulation:

In this modulation the signal is generated by injecting harmonics to the sine wave. The result is a flat topped wave form and it reduces the amount of over modulation. A higher fundamental amplitude and low distortion of output voltage is provided. The amplitude of fundamental components is approximately 15% more than that of normal sinusoidal Pulse Width Modulation.

E. Delta Modulation:

In this modulation a triangular wave is allowed to oscillate within a defined window Δv above and below the reference wave V_r. From the vertices of the triangular wave V_c, the output voltage is generated. This type of modulation is also known as Hysteresis modulation. Keeping the slope of the triangular wave constant, if the frequency of modulating wave is changed, the number of pulses and pulse widths of modulated wave would change. The fundamental output voltage can be up to V_S and is dependent on peak amplitude A_r and frequency f_r of reference voltage. This modulation can control the ratio of voltage to frequency. Depending on the permissible harmonic content in the inverter output voltage, machine type, power level and semi conductor switching devices employed for a particular application, the particular Pulse Width Modulation is choose.

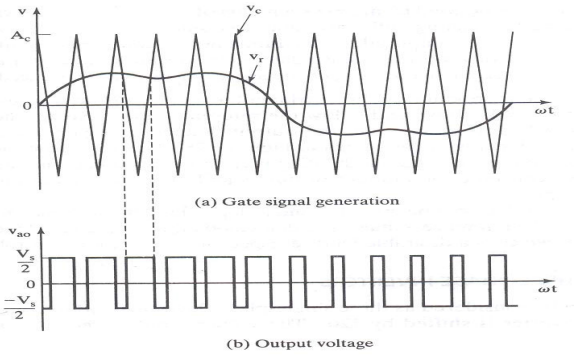

Fig. 7 Harmonic injected modulation

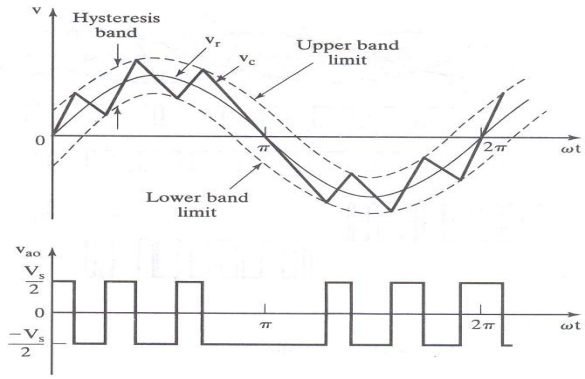

Fig. 8 Delta modulation

F. Space Vector Pulse Width Modulation:

This modulation is relatively new and popular technique in controlling motor devices. In SVPWM method the output voltage is approximated by using the nearest three output vectors that the nodes of the triangle containing the reference vector in the space vector diagram of the inverter. When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location. The main advantage of this technique is that it will generate less harmonic distortion in the output voltages and currents [4].

Advantages of Pulse Width Modulation Techniques:

- Using Pulse Width Modulation techniques lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are also minimized.

- Both the output voltage and frequency control is possible in a single power stage of the inverter without any additional components.
- The presence of constant DC supply permits the parallel operation of several independent Pulse Width Modulation inverters on the same rectifier power supply. Pulse Width Modulation inverter has a transient response which is much better than that of quasi-square wave rectifier.
- The commutative ability of Pulse Width Modulation inverters remain substantially constant compared to variable dc link inverter, irrespective of the voltage and frequency settings.
- The power factor of the system is good, as a diode rectifier can be employed on the line side.
- With constant DC supply used in Pulse Width Modulation, we can obtain commutation even at low voltage whereas six - step inverter needs an auxiliary DC supply for commutating thyristors at low output voltages.
- The amplitude of torque pulsations are minimized even at low speeds.
- A sophisticated Pulse Width Modulation technique eliminates lower order harmonics in the motor current, low speed torque pulsations and cogging effects.

IV. Five-Level SVPWM Inverter

Fig. 9 shows diagram of a five-level diode clamping inverter. Each leg is composed of four upper and lower switches with anti-parallel diodes. Four series *dc*-link capacitors split the *dc*-bus voltage in half, and eighteen clamping diodes confine the voltages across the switches within the voltages of the capacitors. The necessary conditions for the switching states for the five-level inverter are that the *dc*-link capacitors should not be shorted, and the output current should be continuous. As indicated in Table I, each leg of the inverter can have five possible switching states, P_1, P_2, O, N_1 or N_2. When the top four witches Sx_1, Sx_2, Sx_3 and Sx_4 ($x = a, b, c$) are turned on, switching state is P_2. When the switches Sx_2, Sx_3, Sx_4 and Sx_5 are turned on switching state is P_1. When the switches Sx_3, Sx_4, Sx_5 and Sx_6 are turned on, the switching state is O. when the switches Sx_4, Sx_5, Sx_6 and Sx_7 are turned on, the switching state is N_1. When the switches Sx_5, Sx_6, Sx_7 and Sx_8 are turned on, the switching state is N_2.

Fig. 10 shows the space vector diagram for five-level inverter. The output pace vector is identified by combination of switching states P_2, P_1, O, N_1 or N_2 of the three legs. For example, in the case of P_2ON_1, the output terminals a, b and c have the potentials $2E$, 0, and $-E$ respectively. Since five kinds of switching states exist in each leg, three-level inverter has $5^3 = 125$ switching states, as indicated in Fig. 10. The output voltage vector can take only 61 discrete positions in the diagram because some switches states are redundant and create the same space vector. In Fig. 10, it is also indicated an arbitrary reference vector V* to be generated by the inverter.

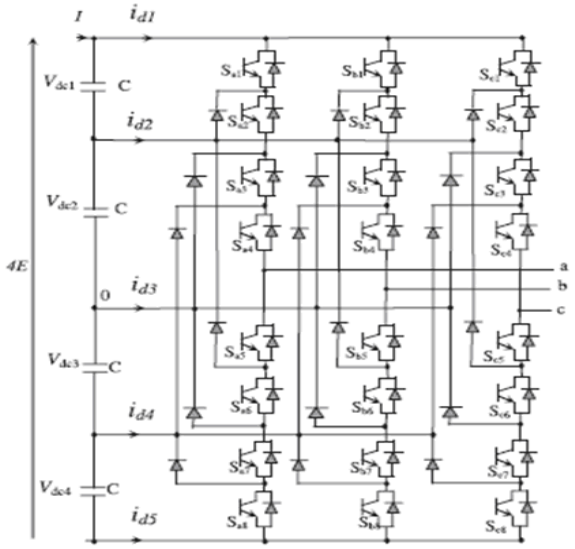

Fig. 9 Configuration of five-level inverter

TABLE I
Switching and Terminal Voltages of Five-Level Inverter

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{xo}
P_2	1	1	1	1	0	0	0	0	2E
P_1	0	1	1	1	1	0	0	0	E
O	0	0	1	1	1	1	0	0	0
N_1	0	0	0	1	1	1	1	0	-E
N_2	0	0	0	0	1	1	1	1	-2E

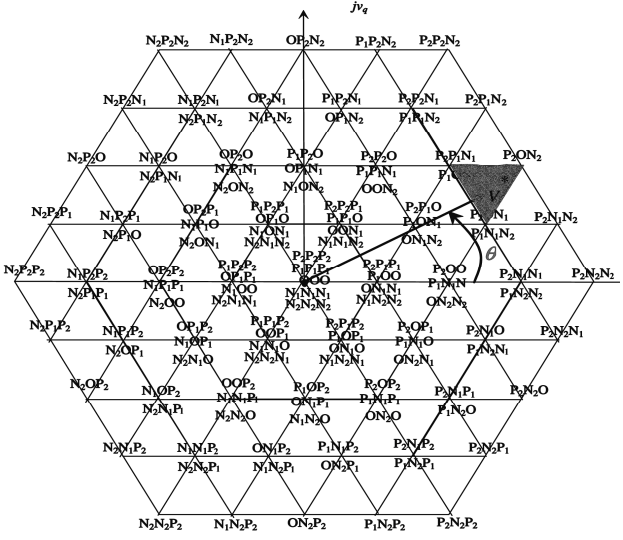

Fig. 10 Space vector diagram of five-level inverter

V. Fast Space Vector Pulse Width Modulation Method

A. Basic Principle of Proposed SVPWM Method

The space vector diagram of multilevel inverter can be divided into different forms of sub-diagrams, in such a manner that the space vector modulation becomes more simple and

easy to implement, as made in several works [5]–[9]. But these works do not reach a generalization of the two-level SVPWM to the case of multilevel inverters; either they divide the diagram into triangles, or into interfered geometrical forms. In this work, we present a simple and fast method that divides the space vector diagram of five-level inverter, within two steps, into several small hexagons, each hexagon being space vector diagram of two-level inverter, as shown in Fig. 11. This method is the extension of that presented in [10]-[12] for the case of three-level inverter. We have to make two simplifications: Firstly, the space vector diagram of five-level inverter is divided into six space vector diagrams of three-level inverters. Secondly, each one of these three-level inverter diagrams is divided into six space vector diagrams of two level inverters.

Thus the space vector modulation of five-level inverter becomes very simple and similar to that of conventional two-level inverter space vector modulation. To each this simplification, two steps have to be done. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the hexagons. Secondly we translate the origin of the reference voltage vector towards the centre of the selected hexagon. These steps are explained in the next section.

B. First Correction of Reference Voltage Vector

Having the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that contain the five-level space vector diagram Fig. 11. There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided in equality between the two hexagons as shown in Fig. 12. Each hexagon is identified by a number *s* defined as given in Table II.

TABLE II
SELECTION OF HEXAGONS BASED ON ANGLE 'Θ'

Hexagon 'S'	Location of reference voltage vector phase angle 'θ'
1	$-\pi/6 < \theta < \pi/6$
2	$\pi/6 < \theta < \pi/2$
3	$\pi/2 < \theta < 5\pi/6$
4	$5\pi/6 < \theta < 7\pi/6$
5	$7\pi/6 < \theta < 3\pi/2$
6	$3\pi/2 < \theta < -\pi/6$

After selection of one hexagon, we make a translation of the reference vector $\boldsymbol{V}^*$ towards the center of this hexagon, as indicated in Fig. 13. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table III gives the components *d* and *q* of the reference voltage $\mathbf{V}^{3}*$ after translation, for all the six hexagons. The index (3) or (5) above the components indicate three or five-level cases respectively.

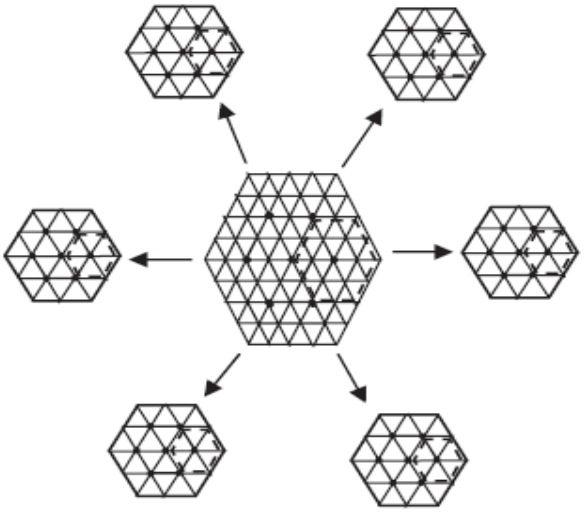

Fig. 11 Decomposition of space vector diagram of five-level inverter to six hexagons

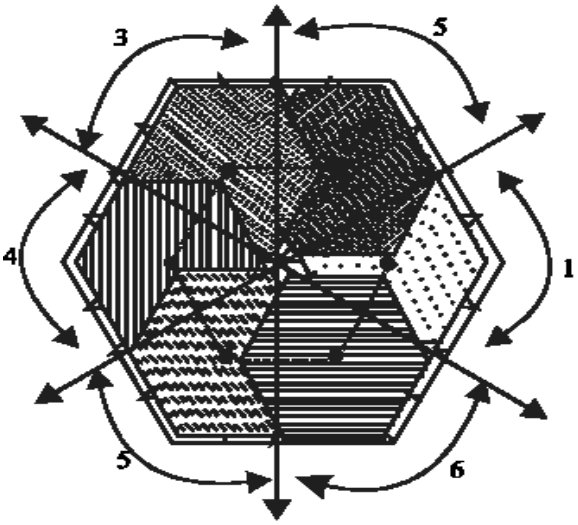

Fig. 12 Division of overlapped regions

C. Second Correction of Reference Voltage Vector

Having the selected three-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this three-level diagram Fig. 15. Here also the overlapped regions are equally divided between the two hexagons. After selection of one hexagon, we make a translation of the reference vector V^* towards the center of this hexagon, as indicated in Fig. 15. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table IV gives the components d and q of the reference voltage $V^{2}*$ after translation, for all the six hexagons. The index (2) or (3) above the components indicate two or three-level cases respectively.

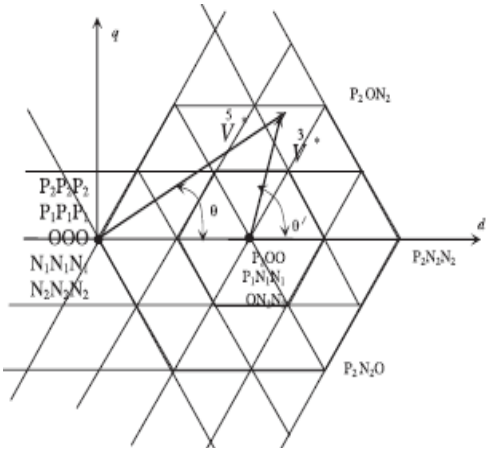

Fig. 13 First Translation of Reference Voltage Vector

TABLE III
FIRST CORRECTION OF REFERENCE VOLTAGE VECTOR

S	V_d^{3*}	V_q^{3*}
1	V_d^{5*}-1/2 cos(0)	V_q^{5*}-1/2 sin(0)
2	V_d^{5*}-1/2 cos (π/3)	V_q^{5*}-1/2 sin(π/3)
3	V_d^{5*}-1/2 cos(2π/3)	V_q^{5*}-1/2 sin(2π/3)
4	V_d^{5*}-1/2 cos(π)	V_q^{5*}-1/2 sin(π)
5	V_d^{5*}-1/2 cos(4π/3)	V_q^{5*}-1/2 sin(4π/3)
6	V_d^{5*}-1/2 cos(5π/3)	V_q^{5*}-1/2 sin(5π/3)

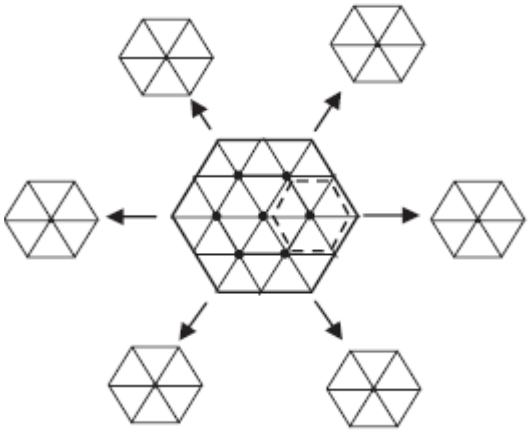

Fig. 14 Decomposition of space vector diagram of three-level inverter to six hexagons

TABLE IV
FIRST CORRECTION OF REFERENCE VOLTAGE VECTOR

S	V_d^{2*}	V_q^{2*}
1	V_d^{3*}-1/4 cos(0)	V_q^{3*}-1/4 sin(0)
2	V_d^{3*}-1/4 cos(π/3)	V_q^{3*}-1/4 sin(π/3)
3	V_d^{3*}-1/4 cos(2π/3)	V_q^{3*}-1/4 sin(2π/3)
4	V_d^{3*}-1/4 cos(π)	V_q^{3*}-1/4 sin(π)
5	V_d^{3*}-1/4 cos(4π/3)	V_q^{3*}-1/4 sin(4π/3)
6	V_d^{3*}-1/4 cos(5π/3)	V_q^{3*}-1/4 sin(5π/3)

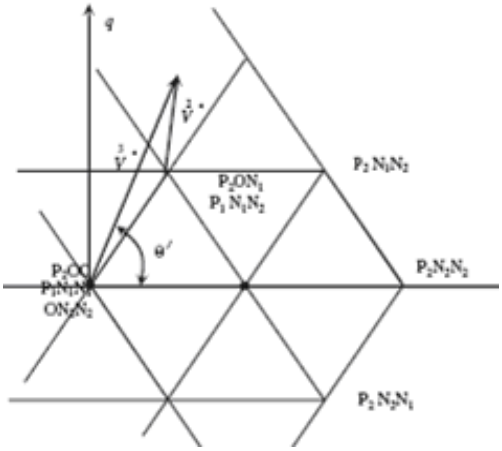

Fig. 15 Second Translation of Reference Voltage Vector

Determination of Dwelling Times

Once the corrected reference voltage V^{2*} and the corresponding hexagon are determined, we can apply the conventional two-level space vector PWM method to calculate the dwelling times, the only difference between the two-level SVPWM and the five-level SVPWM is the factor 4 appearing at the first two equations as shown in (1). The remaining procedure is implemented like conventional two-level inverter SVPWM method and two level equivalent pulses are obtained.

$$T_1 = 4*\left[\frac{\left|\vec{V^{2*}}\right|\cdot T_s\cdot\sin\left(\frac{\pi}{3}-\alpha\right)}{\sin\left(\frac{\pi}{3}\right)}\right]$$
$$T_2 = 4*\left[\frac{\left|\vec{V^{2*}}\right|\cdot T_s\cdot\sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)}\right] \quad (1)$$
$$T_0 = T_s - T_1 - T_2$$

The reference voltage vector V_2* is approximated using the nearest three states, which are nodes of the triangle containing the vector, identified as *X*, *Y* , and *Z*, For example, in the case of Fig. 16 , *X* is either the state P_2ON_1 or $P_1N_1N_2$, *Y* is the state P_2ON_2, while *Z* is either he state $P_2P_1N_1$ or the state P_1ON_2. The optimum sequence of these three states is selected so as to minimize the total number of switching transitions and fully optimize the harmonic profile of the output voltage. Note that from two level space vector modulation theories, it is well known that these sequences should be reversed in the next switching interval for minimum harmonic impact as given in [11], [12].

TABLE V
SIMULATION PARAMETERS

SVPWM Parameters	Modulation index $m = 0.8$
	DC Supply voltage E = 400V
	No. of switching intervals $n = 120$
Induction motor	5.4 HP; 4 pole; 1430 rpm; $f = 50$ Hz
	$R_s = 1.405\ \Omega$; $R_r = 1.395\ \Omega$;
	$l_s = l_r = 0.005839$ H; $l_m = 0.1722$ H
SVPWM Parameters	Modulation index $m = 0.8$

VI. EXPERIMENTAL TEST SETUP

The experimental setup employed a powerful TMS320LF2407, 16-bit DSP processor working at 40 MIPS as its controller and PEC16DSMO10A, an intelligent power module (IPM) of three phase three-level diode clamped inverter. The inverter is connected to a load of 3Ø, 0.5HP, 415V, 50 Hz, 4-pole, 1.05A, 1380 rpm induction motor and the results are obtained. The experimental setup is as shown in Fig. 16.

Fig. 16 Experimental setup of three-level inverter

VII. RESULTS AND DISCUSSIONS

In order to prove the validity of the proposed fast space vector pulse width modulation (SVPWM) method, a three phase five-level inverter fed induction motor is simulated with the simulation parameters shown in Table V. The simulation results of five-level inverter are shown in Figs. 17-19. The inverter output line to line voltage (V_{ab}) and its harmonic spectrum is shown in Fig. 18. The total harmonic distortion (THD) is only 0.64% and it proves the effectiveness of the proposed SVPWM method. Fig. 12 shows the load current and its harmonic spectrum. The speed, torque and stator currents of induction motor are shown in Fig. 21. The experimental results of three-level inverter are obtained, when a 3Ø, 0.5HP, 415V, 50 Hz, 4-pole, 1.05A, 1380 rpm induction motor is connected as load. The output line to line voltage V_{ab} and V_{cb} are shown in Fig. 20. The induction motor load currents I_{ab} and I_{bc} are shown in Fig. 22.

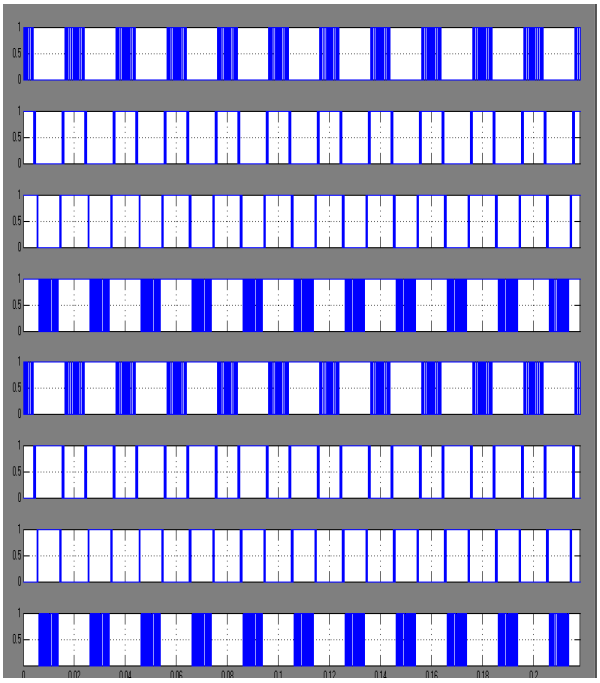

Fig. 17 Gate pulses for phase-A of five-level inverter

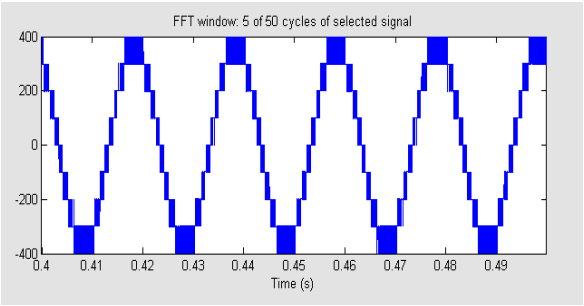

Fig. 18 (a) The line to line voltage (V_{ab}) of five-level inverter

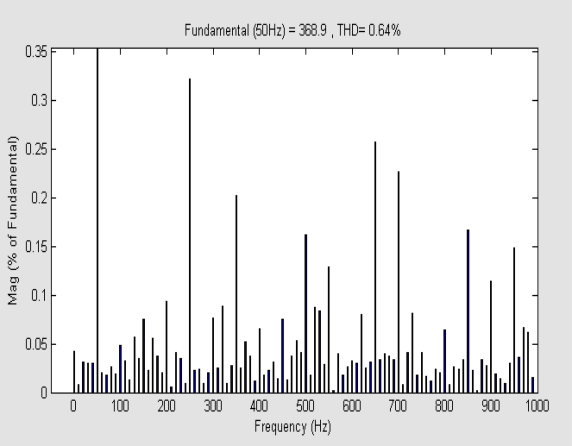

Fig. 18 (b) The harmonic spectrum of line to lime voltage of five-level inverter

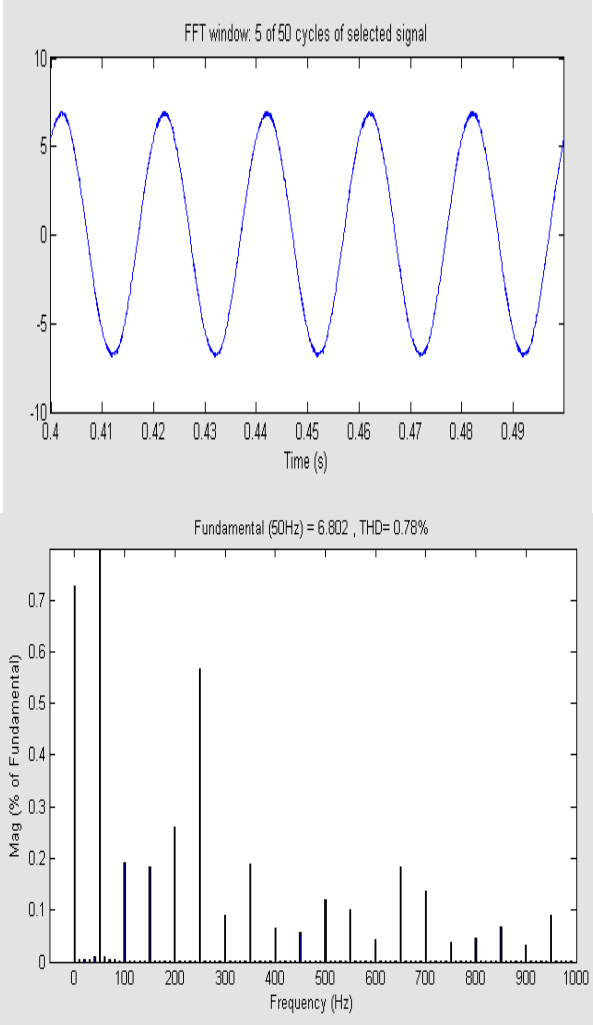

Fig. 19 The stator current I_{as} and its harmonic spectrum of five-level inverter fed induction motor

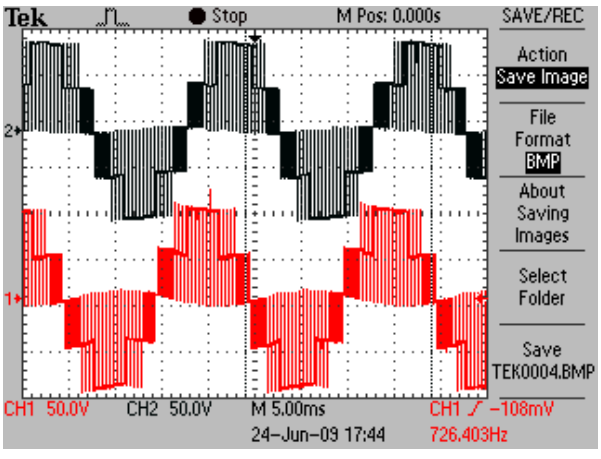

Fig. 20 The output line to line voltages V_{ab} and V_{cb} of three-level inverter

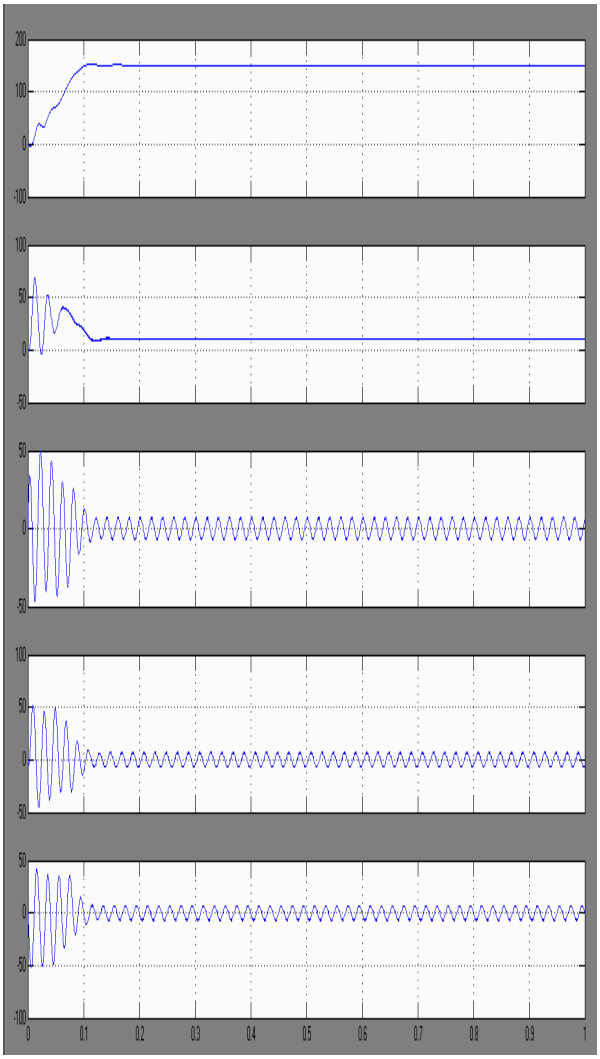

Fig. 21 Speed (N), Torque (T) and line currents Ias, Ibs, Ics of five-level inverter fed induction motor (from top to bottom)

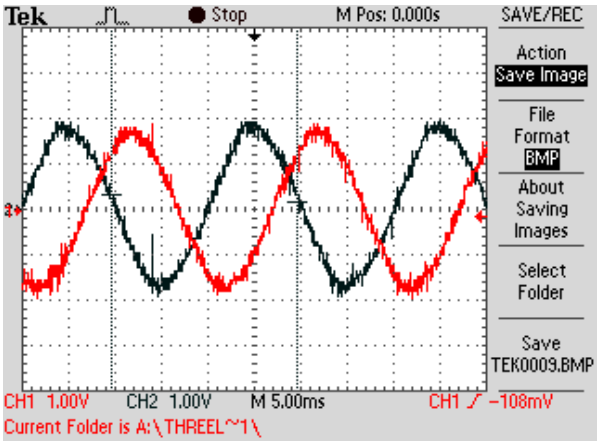

Fig. 22 The load currents I_{ab} and I_{bc} of three-level inverter fed induction motor

VIII. Conclusions

In this paper, a fast space vector pulse width modulation method has been proposed and described for a five-level inverter. In this method, the space vector diagram of the five-level inverter is decomposed into six space vector diagrams of three-level inverters. In turn, each of these six space vector diagrams of three-level inverter is decomposed into six space vector diagrams of two-level inverters. After decomposition, all the remaining necessary procedures for the three-level SVPWM are done like conventional two-level inverter. The dwelling times of voltage vectors are calculated at the same manner as two- level inverter. Thus the proposed method reduces the algorithm complexity and the execution time. It can be applied to the multi-level inverters above the five-level also. The obtained total harmonic distortion (THD) with the proposed method is only 0.64%, which is very less as compared with the other conventional methods of SVPWM techniques. The waveforms of the simulation and experimental results of three-level diode clamped inverter prove the validity of the proposed method. The results have been good agreement with the published work.

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