Closed Loop Control of Bridgeless Cuk Converter Using Fuzzy Logic Controller for PFC Applications

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Abstract—This paper is based on the bridgeless single-phase Ac–Dc Power Factor Correction (PFC) converters with Fuzzy Logic Controller. High frequency isolated Cuk converters are used as a modular dc-dc converter in Discontinuous Conduction Mode (DCM) of operation of Power Factor Correction. The aim of this paper is to simplify the program complexity of the controller by reducing the number of fuzzy sets of the Membership Functions (MFs) and to improve the efficiency and to eliminate the power quality problems. The output of Fuzzy controller is compared with High frequency triangular wave to generate PWM gating signals of Cuk converter. The proposed topologies are designed to work in Discontinuous Conduction Mode (DCM) to achieve a unity power factor and low total harmonic distortion of the input current. The Fuzzy Logic Controller gives additional advantages such as accurate result, uncertainty and imprecision and automatic control circuitry. Performance comparisons between the proposed and conventional controllers and circuits are performed based on circuit simulations.

Keywords—Fuzzy Logic Controller (FLC), Bridgeless rectifier, Cuk converter, Pulse Width Modulation (PWM), Power Factor Correction, Total Harmonic Distortion (THD).

I. INTRODUCTION

POWER supplies with active Power Factor Correction techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations. The major problem with the conventional rectifiers is harmonic content. The AC main current drawn by present-day power supplies is non-sinusoidal and reasonably phase shifted with the supply voltage waveform resulting in poor Power Factor and their use in telecommunication network present a growing problem for Power distribution. Therefore, Power Factor Correction is fundamental requirement in Switched Mode Power Supply to reduce the voltage and current distortion and losses. There are several converters for step-up/step-down applications such as buck converter, boost converter, Buck-Boost converter, and Cuk converter. A buck converter is a step-down DC-DC converter. Its design is similar to the step-up boost converter, and like the boost converter it is a Switched Mode Power Supply that uses two switches (a transistor and a diode), an inductor and a capacitor.

The Bridgeless Cuk converter is proposed and this type of DC-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. The non-isolated Cuk converter can only have opposite polarity between input and output. It uses a capacitor as its main energy-storage component, unlike most other types of converters which use an inductor. The Bridgeless rectifier reduces the switching losses and conduction loss because of having reduced number of switches. The purpose of Fuzzy Logic Controller is to influence the behavior of a system by changing an input or inputs to that system according to a rule or set of rules that model how the system operates. The main advantages of Fuzzy Logic Controller are that it allows imprecise or contradictory inputs, rule base or fuzzy sets can be easily modified, can achieve steady state in a shorter time interval. Pulse-Width Modulation is a modulation technique that confirms the width of the pulse, formally the pulse duration, based on modulator signal information. A new bridgeless single-phase AC–DC Power Factor Correction rectifier based on SEPIC and Cuk topologies was described in [1]. The topologies were designed to work in Discontinuous Conduction Mode to achieve almost unity power factor in a simple and effective manner. An interleaving totem-pole boost bridgeless PFC rectifier was reviewed in [2]. The converter consists of two interleaved and inter-coupled totem-pole boost bridgeless converter cells. A SEPIC and Cuk converters working as Power Factor Pre-regulators (PFP) in Discontinuous Conduction Mode presented the desirable characteristics such as the converter works as a voltage follower, theoretical power factor is unity, the input current ripple was defined at the design stage [3]. A simple single-phase bridgeless SEPIC rectifier with low input current distortion and low conduction losses is described in [4]. The absence of an input diode bridge and the presence of only one diode in the flowing-current path during each switching cycle result in less conduction loss and improved thermal management compared to existing PFC Rectifiers. These advantages are desirable features for high-power and high-voltage applications. A single-phase soft-switched boost AC-DC rectifier that operated with power-factor correction was described in [5]. Soft switching in the converter was achieved using a zero-current-switching quasi-resonant technique. The method of control used to ensure unity power factor operation, a constant on-time and variable off-time technique. Laszlo developed a bridgeless buck PFC rectifier that substantially improves efficiency at low line [6]. By eliminating input bridge diodes, the presented rectifier's efficiency was further improved. The rectifier doubles the rectifier output voltage, which extends useable energy of the bulk capacitor after a dropout of the line voltage. The integrated buck-flyback converter as a good solution for implementing low-cost high-power-factor ac–dc converters with fast output regulation was described in [7]. A Cuk converter with Integrated Magnetics,

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when used for input current shaping, exhibits advantages over other topologies [8]. The advantages of the Cuk converter with Integrated magnetic used in current shaping applications are automatic current shaping, zero input and output voltages, small size of magnetic even at switching frequency of 35 KHz. They introduced a new bridgeless single-ended primary inductance converter power-factor-correction rectifier [9]. The number of component conducted at each sub interval mode is reduced compared to the existing topologies in [10]. This is capable to achieve high power factor under universal input voltage condition. The capability to reshape the input current is inherent when the circuit is operated in DCM. The implementation of a bridgeless Power Factor Correction boost rectifier with low common-mode noise was described in [12]. The presented technique improves the efficiency by approximately 1% compared to the conventional PFC boost rectifier, and improves the utilization of the magnetic cores resulting in a low-cost high-power-density design.
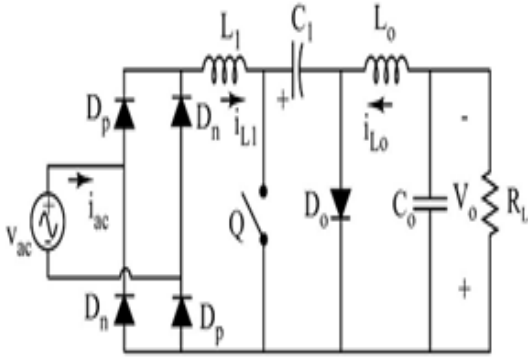

Fig. 1 Conventional Cuk PFC converter

II. DESIGN OF THE PROPOSED CIRCUIT

A. Cuk Converter

The Cuk converter is a type of DC to DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. During this interval, only the diode D_p conducts to provide a path for i_{L1}. Accordingly, the inductors in this interval behave as constant current sources. Hence, the voltage across the three inductors is zero. The capacitor C_1 is being charged by the inductor current i_{L1}. This period ends when Q_1 is turned ON. By applying inductor volt-second across L_1 and L_{01}, the normalized length of the second stage period can be expressed as follows:

$$D_2 = \frac{D_1}{m} \sin \omega t \qquad (1)$$

where ω is the line angular frequency, and M is the voltage conversion ratio ($M = V_0/V_m$).
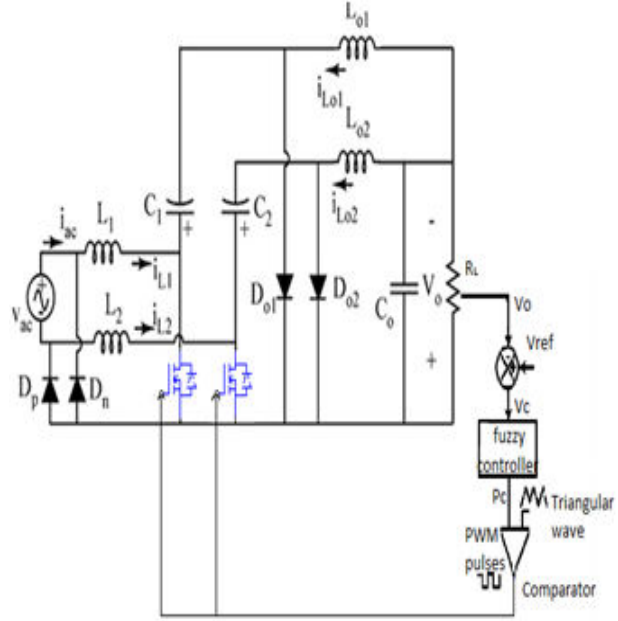

Fig. 2 Proposed circuit using Fuzzy Controller

B. Fuzzy Controller

A Fuzzy Logic Controller is used to regulate the output dc voltage and eliminates the error. The voltage error is calculated from the difference between the reference voltages V_{ref} and the output dc voltage V_o as,

$$V_e(n) = V_{ref}(n) - V_o(n) \qquad (2)$$

C. Pwm Pulse Generator

The output of Fuzzy Logic Controller P_c is compared with triangular wave to generate PWM gating signals for high frequency switches of Cuk dc-dc converters. Since the diode D_p continuously conducts throughout the entire switching period, the average voltage across C_2 is equal to the output voltage V_0. As a result, a negligible ac current will flow through C_2 and L_{02}. Therefore, the current through L_2 during the positive half cycle of the input voltage is equal to the negative current through the body diode of Q_2. It should be noted that the body diode of the inactive switch Q_2 is always conducting current during the positive half cycle of the input voltage. This is due to the low impedance of the input inductors (L_1 and L_2) at the line frequency.

D. Voltage Conversion Ratio (M)

The voltage conversion ratio M in terms of the converter parameters can be obtained by applying the power balance principle. The average input power can be expressed as follows:

$$\langle P_{in}(t) \rangle_{T/2} = \frac{2}{T} \int_0^{T/2} V_{ac}(t) \langle i_{ac}(t) \rangle_{Ts} \, dt \qquad (3)$$

The average input current over a switching cycle is given by

$$\langle i_{ac}(t) \rangle_{Ts} = \langle i_{L1}(t) \rangle_{Ts} = \frac{\langle V_{ac}(t) \rangle}{R_e} \qquad (4)$$

where the quantity Re is defined as the emulated input resistance of the converter. Similar to the conventional Cuk PFC rectifier, the input port of the proposed rectifier obeys Ohm's law. Thus, the input current is sinusoidal and in phase with the input voltage. Hence, the power stage circuit of the converter of Fig. 5 can be represented by its large signal averaged model shown in Fig. 2. Furthermore, the averaged model can greatly reduce the long computation time when it is implemented in simulation software. Evaluating (3) by using (4) and applying the power balance between the input and output ports, the desired voltage conversion ratio is

$$M = \frac{V_o}{V_m} = \sqrt{\frac{R_L}{2R_e}} \qquad (5)$$

The efficiency of the converter can be slightly improved by using synchronous rectification to turn ON the switch Q_2 during the positive half cycle of the input voltage, which eliminates its body-diode conduction. It should be noted that the voltage gain in (5) is also valid for the other two proposed topologies. However, the effective inductance (Le) varies from one topology to another.
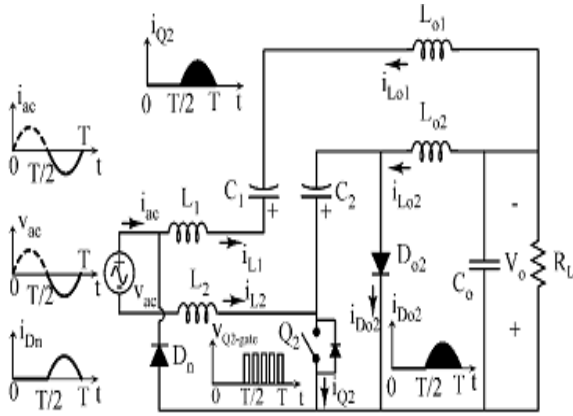

Fig. 3 Equivalent circuit

E. Boundaries between Continuous Conduction Mode and Dcm

Referring to the diode D_{01} current waveform in Fig. 4, the DCM operation mode requires that the sum of the switch duty cycle and the normalized switch-OFF time length be less than one, i.e.,

$$D_2 \leq 1\text{-}D_1 \qquad (6)$$

Substituting (1) into (6) and using R_e and (5), the following condition for DCM is obtained:

$$K_e < K_{e-crit} = \frac{1}{2(M+\sin(\omega t))^2} \qquad (7)$$

where the dimensionless conduction parameter K_e is defined as follows:

$$K_e = \frac{2L_e}{R_L T_S} \qquad (8)$$

It is clear from (7) that the value of K_{e-crit} depends on the line angle (ωt). Hence, the minimum and maximum values of K_{e-crit} is given by

$$K_e < K_{e-crit_{min}} = \frac{1}{2(M+1)^2} \text{ and} K_e < K_{e-crit\_max} = \frac{1}{2M^2} \qquad (9)$$

respectively. Therefore, for values of $K_e < K_{e-crit\_min}$, the converter always operates inDCM, and it operates in the continuous conduction mode (CCM) for values of $K_e < K_{e-crit\_max}$. However, for values of $K_{e-crit\_min} < K_e < K_e < K_{e-crit\_max}$, the converter operates in both modes: CCM near the peak value of the input line voltage and DCM near the zero crossing of the input line voltage.
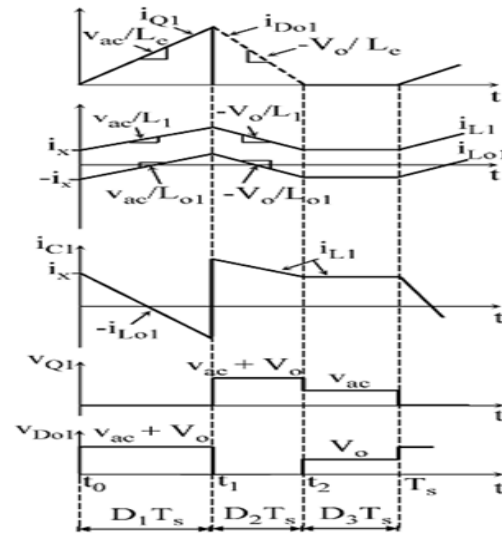

Fig. 4 Theoretical DCM waveforms during one switching period Ts for the converter

F. Capacitor Selection

The energy transfer capacitors C_1 and C_2 are important elements in the proposed Cuk topologies since their values greatly influence the quality of input line current. Capacitors C_1 and C_2 must be chosen such that their steady-state voltages follow the shape of the rectified input ac line voltage waveform plus the output voltage with minimum switching voltage ripple as possible. Also, the values of C_1 and C_2 should not cause low-frequency oscillations with the converter inductors. In a practical design, the energy transfer capacitors C_1 and C_2 are determined based on inductors L_1, L_0 values (assuming $L_1 = L_2$ and $L_{01} = L_{02} = L_0$) such that the resonant frequency (f_r) during DCM stage is higher than the line frequency (f_1) and well below the switching frequency (f_s). Thus,

$$f_1 < f_r < f_s \qquad (10)$$

where

$$f_r = \frac{1}{2\pi\sqrt{C_1(L_1+L_2)}} \qquad (11)$$

On the other hand, the output capacitor C_0 needs to be sufficiently large to store minimum energy required for balancing the difference between the time varying input power and constant load power. The low-frequency peak–peak output voltage ripple is given by

$$\Delta V_0 = \frac{1}{C_0} \int_{T_L/8}^{3T_L/8} [i_{L01} - I_0]dt \qquad (12)$$

where I_0 is the output load current, and i_{L01} represent the average output inductor current over one switching cycle and it is given by

$$i_{Lo1} = \frac{V_{ac}^2}{R_e V_0} \qquad (13)$$

Substituting (12) into (13) and evaluating (13), the capacitor ripple equation is obtained as follows:

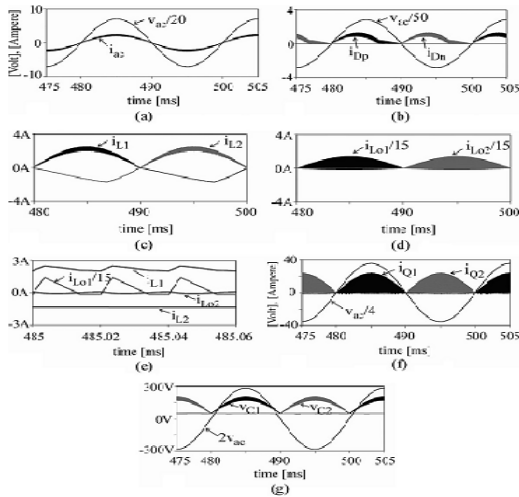$$\Delta V_0 = \frac{V_0}{\omega R_L C_0} \qquad (14)$$

Fig. 5 Simulation waveform

III. FUZZY LOGIC CONTROLLER DESIGN

In this section, the fuzzy control fundamentals will be outlined first. Afterward, the modified design of the proposed Bridgeless Cuk converter for PFC applications will be described in detail.
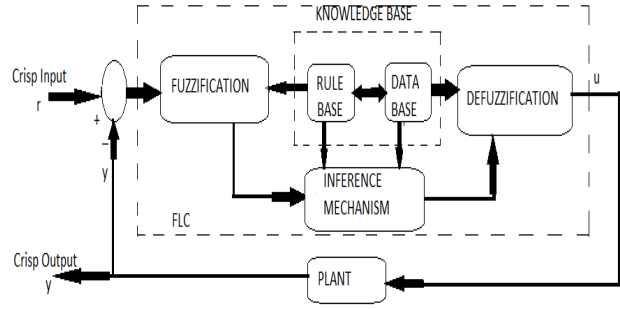

Fig. 6 Basic structure of fuzzy logic system

A. Fuzzy Control Philosophy

A basic FLC system structure, which consists of the knowledge base, the inference mechanism, the fuzzification interface, and the defuzzification interface, is shown in Fig. 3. Essentially, the fuzzy controller can be viewed as an artificial decision maker that operates in a closed-loop system in real time. It grabs plant output $y(t)$, compares it to the desired input $r(t)$, and then decides what the plant input (or controller output) $u(t)$ should be to assure the requested performance. The inputs and outputs are "crisp." The fuzzification block converts the crisp inputs to fuzzy sets, and the defuzzification block returns these fuzzy conclusions back into the crisp outputs.

B. Overview of FLC for Bridgeless Cuk Converter

Fuzzy logic is widely used in various fields. Most control situations are more complex than we can deal with mathematically. A bridgeless single-phase ac–dc Power Factor Correction rectifiers with Fuzzy Logic Controller based on Cuk topology. In this situation fuzzy control can be developed, provided a body of knowledge about the control process exists, and formed into number of fuzzy rules, the error e and change of error Δe are used as the input variables, which are defined as,

$$e(k) = r(k) - y(k) \qquad (15)$$

$$\Delta e(k) = e(k) - e(k-1)$$
$$= y(k-1) - y(k)$$

$$\text{if } r(k) = r(k-1) \qquad (16)$$

where r and y denote the reference command and plant output, respectively. Indices k and k −1 represent the current and previous states of the system, respectively. The controller output is the incremental change of the control signal $\Delta u(k)$. The control signal can be obtained by

$$u(k) = u(k-1) + \Delta u(k) \qquad (17)$$

The UOD in all membership functions of the controller inputs, i.e., *e* and *Δe*, and output, i.e., *Δu*, are defined on the normalized domain *[0, 1]*, as shown in Fig. 6. The linguistic values NB, NS, ZE, PS, and PB stand for negative big, negative small, zero, positive small, and positive big,

respectively. Then, the UOD for the gain updating factor α (which is utilized to fine tune the output) is normalized over the interval [0, 1], as shown in Fig. 7. Here, except for the two fuzzy sets at the outmost ends (trapezoidal MFs are considered), symmetric triangles with equal bases and 50% overlap with adjacent MFs are chosen. The SFs Ge, $G\Delta e$, and $G\Delta u$, which perform the specific normalization of input and output variables, play a role equivalent to that of the gains of a conventional controller. Hence, they hold the dominant impact on controller stability and performance.
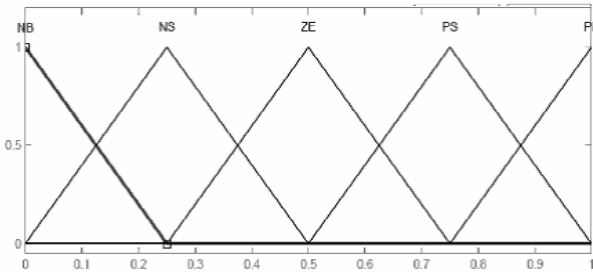

Fig. 7 Membership functions of e, Δe, and Δu.

TABLE I
RULE BASE FOR DERIVING FUZZY OUTPUT VARIABLE Δu

E		NB	NS	ZE	PS	PB
Δe	o/p					
NB		NB	NB	NM	NS	ZE
NS		NB	NS	NS	ZE	PM
ZE		NB	NS	ZE	PS	PB
PS		NM	ZE	PS	PS	PB
PB		ZE	PS	PM	PB	PB

The MFs for both normalized inputs (eN and ΔeN)and output (ΔuN) of the controller have been defined on the normalized domain $[0,1]$. For conventional FLCs, the controller output (ΔuN) is mapped onto the respective actual output (Δu) domain by the output SF $G\Delta u$. On the other hand, the actual output of the self tuning FLC is obtained by using the effective SF $\alpha G\Delta u$. Hence, adjusting the SFs can modify the corresponding UODs of the control variables. The adequate values of the input and output SFs can be derived based on the professional experience from the plant under control. It can also be derived through trial and error to achieve the best acceptable control performance. The relationships between the SFs and the input and output variables of the STFC can be expressed as follows:

$$eN=Ge \cdot e \tag{18}$$

$$\Delta eN =G\Delta e \Delta e \tag{19}$$

$$\Delta u=(\alpha G\Delta u)\Delta uN \tag{20}$$

IV. RESULTS

The converter has been simulated using PSPICE for the following input and output data specifications: vac =100 Vrms, Vo = 48V, Pout = 150W, and fs = 50 kHz.
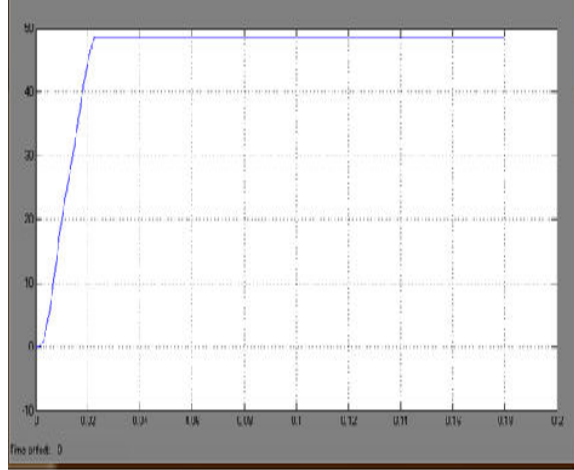

Fig. 8 Improved Efficiency Performance

V. CONCLUSION

In this paper, a bridgeless Cuk Converter using Fuzzy Logic Controller based on closed loop configuration are devised. The validity and improved performance of the proposed topologies are verified by simulation results. Due to the Power Factor Improvement, low harmonic distortion and slow response, the proposed topologies can further improve the conversion efficiency using Fuzzy Logic Controller when compared with the conventional Bridgeless Cuk PFC rectifier. Fuzzy Logic Controller with the self-tuning mechanism by altering a gain updating factor has been devised. Namely, to maintain the efficiency, the proposed circuits can operate with a higher switching frequency. Thus, additional reduction in the size of the PFC inductor and EMI filter could be achieved. The proposed bridgeless topologies can improve the efficiency by approximately 3-4% compared to the conventional PFC Cuk converter which shows very good stability and robustness.

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