A New Approach to Design an Efficient CIC Decimator Using Signed Digit Arithmetic

Vishal Awasthi, Krishna Raj

Abstract**—**Any digital processing performed on a signal with larger nyquist interval requires more computation than signal processing performed on smaller nyquist interval. The sampling rate alteration generates the unwanted effects in the system such as spectral aliasing and spectral imaging during signal processing. Multirate-multistage implementation of digital filter can result a significant computational saving than single rate filter designed for sample rate conversion. In this paper, we presented an efficient cascaded integrator comb (CIC) decimation filter that perform fast down sampling using signed digit adder algorithm with compensated frequency droop that arises due to aliasing effect during the decimation process. This proposed compensated CIC decimation filter structure with a hybrid signed digit (HSD) fast adder provide an improved performance in terms of down sampling speed by 65.15% than ripple carry adder (RCA) and reduced area and power by 57.5% and 0.01 % than signed digit (SD) adder algorithms respectively.

Keywords**—**Sampling rate conversion, Multirate Filtering, Compensation Theory, Decimation filter, CIC filter, Redundant signed digit arithmetic, Fast adders.

I. Introduction

In many applications of digital signal processing, it is necessary to process the data at more than one sampling rate. Multirate processing is basically an efficient technique for changing the sampling frequency of a signal digitally. The main advantage of a multirate system is the substantial decrease of computational complexity. The crucial role of multirate filtering is to enable the sampling rate conversion of the digital signal without significantly destroying the signal components of interest. The basic roles of Multirate filtering on modern signal processing systems have followed main directions.

(i) Firstly, the Multirate filtering is used for aliasing suppression and imaging removal in decimation and interpolation respectively.
(ii) Secondly, to solve filtering problems when a single filter operating at a fixed sampling rate is of significantly high order and suffers from output noise due to multiplication round-off errors and from the high sensitivity to variations in the filter coefficients.

The rapid development of the new algorithms and new design methods has been influenced by the advances in computer technology and software development. If the bandwidth of the signal $x[n]$ is larger than $1/N$ times the Nyquist interval, aliasing will occur. In order to retain the baseband spectrum and to reconstruct the analog signal, we would require an ideal lowpass filter with infinite attenuation and a perfect brick wall response with no transition gap between passband and stop band. Linear-phase FIR filters can work effectively in this contest that have either symmetric or antisymmetric impulse responses with a desire frequency deviation [1]. However, in many cases, the use of multistage/ Multirate techniques can yield FIR implementations that can compete (and even surpass) IIR implementations while retaining the nice characteristics of FIR filters such as linear-phase, stability, robustness to quantization effects, and good pipeline-ability.

A very effective way of improving the efficiency of filter designs is to use several stages connected in cascade (series) in which, first stage addresses the narrow transition band without requiring a high implementation cost and subsequent stages make-up for compromises to make the first stage to be efficient. There are an optimal number of stages which provide maximum computational savings.

E. B. Hogenauer [2] suggested a comb based filter known as cascade Integrator comb (CIC) filter for efficient down sampling or up sampling of any input signal with sampling rate F_s. This filter is a multiplierless filter, consisting of only adders and delay elements which is a great advantage when aiming at low power consumption. G. Jovanovic, Dolecek et al. [3] presented a new multiplier-free CIC-cosine decimation filter at the high input rate. Y. Djadi, et al. [4] designed a programmable decimation and interpolation digital filter based on the CIC structure. The circuit was configurable as either a decimation filter or an interpolation filter and the conversion ratio was programmable to any integer value from 10 to 256. Yonghong G. et al. [5] presented partial-polyphase architecture for CIC decimation filters based on the partial-polyphase decomposition and parallel processing techniques. Designed filters can operate at much lower sampling rate and still achieve the same performance as Hogenauer's CIC filters. This new architecture has advantages in high speed operation, low power consumption and low complexity for VLSI implementation. Alan Kwentus et al. [6] designed and fabricated a programmable CIC decimation filter in a 0.8 µm CMOS process whose decimation factor varied in power of two ranges of 2 to 1024. The integrator and comb stages were implemented using carry-save arithmetic in order to get high throughput. An improvement of a rational sampling rate converter based on stepped triangular comb filter is proposed in [7].

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The multiplier less CIC filter internal structure significantly uses addition operation to perform down sampling and the execution speed of an arithmetic operation is directly related to its chosen architecture and the number system employed to implement the architecture. Most of the hardware complexity is due to multipliers that leads excessive delay, area and power consumption even if implemented in a full-custom integrated circuits. The proposed concept is to use redundant signed digit number system arithmetic in the addition operation at bit level to make an improved, fast and efficient mechanism for signal rate alternation in CIC filter.

Fred Harris et al. [8] in 2009 proposed Simple multiplier free Sin based compensator with only two adders. The proposed method is computationally efficient and less complex. G. J. Dolecek et al. [9], designed a multiplierless CIC compensation filter based on the 2*M*-order filter and the sharpening technique. This technique attempts to improve the pass band and the stop band of a symmetric nonrecursive filter using the multiple copies of the same filter. J. Dolecek et al. [10], [11] proposed an efficient technique to design an economical recursive generalized comb filter (GCFs). This technique quantizes the multipliers in the z-transfer function employing power-of-2 terms.

The computational speed of the arithmetic operation can further increase by speedup techniques (Carry Skip and Carry Select) and anticipation techniques (Carry Look Ahead, Brent and Kung). The carry propagation can again speed-up by the use of faster logic circuit technology, forecasting logic and by carry free addition algorithm.

A ripple carry adder is a simple adder composed of a chain of full adders connected in series so that the carry propagates through every full adder before the addition is complete. Oklobdzija and Barnes proposed a variable skip group scheme to optimize the delay of critical carry signal [12]. A common approach to the design an efficient adder is hybrid adders that choose one method for carry propagation and another method for sum calculation such as Kogge and Stone proposed a general recurrence scheme for parallel computation [13]. King Stone structure is very attractive to generate intermediate carries but requires a higher area and power. An improved version of conventional carry-lookahead adder is proposed by Ling [14]. This approach is faster, less expensive and generally implemented through BiCMOS technology which results in a much cheaper operation. Robertson [15] and Avizienis [16] suggested a set of arithmetic rules for redundant signed digit numbers. Takaji and Yazima [17] proposed a high-speed algorithm suitable for VLSI implementation using RBSD numbers. A carry select addition technique was presented [18] by O. J. Bedrij. Changes at all levels are required to have a higher performance design since the clock frequency and power consumption doubles every two years. In this paper, we presented an efficient CIC decimator using signed digit adder algorithm for sample rate conversion with high speed and lower cost in terms of area and power.

The rest of the paper is organized as follows. Basic theory of Multirate decimation and interpolation with a brief description of special Multirate filters is presented in Section II. Some advance compensation techniques and open issues related to efficiently structure is given in Sections III and IV respectively. Section V presents the previous work related to the proposed structure. Section VI describes the proposed approach to design an efficient decimator using signed digit arithmetic. Performance analysis of designed compensated CIC decimation filter with different fast adder algorithm is mentioned in Section VII. A brief discussion and conclusions are drawn in Section VIII and finally, Section IX discusses the directions for further work.

II. Multirate Decimation and Interpolation Theory

In a sampled signal, some amount of excess bandwidth is present to compensate the aliasing that occurs in the transition band so that it does not affect the application. An optimal equiripple filter requires more multipliers if we do not take advantage of the symmetry in the filter coefficients [1]. The Multirate implementation yields a Multirate-multistage design which low pass filters data while decreasing the sampling rate at each stage for maximum computational efficiency. In many applications, if a very narrow transition width is required relative to the sampling frequency, we lower the sampling rate in stages by using simple low pass filters until we achieve a rate at which the required transition width is not large relative to such rate. Then we design a filter that provides the required transition.

Widely used decimation and interpolation filters are one of the basic building blocks of a sampling rate conversion system that performs two operations: low-pass filtering as well as up/down-sampling. Decimation filter (Decimator) converts the low resolution high bit-rate data to high resolution low frequency data along with removing quantization noise whereas interpolation filter (interpolator) converts high resolution low bit-rate data to low resolution high frequency data respectively. During this conversion process, down-sampling is affected by aliasing whereas up-sampling produces the unwanted spectra in the frequency band of interest, respectively. Hence, decimation has to be performed in such a way that avoids the effects of aliasing, which occurs when the highest frequency in the spectrum of a down-sampled signal w_H exceeds the value π/N.

When constructing a Multirate system for fast decimation process, it is desirable to form an efficient implementation structure that permits the arithmetic operation to be evaluated at lower possible sampling rate with higher speed. In a decimator, filtering has to prevent aliasing before the down-sampling while an interpolator, to remove images produced by the up-sampling operation. Obviously, the efficiency of the sampling rate converters may be improved if fast down-sampling (up-sampling) operations are incorporated into the filter structure and hence, the expected properties of the new structure are twofold: (i) the arithmetic operations are to be evaluated at the lower sampling rate with high speed, and

(ii) the modification of the structure does not affect the overall performance of the decimator (interpolator).

A. Special Multirate Filters: Nyquist, Farrow and Comb-Based Filters

Nyquist and Farrow filters are a special class of filters which are useful in multirate implementations. Nyquist filters are used for pulse shaping the signal whereas Farrow filter can be used effectively for both fractional advances/delays and changing the sampling rate of signals by arbitrary factors. Nyquist filters are well-suited for either decimation or interpolation. Nyquist and Farrow filter highly desirable for multistage designs as it has a very small passband ripple even when the filter is quantized for fixed-point implementations and to change the sampling-rate of a signal by an irrational factor without adding complexity in terms of the number of coefficients respectively.

Comb filters are also a special class of multirate filter, that consists of an integrator block working at the oversampled frequency F_s, a clock divider for a rate reduction and a differentiator block working at F_s/k, where k is the decimation ratio. Comb filters are developed from the structures based on the moving average (boxcar) filter. These comb-based filters can be implemented without multipliers due to unity-valued feedback coefficients. Hence, this filter class is suitable for a single-chip VLSI implementation that can operate at high frequencies.

In decimation, CIC filters are usually used at the first stage of a multistage design. This is because at that stage the sampling-rate is the highest, making the multiplier less feature of CIC filters very attractive [2]. This is an attractive feature for certain hardware such as FPGAs and ASICs because multipliers take up quite a bit of the area and is difficult to make to operate at very high clock rates. However, the disadvantage of a CIC filter is that the response of the CIC filter provides a poor lowpass characteristic, which is undesirable in many applications. Fortunately, this problem can be alleviated by a compensation filter. The only way for CIC filters to work is by using fixed-point arithmetic (with overflows wrapping). CIC filters have been constructed by adding a pole and a zero at z = 1. This pole/zero pair should cancel, yielding the traditional FIR transfer function.

The basic concept of a comb-based decimator is explained in Fig. 1. Figure shows the factor-of-*N* decimator consisting of the *K*-stage CIC filter and the factor-of-*N* down-sampler. The CIC filter first performs the averaging operation then follows it with the decimation. The transfer function of the CIC filter on z-domain is given in (1):

$$H[z] = H[z]_I^K . H[z]_C^K = \frac{(1-z^{-N})^K}{(1-z^{-1})^K} = \left(\frac{1-z^{-N}}{1-z^{-1}}\right)^K \qquad (1)$$

For decimation by a factor of N, the original data must reside in a bandwidth given by $F_s/(2N)$, where F_s is the rate at which the original data was sampled. Thus, if the original data contains valid information in the portion of the spectrum beyond $F_s/(2N)$, decimation is not possible. CIC decimators are generally designed and implemented through pipelined structure to ensure high system clock frequencies.

B. Limitation of Multirate & Multistage Filtering

In spite of extremely efficient inherent multiplier less implementations of CIC filters, there are three main problems in the application of comb decimators and interpolators: (i) Register overflow due to the unity feedback in all integrator stages (ii) High power consumption at the integrator sections due to high sampling rate and (iii) The desired frequency response cannot be met in the majority of practical applications due to the dependency on decimation factor (*N)* and number of stage (K).

III. Advance Compensation Techniques

The decimated version of the CIC filtered signal shows significant overlap between spectral replicas with smaller gain and larger the droop in the passband of interest. CIC compensators are single-rate or multirate low pass filters that are used to compensate the passband droop in CIC filters. In the case of CIC interpolation, it is usually done to pre-equalize the droop in the prior stage while in decimation, it is done in post-equalizing stage to achieve frequency response correction. The motivation behind the compensation methods is to appropriately modify the original CIC characteristic in the pass band such that the compensator filter has as low complexity as possible. Hyuk Jun Oh and Yong H. Lee [19] used a simple interpolated second-order polynomial filter (ISOP) cascaded with a CIC decimation filter to effectively reduce the pass band distortion caused by CIC filtering with little degradation in aliasing attenuation. The various methods used for compensation of CIC decimation filter are as follows:

A. Cascading CIC Filter and FIR Filter

In the two-stage solutions of Fig. 2, the role of the CIC Decimator (interpolator) is to convert the sampling rate by the large conversion factor *N*, whereas the FIR filter that has a magnitude response, the inverse of the CIC filter, provides the desired transition band of the overall Decimator (interpolator) and compensates the passband characteristic of the CIC filter. Usually the CIC filter is followed by a second decimating lowpass filter stage whose decimation ratio is significantly smaller than that of the CIC stage (typically ≤ 16). The decimation factor of this second stage will determine the frequency at which the worst-case aliasing will occur and will also determine the edge frequency of the passband of interest, where the worst-case passband distortion will occur.

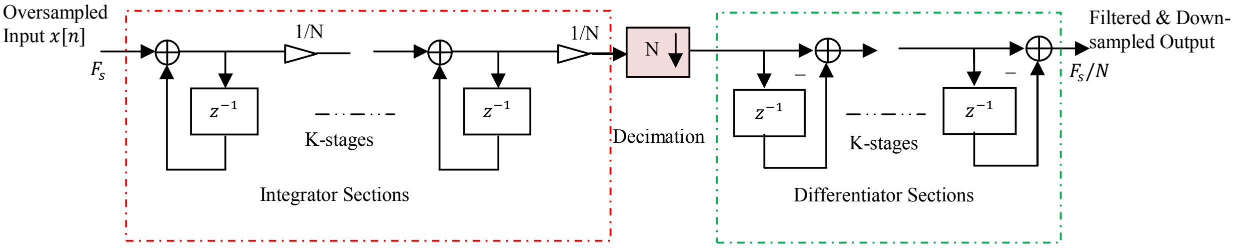

Fig. 1 Block diagram representation of CIC Decimator: Implementation structure consisting of the cascade of K integrators, down sampler, and the cascade of K differentiators

B. CIC Roll-off Compensation Filter

This compensation filter is like a channel selective filter having symmetrical characteristics in frequency response. This method compensated the roll off of the CIC filter in pass band by cascading CIC filter followed by a symmetric FIR filter with a minimum order [8]. The performance of CIC roll off compensation filter depends on the value of compensation filter coefficients, which is obtained by minimizing the corresponding error function. It is observed that if the frequency response characteristics of the received signal are used as a weighting function then the Roll off phenomenon of the CIC filter can exactly compensate. This method basically focused on compensating the slope of the pass band.

C. Compensated CIC-Cosine Decimation Filter

In this compensation method a second order compensator filter is introduced at low rate in order to improve the passband of interest of the overall filter. The coefficients of the compensator filter are presented in a canonical signed digit (CSD) form, and can be implemented using only adders and shifts [10], [20]. Transfer function and magnitude response of compensation filter are given by-

$$H_{comp}(z^M) = v + uz^{-N} + vz^{-2N} \quad (2)$$

$$\left|H_{comp}(e^{jNw})\right| = |2v\cos(Nw) + u| \quad (3)$$

where v & u real valued constant and N be decimation factor. In order to compensate the pass band droop (δ_c) at the cut off frequency, a compensated droop δ_{comp} is introduced whose value is reciprocal of δ_c. If the passband droop is within the desired limit then the transfer function of compensated filter can represented in canonical signed digit (CSD) arithmetic as:

$$H_{comp-CSD}(z^N) = x_{CSD} + y_{CSD}z^{-N} + x_{CSD}z^{-2N} \quad (4)$$

where x_{CSD} *and* y_{CSD} are the CSD representations of the quantized coefficients of the proposed compensation filter. The new value of δ_{comp} is further calculated until the desired pass band compensation is obtained.

IV. Open Issues

The previous section highlighted the different techniques to compensate the droop through the cascading of the CIC filter with FIR [3] and roll-off [8] at block level. A step towards efficient filtering is briefly addressed by Dolecek J. et al. [10] by using CSD in coefficient level. Polyphase structure, efficient sampling rate alternation and power & cost reduction are the key issues that require further exploration.

A. Polyphase Structures for Efficient Implementation

The polyphase decimators [21] used along with multirate multistage signal processing provides efficient decimation filter structures. In this structure, a down-sampler is used for further reduction of the sampling frequency in every stage of the filter and hence it reduces the hardware and power dissipation during the decimation process. However, it can introduce enough phase error if the signal sampling frequency is too low. To rectify such error, Hong-Kui Yang and W. Martin Snelgrove [22] decomposed the decimation ratio into two factors to implement a polyphase CIC decimation filter.

In polyphase decimators, the arithmetic units operate at all instants of the output sampling period, which is K times that of the input sampling period. Thus, the computational requirements of the overall structure for an *Nth*-order FIR filter are N multiplication and N – 1 addition. Thus, multirate multistage techniques employed along with polyphase decimate result in computationally efficient realizations. The major drawback of this technique is high power consumption in the Integrator stage when operating at high frequencies.

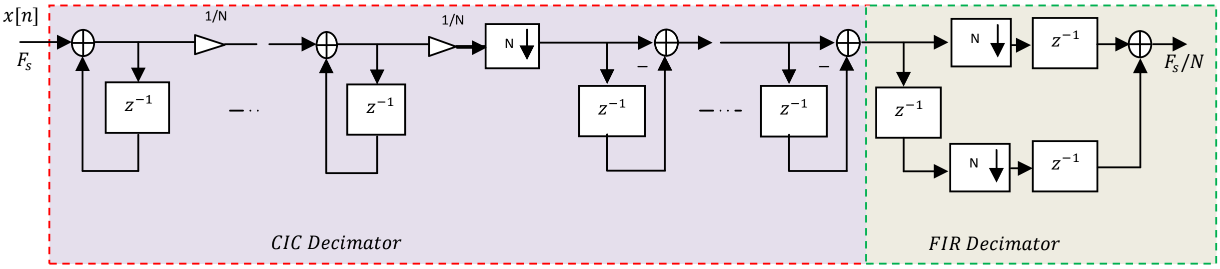

Fig. 2 Implementation structure of the two-stage Decimator composed of a CIC filter and an FIR filter

B. Two-Stage Sharpened Comb Filters & Modified Comb Zero-Rotation Approaches for Efficient Sampling Rate Alternation

Filter sharpening is a technique that improves passband/stopband filter performances with smaller passband error and greater stopband attenuation. Many attractive methods have been advanced to improve the frequency responses of comb-based decimators and interpolators [23]-[25]. Kaiser and Hamming [26] sharpened the magnitude response of a digital filter by using multiple realizations of a low-order basic filter where as Jovanovic-Dolecek et al. [7], [27] proposed a modified sharpening technique in which a sine-based compensation filter is introduced to decrease the passband droop of the original comb filter, and a cosine filter to improve the overall stopband characteristic. Kwentus, Jiang, & Willson [28], Laddomada & Mondin [29], and Laddomada [30] also proposed several attractive approaches for the comb filter sharpening.

To improve the stopband attenuation in the aliasing bands and to provide the maximum suppression of the quantization noise in the first decimation stage, a zero-rotation approach was proposed by Lo Presti [25] that was extended by Laddomada [29], [30]. In this approach, rotation of the natural nulls in the z-plane is applied to the comb filter sections and as a result, the new nulls placed are produced at the intervals of the comb filter natural nulls and each pair of new nulls is located symmetrically around the natural comb filter nulls. The zero-rotation approach considerably improves the ability of the modified comb filter to suppress aliasing in decimation, but the passband droop and implementation complexity are slightly increased.

V. Related Work

Various methods have been introduced that uses the non -recursive structure of a comb filter to reduce the power consumption as well as to increase the circuit speed.

- Kwentus et al. [28] outlined a method that uses the sharpening technique to decrease the passband droop and to increase the stopband attenuation at the high input rate and hence resulting higher power consumption. Presti L. L. [25] and Jovanovic et al. [7] discussed some methods to attain the desired low stopband attenuation by allowing the sharpening section to operate at the lower rate with the cost of the introduction of two multipliers working at a high rate.
- G. Javanovic Dolecek et al. proposed an efficient modification of the CIC cosine decimation filter [8] using canonical signed digits (CSD). In its proposed structure, a second order compensator filter is introduced at low rates to improve the passband and then the compensator filter coefficient is presented in a canonical signed digit (CSD) form but limiting with speed.
- A. Avizienis [16] present a fast parallel arithmetic using signed digit (SD) number representation which provides parallel carry free addition. In redundant signed digit number arithmetic, each digit can consider any one of three values $\{\bar{1}, 0, 1\}$ where $\bar{1} = -1$ and therefore a number can be represented in more than its base. Due to the presence of redundancy one can perform carry-propagation free addition and hence parallel addition of two redundant numbers in a constant time independent of the word length of operands.
- Phatak and Koren [31] presented an extension of SD number system arithmetic. They proposed a hybrid signed digit (HSD) adder algorithm in which instead of insisting every digit be a signed digit, some of the digits be signed and leave the others unsigned. This representation limits the maximum length of carry propagation chains to any desired value (d + 1), where d is the longest distance between neighboring signed digits. This number system opens an intermediate option between fully parallel carry free addition to desired length carry propagation addition.
- Khoo, K. Y. et al. [32] proposed an efficient architecture using a first carry-save integrator stage in a high-speed cascaded integrator-comb (CIC) decimation filter based on exploiting the carry propagation properties in a carry-save accumulator. A reduction of the number of registers by 6.3% to 13.5% is achieved by this architecture and therefore replacing a large number of full-adders by half-adders by 18% to 42%, thus saving area and power. Significant savings are achieved when the decimation rate is high and the number of integrator stages is small.
- Paper [33] presents a new multistage CIC-cosine decimation filter in which the cascade of expanded cosine pre-filters is added to improve the stop band CIC characteristic. The passband characteristic of this filter is improved by adding the simple 2M-order compensation filter. Resulting structure exhibits high aliasing attenuation and a low passband droop.

- Recently, in 2012, Pecotic, M.G. et al. [34] presented a method for the design of finite impulse response CIC compensators whose coefficients are expressed as the sums of powers of two (SPT). The proposed method is based on the minimax error criterion and to obtain the SPT coefficients, a global optimization technique based on the interval analysis is used.

VI. Proposed Approach to Design CIC Decimation Filter Using Signed Digit Arithmetic

As we already mentioned that the multipliers CIC decimation filter gives a high performance in terms of sampling rate conversion and hardware complexity in comparison to other digital filters but it fails to compensate the register overflow arise due feedback, high power consumption due to high sampling rate and desired frequency response due to passband droop. To tackle these issues, we propose the following mechanism:

(a) First, we compensate the passband droop by cascading CIC decimation filter with FIR filter. The selection of the order and number of stages of cascaded FIR filter should be optimum that gives a desired frequency response in the band of interest.
(b) Second, to avoid the register overflow at the integrator stage, we adopted the carry free signed digit addition algorithm. The adopted signed digit and hybrid signed algorithm limits the maximum length of carry propagation chain from fully parallel addition to any desired value.
(c) Third, we propose an efficient mechanism to design a Compensated CIC decimation filter in which the signed digit arithmetic is introduced to optimized the overall performance in terms of gate delay, hardware complexity and cost in comparison to other conventional adder algorithms.

A. Redundant Signed Digit (SD) and Hybrid Signed Digit (HSD) Adder Arithmetic

A symmetrical signed digit (SD) number can assume the following values i.e. $[-\alpha, \ldots, -1, 0, 1, \ldots, \alpha]$, where the maximum value of α must be within $[(r-1)/2] \leq \alpha \leq r-1$ range. For a digit set $[\alpha, \beta]$ of radix-r, the redundancy δ of the number system is defined as $\delta = \alpha + \beta + 1 - r$ where $\alpha + \beta + 1 \geq r$.

The addition here is done in two steps. In the first step, an intermediate sum s_i and a carry c_i is generated parallely for all digit position based on the operand digits m_i and n_i at each digit position i. In the second step, the summation $p_i = s_i + c_{i-1}$ is carried out to produce the final sum digit p_i. The most important fact is that it is always possible to select the intermediate sum s_i and carry c_{i-1} such that the summation in the second step does not generate a carry.

B. Rules for Selecting Intermediate Carry c_i and Sum s_i

Based On $\alpha_i = m_i + n_i$ for Radix r = 2b for SD and HSD Number System

The signed-digit positions generate a carry out and an intermediate sum based on two input signed digits i.e. m_i and n_i and the two bits at the neighboring lower order unsigned digit positions i.e. m_{i-1} and n_{i-1}.

(i) When both m_i and n_i is one then the intermediate carry c_i and the intermediate sum s_i is 1 and 0 respectively.
(ii) When both m_i and n_i is non-negative, only one input is non-zero and both m_{i-1} and n_{i-1} bits are non-negative, then the intermediate carry c_i and the intermediate sum s_i is 1 and $\bar{1}$ i.e. $\bar{b}$ respectively else 0 and 1 i.e. b.
(iii) When the addition of input bits m_i and n_i i.e. $\alpha_i = m_i + n_i$ is zero then the intermediate carry c_i and the intermediate sum s_i is 0.
(iv) When at least one input m_i or n_i is negative and zero and both m_{i-1} and n_{i-1} bits are non-negative, then the intermediate carry c_i and the intermediate sum s_i is 0 and $\bar{1}$ for SD algorithm and $\bar{1}$ and b for HSD algorithm else $\bar{1}$ and 1 for SD and 0 and $\bar{b}$ for HSD algorithm respectively.
(v) When both m_i and n_i is non-positive, then the intermediate carry c_i and the intermediate sum s_i is $\bar{1}$ and 0 respectively.

VII. Performance Evaluation

A. Simulation Setup

In this section, we study the block level structure of the proposed algorithm with its performance. Fig. 3 demonstrated the basic setup of CIC decimation filter with the inclusion of fast adder block replacing the adder block in basic CIC Decimator at Integrator section. This implemented structure enhances the filter performance in terms of down sampling speed and register overflow.

To implement this structure, we used FPGA Family: Virtex-5; Device: XC5vsx240T; Package: ff1738, which is a popular logic family in terms of high packing density, low power dissipation and high yield. Table I listed the different parameters used to setup this efficient structure. The overall operation is analyzed in terms of the gate delay, area on silicon wafers and cost in terms of the product of available on chip leakage power i.e. 3.303 W and area with the variation of number of bits.

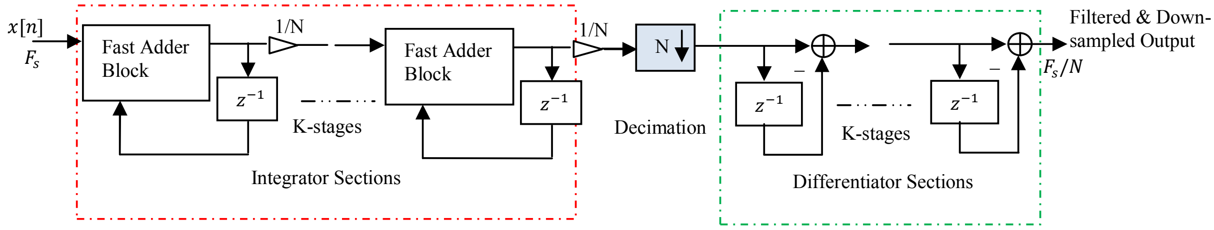

Fig. 3 Block level structure of CIC decimation filter

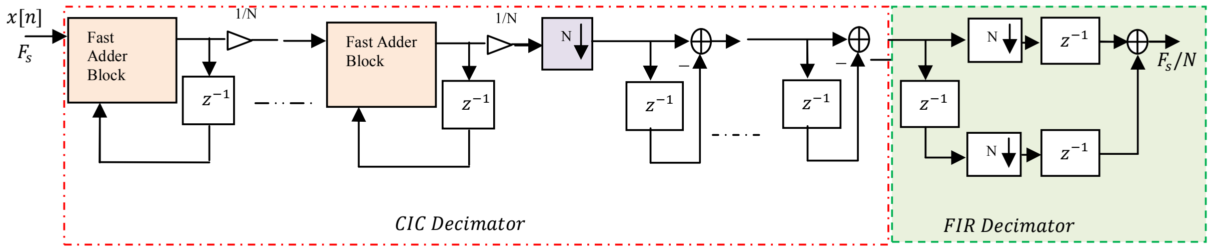

Fig. 4 Block level structure of the CIC Compensator filter composed of a CIC decimator and an FIR decimator

This proposed structure is efficient in terms of down sampling speed but still limiting with its passband droop and thus to compensate this droop, we implemented a CIC compensator by cascading the proposed Decimator with FIR Decimator as demonstrated in Fig. 4.

TABLE I
THE SIMULATION PARAMETERS

Simulation Parameters	Values
Oversampled input signal rate	1. 28 MHz
Downsampled output signal rate	20 KHz
Passband ripple (peak to peak)	0.01 dB
Decimation factor	64
Input wordlength	18, 20 & 22 bits
Output wordlength	20
No. of stage of CIC decimator	1
Decimation factor of FIR decimator	8
Number system adopted	Signed & Hybrid Signed digit

B. Simulation Results

Fig. 5 and Table II presented the overall magnitude response of the single stage CIC filter and compensated CIC filter respectively. In these figures, we observe clearly that the passband droop is improved. We obtain 84.07% improvement with single stage FIR compensation and 83.79% improvement in two stage FIR compensation. Figs. 5 (b) & (c) show the passband of the overall decimator and shows how the droop in the passband has been equalized.

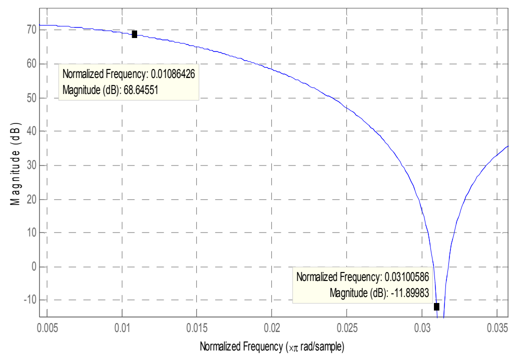

Fig. 5 (a) Single CIC Stage ($N = 64$)

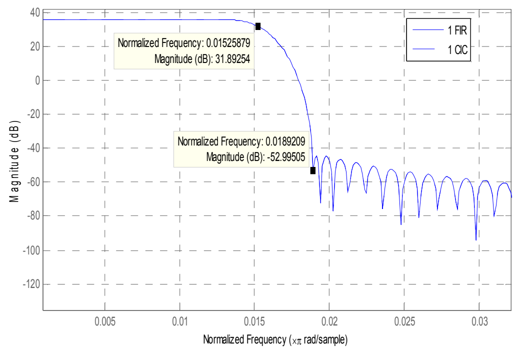

Fig. 5 (b) One CIC filter with one FIR filters (8×8)

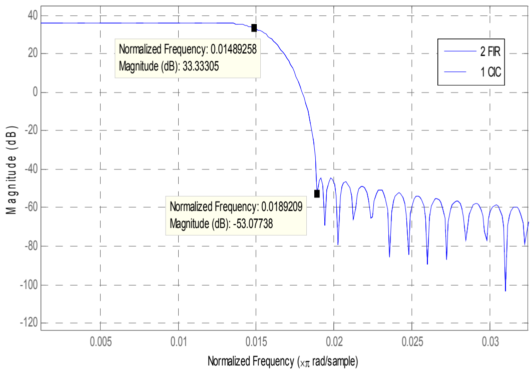

Fig. 5 (c) One CIC filter with two FIR filters $(8 \times (4,2))$

TABLE II
PASSBAND-DROOP COMPENSATION CHART

Filter Stages with decimation factor = 64	Magnitude (dB) of Passband droop at Normalized Frequency $(\times \pi \frac{rad}{sample})$						
	0.005	0.0075	0.01	0.0125	0.015	0.0175	0.02
Single stage CIC filter	69.79	69.05	68.83	67.61	65.12	62.79	58.23
Compensated CIC with one FIR filter stage	37.21	37.21	37.21	36.73	32.11	16.62	-43.18
Compensated CIC with two FIR filter stage	37.21	37.21	37.21	36.85	33.13	5.83	-44.21

Next, Fig. 6 represented the gate delay, area on silicon wafers and cost in terms of product of On-chip leakage power and area respectively of fast adder algorithms i.e. RCA, SD and HSD with the variation of number of bits. Through the comparison, it is observed that with the variation of number of bits, the gate delay of RCA is increasing faster by 41% with SD and 41.68% with HSD but limiting in terms of its area (no. of occupied slice) whereas the SD adder gives fast addition operation in constant time by 41% with RCA and 8.8% HSD but an area on silicon wafer is also increasing with faster rate and therefore it cannot be used for optimum design where both time and area are the major concern. The efficient HSD adder algorithm is an optimum algorithm in which it initially requires slight higher gate delays in addition but becomes constant as the number of bits increases (≥ 16 bit). HSD algorithm efficiently improves the gate delay by 65.15%, 41.68% and 24.24% with RCA and area by 56.92%, 51.06% and 52.85% with SD for 16, 32 and 64 bits respectively. The savings in the terms of slice and no. of bonded IOBs are even higher if HSD utilizes the longer signed digit spacing such as $d > 1$. Looking at the results from the cost function, we can see that while the gate delay of SD is almost constant (lower than a single-rate design) w.r.t. HSD, the cost has been reduced substantially by 51.06 %.

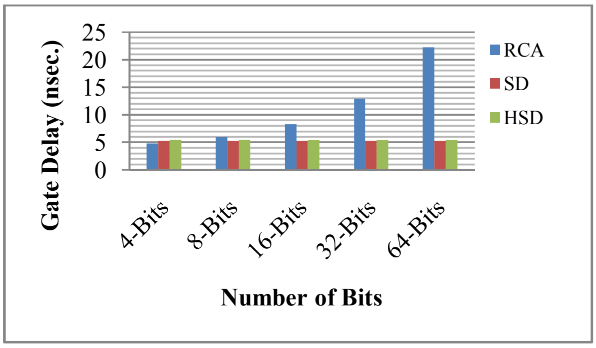

Fig. 6 (a) Gate Delay of fast adders

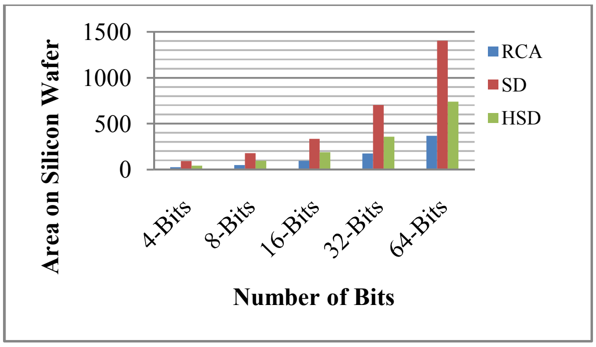

Fig. 6 (b) Area on Silicon Wafer of fast adders

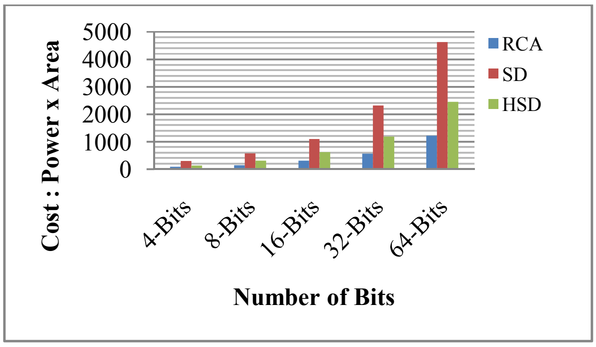

Fig. 6 (c) Cost: Power × Area of fast adders

After the proper analysis and comparison of fast adder algorithms, we introduced these algorithms in compensated CIC filter structure for 18, 20 and 22 bit word length as shown in Fig. 7. It is found that the proposed compensated filter structure using hybrid signed digit arithmetic is more efficient in terms of the gate delay by 38.6%, area by 57.5% and On chip leakage power by 0.1% with SD and hence an overall performance of compensated CIC filter with HSD algorithm technique results improvement in terms of gate delay, area and power respectively.

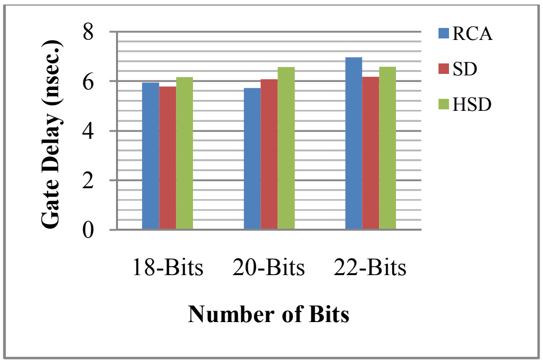

Fig. 7 (a) Gate Delay of Compensated CIC filter with fast adder algorithms

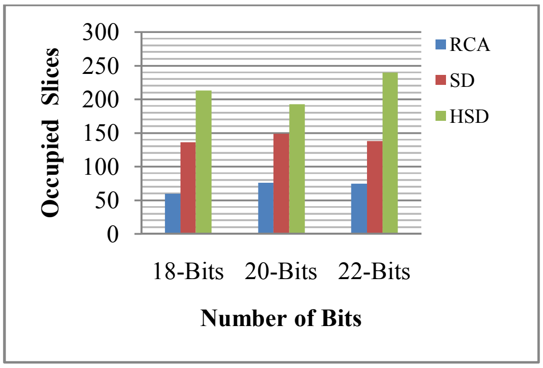

Fig. 7 (b) Number of Occupied Slices of Compensated CIC filter with fast adder algorithms

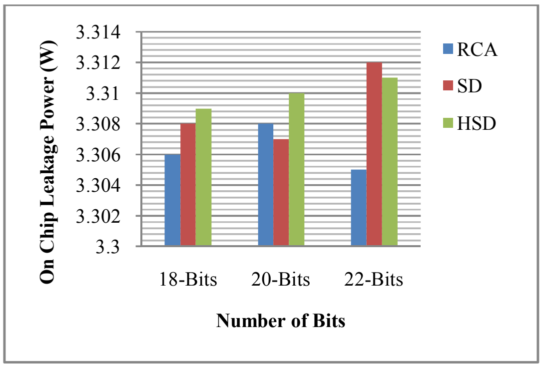

Fig. 7 (c) On Chip Power Leakage (W) of Compensated CIC filter with fast adder algorithm

This proposed filter results a trade-off between the desired compensation of the passband droop with area and speed. The width of the passband and the frequency characteristics outside the passband are severely limited. Additionally, using the polyphase decomposition, the filters at the first stage can be moved at the lower rate and by increasing the number of stages, the amount of passband aliasing or imaging error can be brought within the required ranges.

VIII. Discussion and Conclusion

Digital computer arithmetic is an aspect of logic design with the objective of developing appropriate algorithms in order to achieve an efficient utilization of the available hardware. HSD representation is very flexible and offers a wide variety of choices to the designer. Increasing d trades off higher delay with lesser area.

In this paper, we presented a new approach to design a Multirate-multistage CIC decimation filter using fast adder algorithms to achieve efficient performance in terms of speed, area and power. CIC filters are very economical, computationally efficient and simple to implement in comparison to FIR or IIR filter for large rate change. The proposed compensated CIC decimation filter initially compensated the passband droop by 84.07% than CIC filter and then with HSD algorithm, it achieves high throughput in terms of down sampling speed by 65.15% than RCA, area and power by 57.5% and 0.01% than SD algorithms respectively. This newly designed structure provides an optimum solution for all signal processing applications which require sampling rate conversion with higher speed and lesser area such as image and speech processing.

IX. Possible Future Scope in Signal Processing Through Signed Digit Arithmetics

So far, the work which has been done leaves a wide scope of signed digit arithmetic in algorithm level, architecture level and implementation level in the signal processing area. Implementations of CIC filter, based on the hybrid signed digit fast adder algorithm, yield fast and compact structure at the cost of few more CLB's than SD adder. This optimum adder design requires a small area with low power consumption. This representation also arises more flexibility by combining the variants of the other fast parallel adder (CSA, Ling etc.) with HSD to obtain more suitable implementations. The area is still wide open to use this algorithm in the field of digital filtering, image processing etc. to accelerate the other arithmetic operations such as multiplication, division and floating-point arithmetic functions to limit carry propagation according to the requirement of applications.

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