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Analytical Subthreshold Drain Current Model Incorporating Inversion Layer Effective Mobility Model for Pocket Implanted Nano Scale n-MOSFET

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Abstract—Carrier scatterings in the inversion channel of MOSFET dominates the carrier mobility and hence drain current. This paper presents an analytical model of the subthreshold drain current incorporating the effective electron mobility model of the pocket implanted nano scale n-MOSFET. The model is developed by assuming two linear pocket profiles at the source and drain edges at the surface and by using the conventional drift-diffusion equation. Effective electron mobility model includes three scattering mechanisms, such as, Coulomb, phonon and surface roughness scatterings as well as ballistic phenomena in the pocket implanted n-MOSFET. The model is simulated for various pocket profile and device parameters as well as for various bias conditions. Simulation results show that the subthreshold drain current data matches the experimental data already published in the literature.

Keywords—Linear Pocket Profile, Pocket Implanted n-MOSFET, Subthreshold Drain Current and Effective Mobility Model.

I. Introduction

As the channel length of MOSFETs is scaled down to deep-submicrometer or nano scale regime, we observe the reduction of threshold voltage with the reduction of channel length [1]. This effect is known as short-channel effect (SCE). It can be reduced or can even be reversed (then it is called reverse short channel effect or RSCE) by locally raising the channel doping near source and drain junctions. RSCE was originally observed in MOSFETs due to oxidation-enhanced-diffusion [2] or implant-damage-enhanced diffusion [3]. Lateral channel engineering utilizing halo or pocket implant [4]-[7] surrounding drain and source regions is effective in retarding SCE with the downsizing of the channel length of MOSFETs. In fact, this pocket implant technology is found to be very promising in an effort to tailor the short channel performances of deep-submicron as well as nano scale MOSFETs [8]-[9]. It could be shown that with an optimized pocket implant process the saturation current is up to 10% higher compared to a conventional optimized junction technology without increasing the leakage current of the devices having minimum channel length [10].

The subthreshold region is particularly important for low-voltage, low-power applications, such as, when the MOSFET is used as a switch in digital logic and memory applications, because the subthreshold region describes how the switch turns on and off. Already few papers have been published focusing on subthreshold behavior of pocket implanted n-MOSFET [7], [11]-[13]. In [7], models for subthreshold and above subthreshold currents in 0.1 μm pocket n-MOSFETs for low-voltage applications have been derived based on the diffusion current transport equation. But this model characterizes the localized pile-up of channel dopants as step profile. A channel length independent subthreshold characteristic in submicron MOSFETs has been reported by Shin et al in [11] due to the presence of localized pileup of channel dopants near the source and drain ends. An analytical subthreshold current model for pocket implanted n-MOSFETs has been presented in [12]. But this model characterizes the localized channel dopants as step profile. In [13], the authors showed an analytical model that the subthreshold current of n-MOSFETs, which is mainly due to diffusion, is determined by the internal two-dimensional hole distribution across the device.

The inversion layer mobility in Si MOSFET's has been a very important physical quantity as a parameter to describe the drain current and a probe to study the electric properties of a two-dimensional carrier system. In an earlier work, the effect of this quantity on subthreshold drain current has not been included [14]. But it has already been reported that the electron and hole mobilities in the inversion layer on a (100) surface follow the universal curves at room temperature independent of the substrate impurity concentration or the substrate bias when plotted as a function of effective normal electric fields, $\mathscr{E}_{eff}$ [15]. Since the use of pocket implants causes a strong non-uniform lateral doping profile and with the reduction of channel length or with the increase of pocket profile parameters, there is a pronounced increase of the effective channel doping concentration, the effective mobility is supposed to be degraded further due to Coulomb scattering with the ionized dopants and charged interface traps at low vertical electric fields i.e. at low gate bias. This is called roll-off region. As the effective vertical electric field increases, the mobility becomes independent of the channel doping and all the samples approach the so-called 'universal curve'. In this region, the main scattering processes are phonon and surface roughness scattering that do not depend on channel doping. In most circuit models [16]-[18], simple mobility models [19], [20] are used to describe the effective surface mobility neither accounting for the degradation by Coulomb scattering in heavily doped MOSFET's (only the so called 'universal curve' [21] is modeled) nor accounting for the lateral non-uniform doping profile. This neglect can cause

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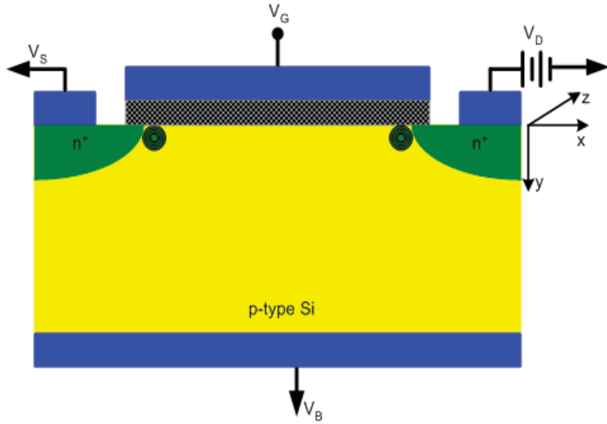

Fig. 1. Pocket implanted n-MOSFET structure

simulation errors in the transconductance of short channel pocket implanted n-MOS devices up to 50% which can not be tolerated in today's circuit simulations [10].

In this paper, an analytical subthreshold drain current model including the inversion layer effective mobility model is developed taking into account the pocket doping effects for the nano scale pocket implanted n-MOSFET. The model is developed using two linear pocket doping profiles. Threshold voltage, surface potential and inversion layer effective mobility models of the pocket implanted nano scale n-MOSFET are used from the published works in [9], [22] and [23] respectively. The pocket profile and device parameters as well as bias voltages are varied to investigate the pocket implantation effect on subthreshold drain current. As a verification of the mobility model, subthreshold drain current model is matched with the experimental data published in [11].

II. Modeling of Pocket Doping Profile

The pocket implanted n-MOSFET structure shown in Fig. 1 is considered in this work and assumed co-ordinate system is shown at the right side of the structure. Localized extra dopings are shown by circles near the source and drain side regions. All the device dimensions are measured from the oxide-silicon interface. In the structure, the junction depth (r_j) is 25 nm. The oxide thickness (t_{ox}) is 2.5 nm, and it is SiO_2 with fixed oxide charge density of 10^{11} cm^{-2}. Uniformly doped p-type Si substrate is used with doping concentration (N_{sub}) of 4.5×10^{17} cm^{-3} with pocket implantation both at the source and drain sides with peak pocket doping concentrations from 1.5×10^{18} cm^{-3} to 2.5×10^{18} cm^{-3} and pocket lengths from 20 to 30 nm, and source or drain doping concentration of 9.0×10^{20} cm^{-3}.

The pocket implantation, which causes the Reverse Short Channel Effect (RSCE), is done by adding impurity atoms both from the source and drain edges. It is assumed that the peak pocket doping concentration (N_{pm}) gradually decreases linearly towards the substrate level concentration (N_{sub}) with a pocket length (L_p) from both the source and drain edges. The basis of the model of the pockets is to assume two laterally linear doping profiles from both the source and drain edges across the channel as shown in Figs. 2-3 for substrate concentration of 4.5×10^{17} cm^{-3} and channel length of 100 nm. The pocket parameters, N_{pm} and L_p, play important role in determining the RSCE.

At the source side, the pocket profile is given as

$$N_s(x) = -\frac{N_{pm} - N_{sub}}{L_p}x + N_{pm}$$

$$N_s(x) = N_{sub}\frac{x}{L_p} + N_{pm}\left(1 - \frac{1}{L_p}x\right) \tag{1}$$

At the drain side, the pocket profile is given as

$$N_d(x) = \frac{N_{pm} - N_{sub}}{L_p}\left[x - (L - L_p)\right] + N_{sub}$$

$$N_d(x) = N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p}\right) + N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p}x\right) \tag{2}$$

,where x represents the distance across the channel. Since these pile-up profiles are due to the direct pocket implantation at the source and drain sides, the pocket profiles are assumed symmetric at both sides. With these two conceptual pocket profiles of equations (1) and (2), the profiles are integrated

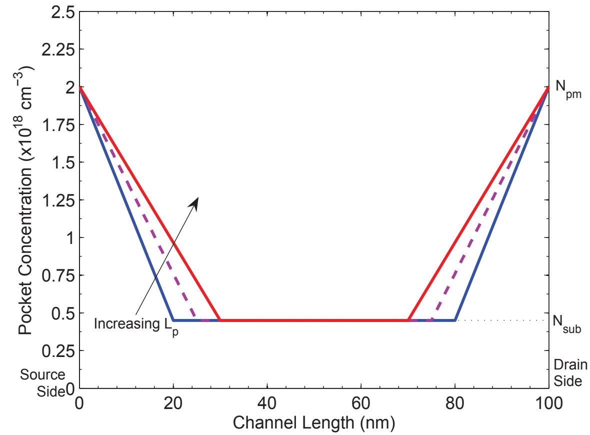

Fig. 2. Simulated pocket profiles at the surface for different pocket lengths, L_p = 20, 25 and 30 nm; peak pocket concentration, N_{pm} = 2.0×10^{18} cm^{-3}

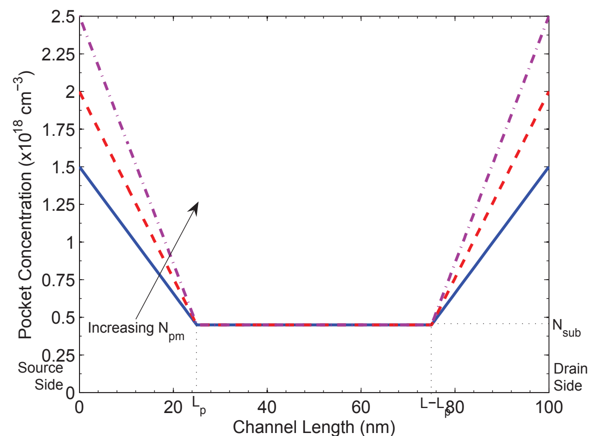

Fig. 3. Simulated pocket profiles at the surface for various peak pocket concentrations, N_{pm} = 1.5×10^{18}, 2.0×10^{18}, 2.5×10^{18} cm^{-3}; pocket length, L_p = 25 nm

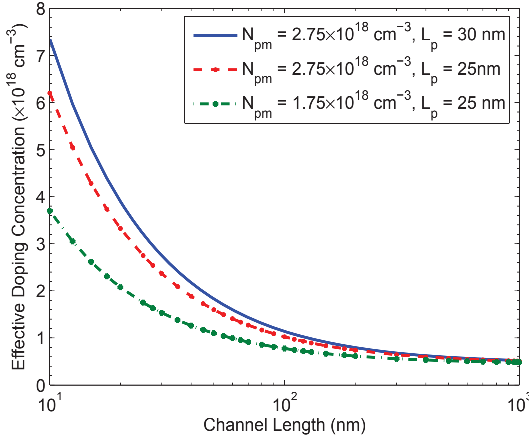

Fig. 4. Simulated effective pocket doping concentration vs. channel lengths at the surface for different peak pocket concentration and pocket lengths with substrate concentration, $N_{sub} = 4.5{\times}10^{17}$ cm^{-3}

mathematically along the channel length (L) from the source side to the drain side and then the integration result is divided by L to derive an average effective doping concentration (N_{eff}) as shown in equation (3).

$$N_{eff} = \frac{1}{L}\int_0^L \Big[N_s(x) + N_d(x) + N_{sub}\Big]\mathrm{d}x \tag{3}$$

Putting the expressions of $N_s(x)$ and $N_d(x)$ from equations (1) and (2) in equation (3), the effective doping concentration is obtained in equation (4).

$$N_{eff} = N_{sub}\left(1 - \frac{L_p}{L}\right) + \frac{N_{pm}L_p}{L} \tag{4}$$

This effective doping concentration expression is then used in deriving the various models of the pocket implanted n-MOSFET. When $L_p \ll L$ for long channel device, the pocket profile has very little effect on uniform substrate doping concentration, but when L_p is comparable with L then the pocket profile affects the substrate doping concentration and hence other operational parameters of n-MOSFET to change due to RSCE. Because of the pocket implantation, effective doping concentration increases with decreasing channel lengths as observed in Fig. 4. This becomes stronger when both peak pocket concentration and/or pocket length increases.

III. Modeling of Subthreshold Drain Current

In the subthreshold regime, the n-MOSFET is in weak inversion or diffusion mode in which the electrons have to cross a potential barrier in the channel region. For a pocket implanted MOSFET, there can, in fact, be two barriers. Hence, conventional formulas for drain current in uniformly doped MOSFETs [24] are not applicable here. The subthreshold current has deleterious effects on the performance of digital circuits in terms of increased power dissipation and a possible shift in logic levels. An accurate estimation of the subthreshold behavior by means of physical modeling is therefore important for the device and circuit design.

The objective of this work is to develop a compact and physics based subthreshold drain current model for the pocket implanted nano scale n-MOSFET. Based on the drift-diffusion equation, the electron current density, J_n in an n-MOSFET can be written as in equation (5).

$$\begin{aligned} J_n &= q\left(-n\mu_{n,eff}\frac{d\psi_s}{dx} + D_n\frac{dn}{dx}\right) \\ &= qD_n\left(-\frac{n}{\phi_{th}}\frac{d\psi_s}{dx} + \frac{dn}{dx}\right) \end{aligned} \tag{5}$$

,where $\psi_s(x)$, ϕ_{th}, n, D_n and $\mu_{n,eff}$ are the surface potential (model is derived in [22]), thermal voltage, electron density, electron diffusion co-efficient and effective electron mobility respectively. ϕ_{th} is given by equation (6).

$$\phi_{th} = \frac{kT}{q} = \frac{D_n}{\mu_{n,eff}} \tag{6}$$

Multiplying equation (5) by an integrating factor of $e^{-\frac{\psi_s}{\phi_{th}}}$, the right hand side of equation (5) can be transformed into an exact derivative. Then using the surface potential model in [22], the electron current density equation (7) is found.

$$J_n = -qD_nN_{eff}\exp\Big(-\frac{\varphi_{bi} - V_{BS}}{\phi_{th}}\Big)\frac{\left(1 - \exp\left(-\frac{V_{DS}}{\phi_{th}}\right)\right)}{\int_0^L \exp\left(-\frac{\psi_s}{\phi_{th}}\right)dx} \tag{7}$$

The integral in the denominator of the right hand side of equation (7) is evaluated by using the numerical integration technique of multiple-segment Simpson's 1/3 rule and the surface potential model in [22]. The diffusion co-efficient for electron (D_n) in equation (7) has been evaluated by using the Einstein relation given in equation (6) and the effective electron mobility ($\mu_{n,eff}$) is obtained from [23]. Finally, the subthreshold drain current, I_{sub} in the channel is obtained by multiplying the electron current density, J_n and the channel cross-sectional area (which is the multiplication of the effective channel thickness, t_{ch} and the channel width, W) as given in equation (8).

$$I_{sub} = J_nWt_{ch} \tag{8}$$

The effective channel thickness, t_{ch} is given in equation (9). It is only valid when $(-\psi_s + V_{BS}) < V_{GT}/\theta$, i.e., in the weak inversion and the depletion regions. It can be obtained as the distance from the surface to the position along the y-direction where the electrostatic potential has changed by V_{th} [25]. When the gate voltage V_{GS} is in the close vicinity of the threshold voltage, the drain current (I_{ds}) becomes the subthreshold current (I_{sub}). By using Gauss's law, the vertical component of the electric field at the surface, V_{th}/t_{ch} is equal to Q_{dep}/ε_{Si} in the subthreshold region. Thus, the effective channel thickness is found in equation (9).

$$t_{ch} = V_{th}\sqrt{\frac{\varepsilon_{Si}}{2qN_{eff}(2\varphi_F - V_{BS} + V_{GT}/\theta)}} \tag{9}$$

,where $V_{GT} = V_{GS} - V_{th}$, θ is the subthreshold ideality factor reflecting the gate voltage division between the insulator capacitance and the depletion layer capacitance and φ_F is

the Fermi potential due to the pocket implantation given by equation (10). Threshold voltage, V_{th} is taken from [9].

$$\varphi_F = \frac{kT}{q} \ln \frac{N_{eff}}{n_i} \tag{10}$$

,where n_i is the intrinsic carrier concentration of Si.

IV. Results and Discussions

In order to verify the analytical subthreshold current model for the pocket implanted n-MOSFET, different types of simulations were performed. At first, surface potential model is simulated for various pocket profile parameters. In Figs. 5-6, it is observed that the surface potential increases with the decreasing peak pocket doping concentrations and pocket lengths respectively. Since when the peak pocket doping concentration or pocket length decreases the effective doping concentration also decreases. Thus drain current is affected.

Figs. 7-8 show the threshold voltage variation with gate lengths for different pocket doses and pocket lengths respectively. It has been observed that as the pocket dose or the pocket length is increased, the RSCE increases and thus delays the threshold voltage roll-off. Since the mobility is affected by the threshold voltage, therefore, variation of pocket dose or pocket length will cause the variation of the effective mobility.

Figs. 9-10 show that as the pocket dose and pocked length are increased the effective mobility degrades at low values of normal electric fields because of the increased Coulomb scattering rate due to the incorporation of more ions in the channel by the additional pocket dopants. But at the higher values of the effective normal electric field, there is no deviation in the effective mobility curve due to the change of pocket profile parameters. This holds the universality of the effective mobility curves.

In Figs. 11-13, subthreshold current variation for different gate voltages are shown for two different drain biases of 0.05 V and 2.5 V with different channel lengths of 0.25 μm, 100 nm and 50 nm. It is observed that for longer channel length

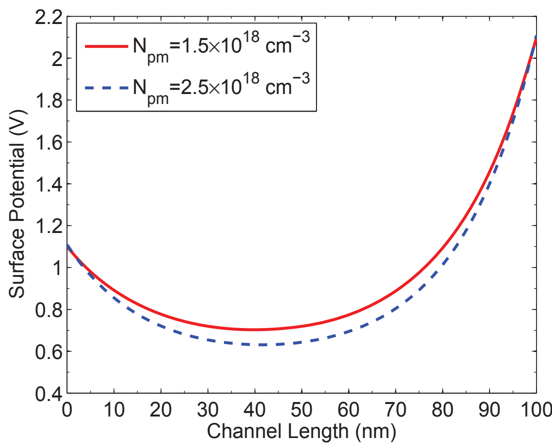

Fig. 5. Surface potential curves along the channel for various peak pocket doping concentration with $L = 100$ nm, $V_{BS} = 0.0$ V and $V_{DS} = 1.0$ V

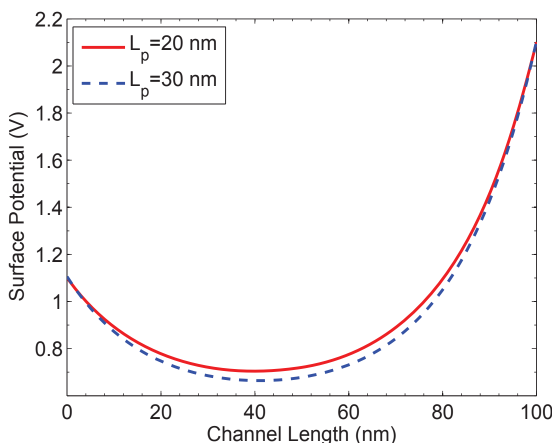

Fig. 6. Surface potential curves along the channel for various pocket lengths with channel length, $L = 100$ nm, substrate bias, $V_{BS} = 0.0$ V and drain bias, $V_{DS} = 1.0$ V

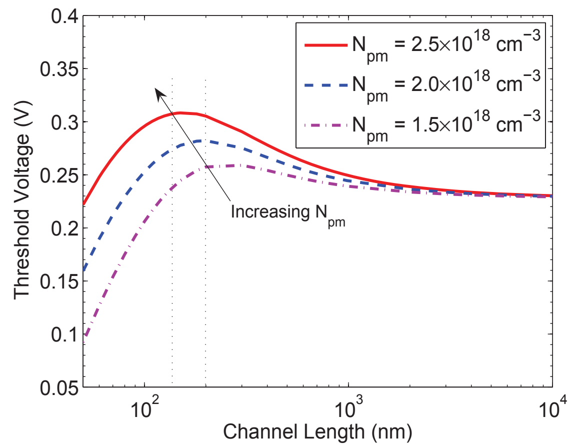

Fig. 7. Threshold voltage vs. channel length curves along the channel for various peak pocket doping concentrations with $V_{BS} = 0.0$ V, $V_{DS} = 0.05$ V and pocket length, $L_p = 25$ nm

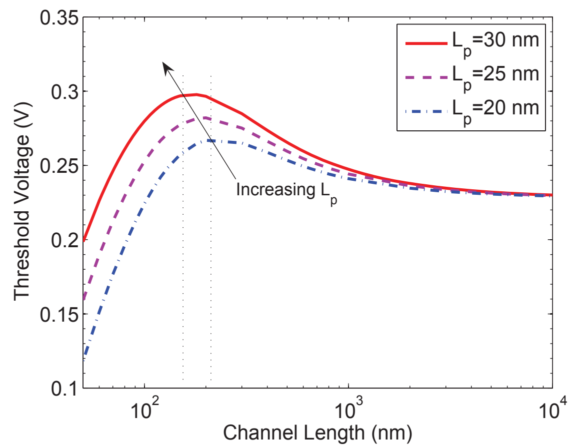

Fig. 8. Threshold voltage vs. channel length curves along the channel for various pocket lengths with $V_{BS} = 0.0$ V, $V_{DS} = 0.05$ V and and peak pocket doping concentration, $N_{pm} = 1.75 \times 10^{18}$ cm^{-3}

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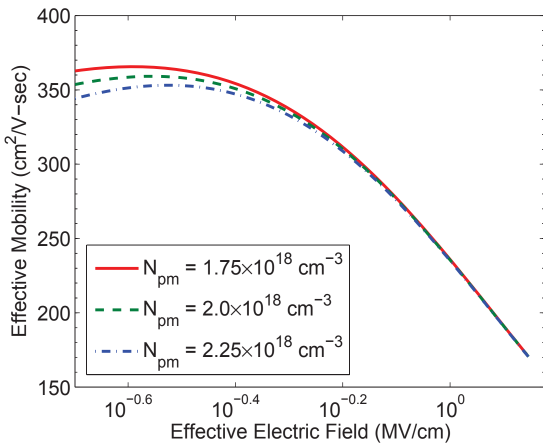

Fig. 9. Effective mobility vs. effective electric field for different peak pocket doping concentrations (N_{pm}) with $L = 0.1$ μm, $N_{sub} = 3.5{\times}10^{17}$ cm^{-3}, $L_p = 25$ nm, $V_{DS} = 0.05$ V, T = 300 K

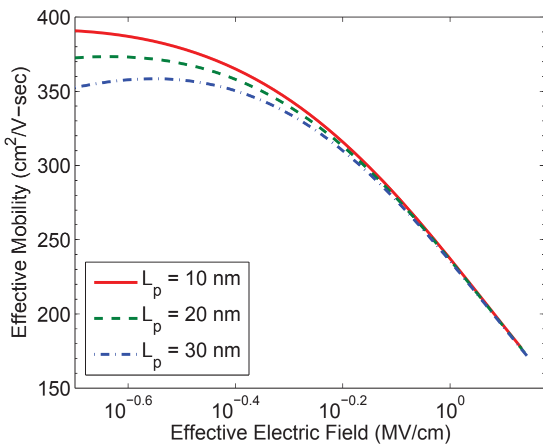

Fig. 10. Effective mobility vs. effective electric field for different pocket lengths (L_p) with $L = 0.1$ μm, $N_{sub} = 3.5{\times}10^{17}$ cm^{-3}, $L_p = 25$ nm, $N_{pm} = 1.75{\times}10^{18}$ cm^{-3}, $V_{DS} = 0.05$ V, T = 300 K

device, subthreshold current does not change appreciably as the drain bias increases, but for shorter channel length device, subthreshold current changes appreciably as the drain bias increases. This also occurs due to significant DIBL effect.

Figs. 14-16 show the variation of subthreshold current for a set of substrate biases (V_{BS}) of 0 V, -0.5 V and -1 V with different channel lengths (L) of 0.25 μm, 100 nm and 50 nm respectively and drain bias, $V_{DS} = 0.05$ V. It is observed that the subthreshold current decreases with increasing substrate bias in the negative direction for the same applied gate and drain biases. The results are in consistent with the substrate bias effect on subthreshold current found in the literature. But it has also been observed that the amount of current increment with increasing gate voltage is less, and the subthreshold slope decreases more rapidly as the gate voltage increases in the shorter channel length device.

Fig. 17 shows the variation of subthreshold drain current with gate voltage for three different oxide thicknesses (t_{ox}) of 1.5, 2.5 and 3.5 nm with peak pocket implant concentration,

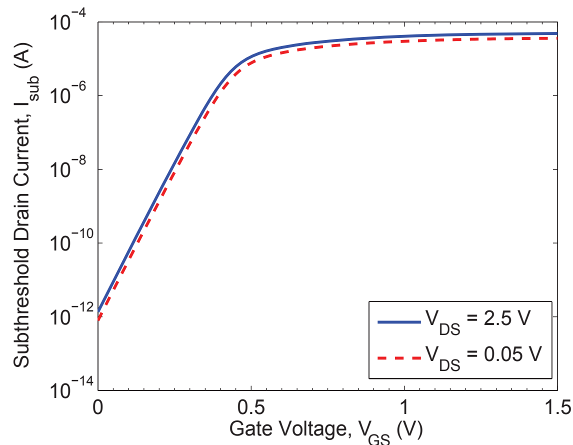

Fig. 11. Subthreshold drain current vs. gate voltage for two drain biases, $V_{DS} = 0.05$ V and $V_{DS} = 2.5$ V with $L = 0.25$ μm

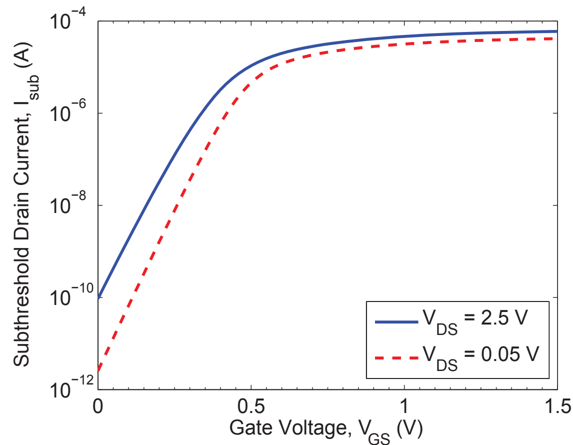

Fig. 12. Subthreshold drain current vs. gate voltage for two drain biases, $V_{DS} = 0.05$ V and $V_{DS} = 2.5$ V with $L = 100$ nm

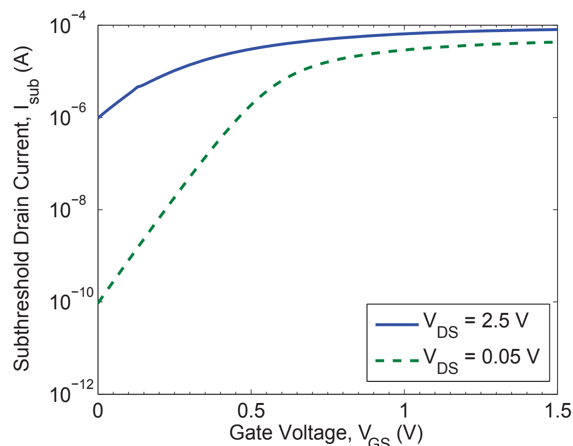

Fig. 13. Subthreshold drain current vs. gate voltage for two drain biases, $V_{DS} = 0.05$ V and $V_{DS} = 2.5$ V with $L = 50$ nm

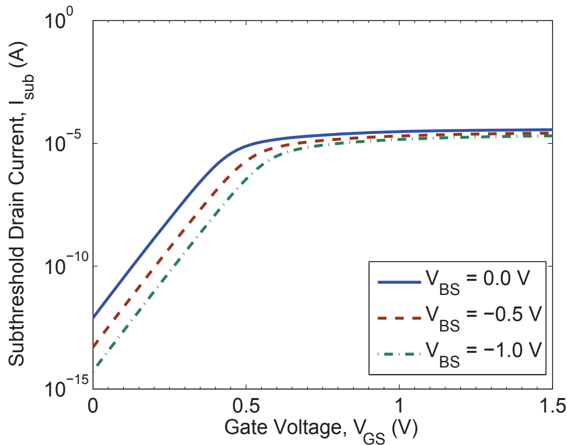

Fig. 14. Subthreshold drain current vs. gate voltage for different substrate biases with $V_{DS} = 0.05$ V and $L = 0.25$ μm

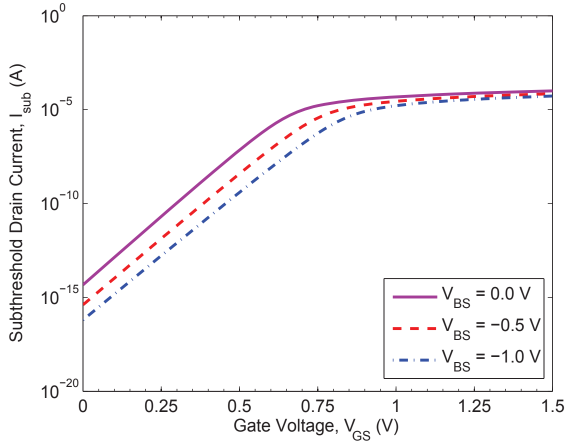

Fig. 15. Subthreshold drain current vs. gate voltage for different substrate biases with $V_{DS} = 0.05$ V and $L = 100$ nm

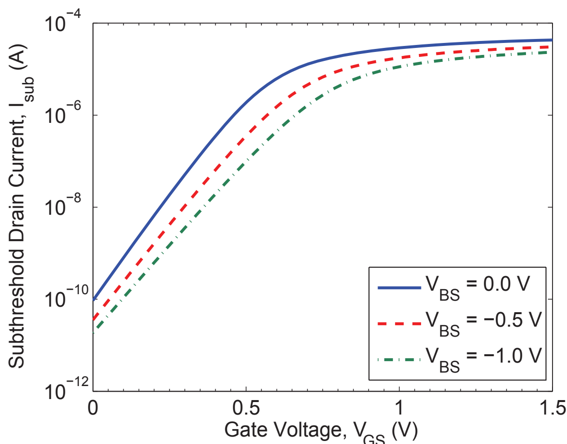

Fig. 16. Subthreshold drain current vs. gate voltage for different substrate biases with $V_{DS} = 0.05$ V and $L = 50$ nm

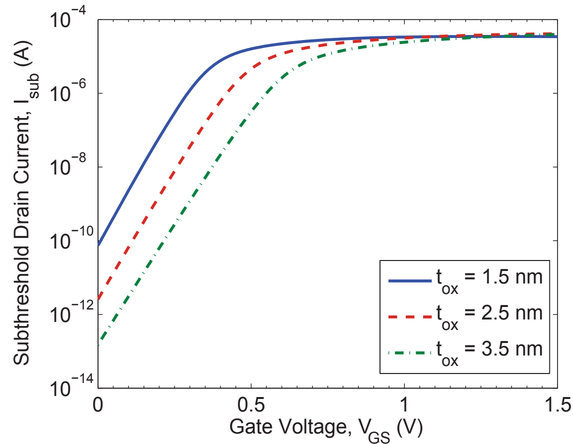

Fig. 17. Subthreshold drain current vs. gate voltage for different oxide thicknesses with $V_{DS} = 0.05$ V and $L = 100$ nm

$N_{pm} = 2.5\times10^{18}$ cm^{-3}, pocket length, $L_p = 25$ nm, channel length, $L = 100$ nm, substrate bias, $V_{BS} = 0.0$ V and drain bias, $V_{DS} = 0.05$ V. It is observed that as oxide thickness increases, subthreshold drain current decreases for the same applied gate and drain biases. This happens due to the less control on the inversion layer charge when t_{ox} increases.

Figs. 18-19 show the variation of subthreshold drain current with the gate voltage for three different peak pocket implant concentrations of $N_{pm} = 2.5\times10^{18}$ cm^{-3}, 1.5×10^{18} cm^{-3} and 9.5×10^{17} cm^{-3} and three different pocket lengths of L_p = 10 20 and 30 nm respectively with drain bias, $V_{DS} = 0.05$ V and channel length, $L = 100$ nm. It is observed that as the peak of the pocket implant concentration/pocket length increases, the subthreshold current decreases for the same applied gate and drain biases. This happens due to the additional doping atoms of pocket implantations present near the source and drain edges. Thus subthreshold behavior is improved by reducing off-state current. It is also observed that as the peak pocket implant concentration/pocket length

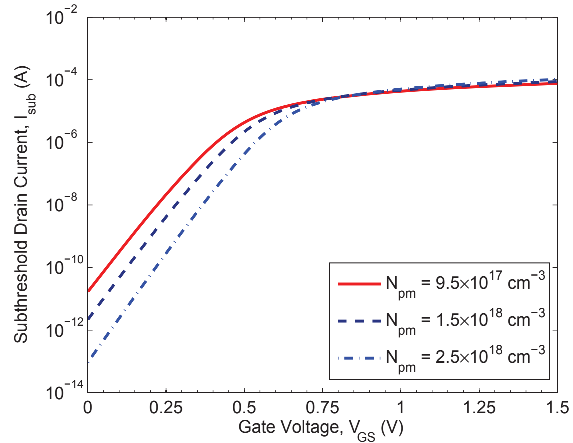

Fig. 18. Subthreshold drain current vs. gate voltage for different peak pocket implant concentrations with $V_{DS} = 0.05$ V, $L_p = 25$ nm and $L = 100$ nm

decreases further then the subthreshold slope decreases. Because then the RSCE diminishes. This is expected from the pocket implanted n-MOSFET for short channel devices. The subthreshold slope variation is larger due to the peak pocket concentration variation than that of the pocket length.

In Fig. 20, experimental data from [11] is fitted to the simulated data for the device parameters given in [11]. The parameter values are- substrate concentration, $N_{sub} = 5.5\times10^{17}$ cm^{-3}, peak pocket concentration, $N_{pm} = 8.0\times10^{17}$ cm^{-3}, pocket length along the channel, $L_p = 40$ nm either from source or drain side, oxide thickness, $t_{ox} = 4$ nm, junction depth, $r_j = 50$ nm, substrate bias, $V_{BS} = 0.0$ V and drain bias, $V_{DS} = 0.05$ V. From Fig. 20, it is clear that the simulated data agrees well with the experimental data in [11] of the subthreshold region. By changing the process conditions, it is possible to adjust the simulated data with the experimental data published in the literature.

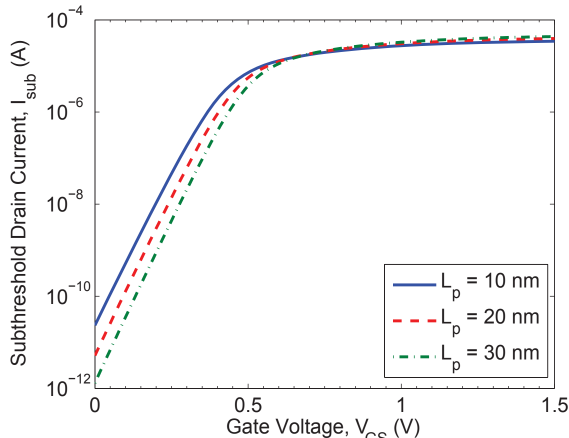

Fig. 19. Subthreshold drain current vs. gate voltage for different pocket lengths with $V_{DS} = 0.05$ V, $N_{pm} = 2.5\times10^{18}$ cm^{-3} and $L = 100$ nm

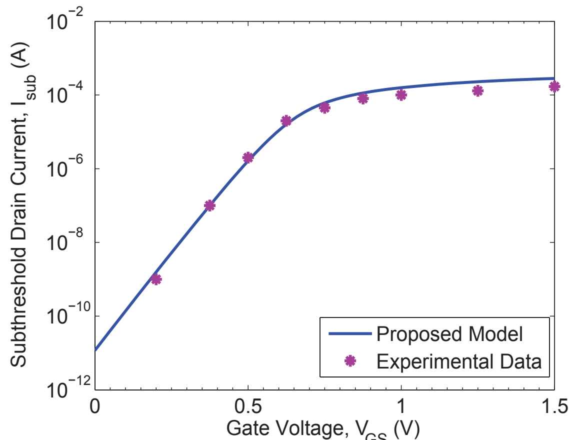

Fig. 20. Fitting experimental data already published in the literature [11] with the simulated results of the proposed subthreshold drain current model

V. Conclusion

This paper gives an analytical subthreshold drain current model for the ultra thin oxide and nano scale pocket implanted n-MOSFET based on conventional drift-diffusion equation and using the surface potential, threshold voltage as well as inversion layer effective mobility models of the pocket implanted n-MOSFET from earlier works. The model is developed assuming two linear pocket doping profiles along the channel at the surface of the device from the source and drain edges towards the center of the channel. The effect of changing the device and pocket profiles parameters as well as bias potentials on subthreshold drain current have been studied using the developed model. Simulated results show that the proposed model predicts the subthreshold drain current in to the nano scale channel lengths. Experimental data for subthreshold drain current found in the literature matches the simulated data. Hence this model efficiently calculates the subthreshold drain current of the pocket doped n-MOSFET having channel lengths in the nano scale regime.

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