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Design and Implementation of a 10-bit SAR ADC

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***Abstract*—**This paper presents the development of a 38.5 kS/s 10-bit low power SAR ADC which is realized in MIMOS's 0.35 µm CMOS process. The design uses a resistive DAC, a dynamic comparator with pre-amplifier and SAR digital logic to create 10 effective bits while consuming less than 7.8 mW with a 3.3 V power supply.

***Keywords*—**Successive Approximation Register Analog-to-Digital Converter, SAR ADC, Resistive DAC.

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) represents the majority of the market for the medium to high resolution ADCs [1]. The advantages of SAR ADCs are they provide low power consumption, high resolution, high accuracy and smaller die area [2]-[6]. These advantages make the ADCs ideal for a wide variety of application such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition [6]. SAR ADCs cover sampling rate from few kilo Sample per second (kS/s) up to 5 Mega Sample per second (MS/s) and the resolution is normally covers from 8 to 16 bits [6].

In agriculture monitoring system, sensors and their electronics normally work at a medium speed ranging from few kHz to few MHz. For post-processing purposes, an ADC is needed to convert the analog signal to digital signal. The requirement for a low power device makes SAR ADC a suitable candidate.

In this paper a single-ended 10-bit SAR ADC is realized based on MIMOS' 0.35 µm CMOS process, using a voltage scaling DAC [7]. Simulation result shows that this proposed ADC achieved low power consumption and suitable for agriculture monitoring system or other battery used applications.

II. Design of the SAR ADC

A. Architecture

The 10-bit SAR ADC consists of a sample-and-hold (S/H) stage, a digital-to-analog converter (DAC), a comparator and a SAR logic module as shown in Fig. 1. The S/H stage circuit will be discussed together with the comparator design. The emphasis of the design focuses on meeting the requirement of 10 bit accuracy for a reference voltage span of 0.5V and considerable low power consumption.

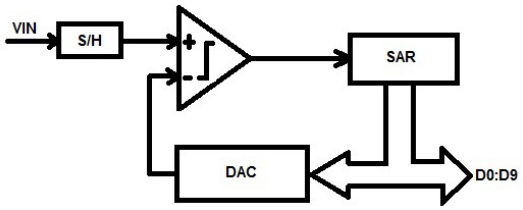

Fig. 1 SAR ADC architecture

B. DAC

The DAC is the most critical component of the SAR, and it is difficult to design. The SAR ADC's speed is mainly limited by the settling time of the DAC and the comparator, which must resolve small difference in input voltage within the specified time.

The DAC utilizes resistive ladder architecture. Fig. 2 shows the DAC circuitry used in this work. The main DAC was controlled by 6 Most Significant Bits (MSB) while the last 4 Least Significant Bit (LSB) controlled lower DAC. This architecture was selected due to its good linearity and there were some limitation in the capacitor sizes for the targeted foundry.

The main DAC has 4 rows and 16 columns resistors connected in series. The 2 MSB bits determined which row to be switched-on and the next 4 bits control which column in that row to be switched-on. The lower DAC has only 16 resistors in series with the 4 LSB controlling the switches. This architecture saved the total number of resistors since only 80 resistors were used compared to 1024 resistors for the conventional architecture, hence the die size is reduced.

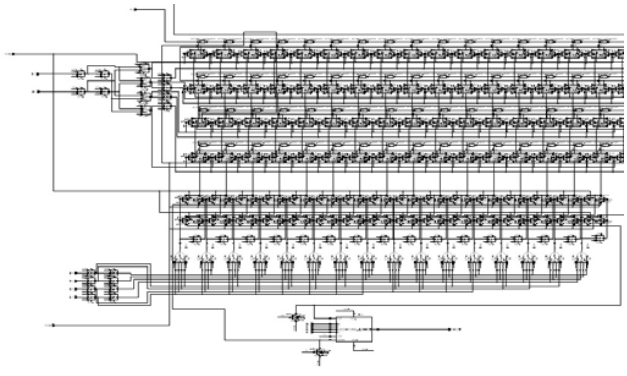

Fig. 2 DAC architecture

C. Comparator

Comparator used in a SAR ADC must be accurate to the

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value of the Least Significant Bit (LSB). For a 10-bit ADC with reference voltage of 0.5V, the LSB value is about 488 μV. Therefore, the comparator must be able to resolve a 488 μV voltage difference between the inputs. However, to design such a high performance comparator would require more resources that lead to higher current and power consumption.

The comparator circuit used in this ADC comprises of a pre-amplifier and a latch. In this design, the sample and hold circuit was included together with the comparator design as shown in Fig. 3.

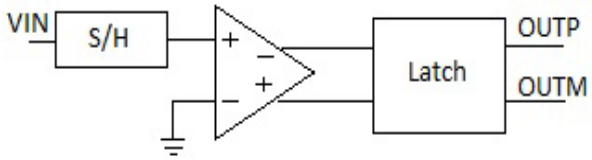

Fig. 3 Sample and Hold, pre-amplifier and latch

S/H stage happens after the offset cancelation stage. During the offset cancelation stage, both the comparator's input terminals are connected to common mode voltage (VCM) or virtual ground. The common mode value for this design was set to the half of the supply voltage. During S/H stage, the input voltage (VIN) will be charge the capacitor which was pre-charge to VCM. So positive terminal now have VIN + VCM voltage which is compared with VCM in the comparator's negative terminals.

In this design, three single stage pre-amplifiers were used to boost the input voltage before the comparator input. This method relaxes the performance required from the latch and hence, reduces the current consumed. The comparator used in this design has a latch with minimum-sized devices.

The pre-amplifier circuit was a single stage fully differential amplifier with a common mode feedback as shown in Figs. 4 and 5.

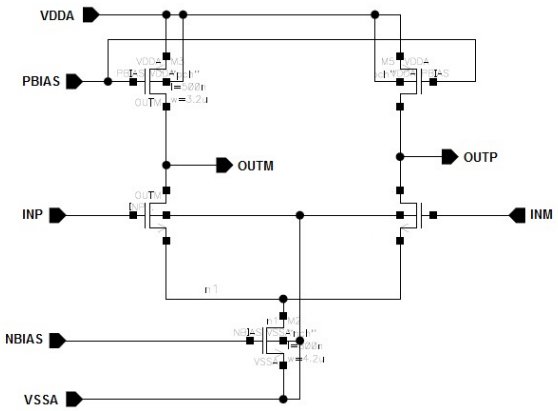

Fig. 4 Single-stage fully differential amplifier

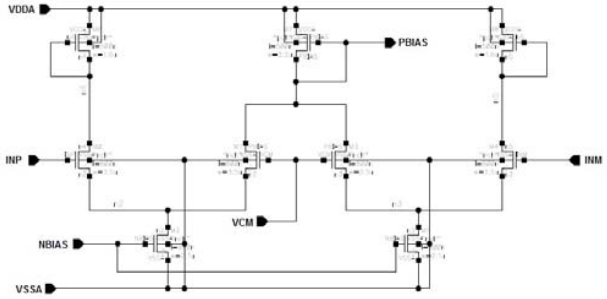

Fig. 5 Common mode feedback circuit

Since the LSB value is very low, noise cancelation is needed for the pre-amplifiers. The auto-zeroing technique was implemented for the amplifiers as shown in Fig. 6. Each amplifier has an auto-zero capacitor connected between each input and output terminals. The pre-amplifiers noise cancelation happens before S/H stage. When the sampling signal is high, the auto-zero switches will be closed. The charge at the input and output terminal for each amplifier will be the same, hence removing the input and output offset voltage.

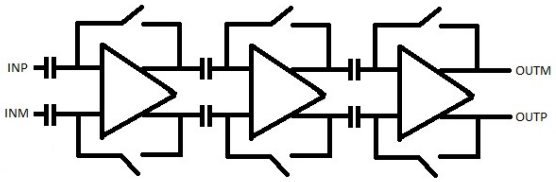

Fig. 6 Pre-amplifier with a noise cancelation circuit

The latch used was a dynamic latch with a reset. The input voltages for the two input terminals were reset to supply voltage when the clock is low. The advantage of using this circuitry compared to the regenerative dynamic latch is there is no extra clock state needed. This circuitry used the same clock signal as the SAR logic. Fig. 7 shows the schematic of the latch.

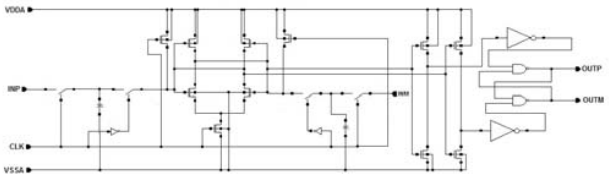

Fig. 7 Dynamic latch

D.SAR Logic

The SAR logic was designed to give a digital code to the DAC based on the output from the comparator. It consists of digital cells designed to perform a binary search algorithm and give the ADC output at the end of the operation together with the End of Conversion (EOC) signal.

In this design the SAR logic used 13 clock cycles per conversion. The first 2 clock cycles were used for offset cancelation and S/H while another 10 clock cycles were used for conversion. The 13th clock cycle was used to generate the EOC signal and output parallel digital data.

III. Result

The 10-bit SAR ADC was designed and simulated using MIMOS' 0.35µm technology. Fig. 8 shows the layout implementation of the ADC.

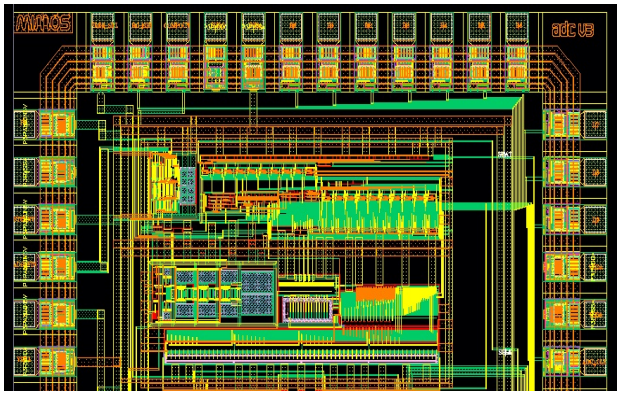

Fig. 8 ADC layout implementation

Fig. 9 shows the simulation result for the DAC. The DAC's DNL shows good linearity with maximum DNL of 0.2598 LSB, which is within ± 0.5 LSB.

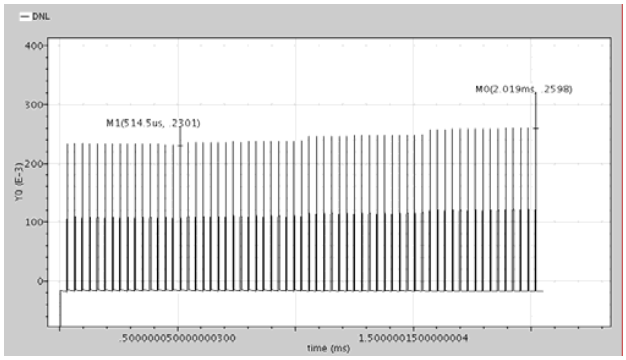

Fig. 9 Simulated DNL

The comparator was designed to be able to detect 0.5LSB change. The simulation result in Fig. 10 shows that the comparator is able to detect a very big positive, small negative, big negative and small positive voltage differences.

The drawback for the comparator is that it consumes current up to 1.1 mA due to large amount of current needed to charge & discharge big capacitors in the latch. This happens due to the process limitation where a small capacitor could not be used.

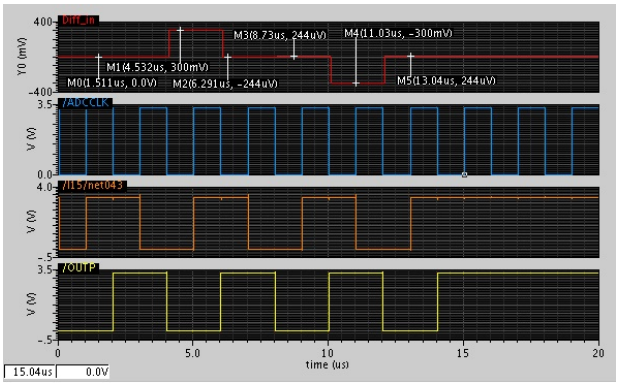

Fig. 10 Comparator result

Simulation result for the SAR logic is shown in Fig. 11. The STCONV signal initializes the SAR logic. The parallel digital code is valid after one clock cycle after the EOC signal. All activities in SAR logic happens at the clock falling edge.

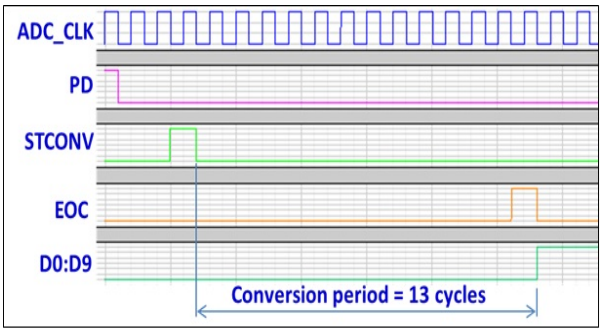

Fig. 11 SAR logic timing diagram

Top level simulation shows that SAR ADC could convert analog signal of 488 µV difference. Fig. 12 shows that the DAC value converged to the input value. The DAC value also shows that the SAR logic is correctly implementing binary search algorithm. Simulation by increasing the input voltage 1 LSB every conversion cycles also shows that the ADC is able to do the conversion without having a missing code as in Fig. 13.

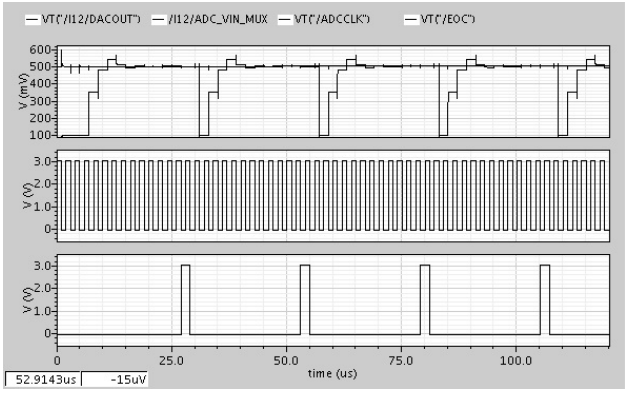

Fig. 12 DAC simulation

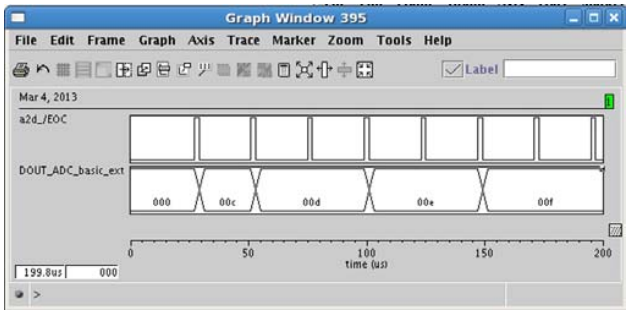

Fig. 13 Top level simulation

IV. Conclusion

A single ended 38.5 kS/s 10-bit SAR ADC was designed in a 0.35µm CMOS technology using standard threshold devices. The overall area of the circuit is 1.7 x 1.8 mm^2. The resistor used in the DAC is implemented using poly resistor. Total power dissipation is 7.8 mW, where large amount came from the comparator design due to the process limitation. The ADC has the option to turn off when not needed. In the future, the comparator design could be improved to achieve lower power consumption.

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