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Analog Front End Low Noise Amplifier in 0.18-μm CMOS for Ultrasound Imaging Applications

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***Abstract*—**We present the design of Analog front end (AFE) low noise pre-amplifier implemented in a high voltage 0.18-μm CMOS technology for a three dimensional ultrasound bio microscope (3D UBM) application. The fabricated chip has 4X16 pre-amplifiers implemented to interface a 2-D array of high frequency capacitive micro-machined ultrasound transducers (CMUT). Core AFE cell consists of a high-voltage pulser in the transmit path, and a low-noise transimpedance amplifier in the receive path. Proposed system offers a high image resolution by the use of high frequency CMUTs with associated high performance imaging electronics integrated together. Performance requirements and the design methods of the high bandwidth transimpedance amplifier are described in the paper. A single cell of transimpedance (TIA) amplifier and the bias circuit occupies a silicon area of 250X380 μm^2 and the full chip occupies a total silicon area of 10x6.8mm².

***Keywords*—**Ultrasound, analog front end, medical imaging, beam forming, biomicroscope, transimpedance gain.

I. Introduction

ADVANCED imaging equipments used in real time three dimensional body scanning are available as portable or hand held units [1]. Availability of such miniature yet low cost medical imaging systems have created a global trend in shifting the emphasis on personal care from a hospital setting to a primary healthcare professional or to an individual level. This revolutionary change in healthcare has not only improved the personal care management but also helped to shift the emphasis from cure to prevention. In recent times the development in ultrasound imaging is much ahead of its peers largely due to the use of sub-millimeter size capacitive micro machined ultrasound transducers (CMUT) as high frequency acoustic sensors or actuators [2]. Ultrasound medical imaging systems typically find their use in ophthalmology, dermatology and intravascular studies apart from other clinical diagnostic and industrial applications.

Three dimensional (3D) Ultrasound Bio microscope (UBM) system provides high image resolution as they use large number of high frequency CMUT elements in 2D array format. In addition to the superior high frequency and larger bandwidth capability of CMUTs, the novel integration methods adopted to interface the CMUT in silicon and the CMOS integrated circuits has further pushed the performance boundaries beyond the large piezoelectric transducer based systems used in the past [2]. However the system design poses challenges in (i) integrating the large number of array elements of transducers to interface circuits (ii) designing the multi channel imaging electronics within the power budget and available silicon area as the transducer frequencies are increased to achieve better image resolution. As shown in Fig. 1. Typical transducer interface circuit consists of a high voltage pulser circuit to actuate and a low noise pre amplifier to recover the noisy signal received in the sense mode. A high voltage isolation switch is employed to select either the actuation or sensing mode at a given point in time.

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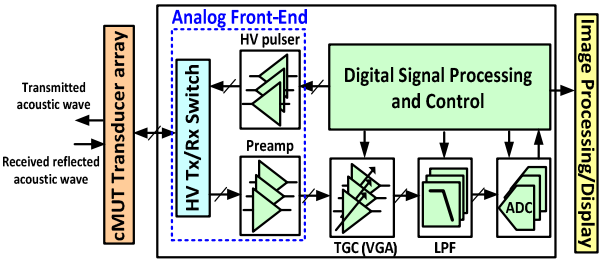


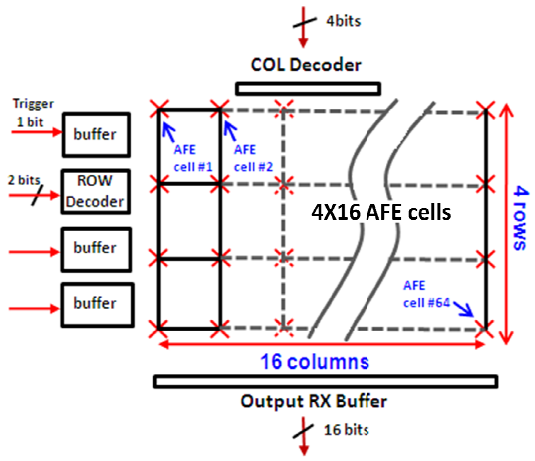
Fig. 1 Overall block diagram of the typical ultrasound imaging system including the multi-channel AFE IC, CMUT array, and signal processor

In this work, we describe the design, fabrication and measurement of a large bandwidth transimpedance amplifier (TIA) interfacing the high-frequency 2-D CMUT array used for 3-D ultrasound medical imaging applications. Design of TIA is critical to image resolution and receive sensitivity. The IC consists of 4X16 High voltage (HV) pulsers in the transmit path to drive the transducers and 4X16 low-noise TIA with HV protection switches to receive the reflected echo signal. In Section II we briefly explain the AFE system details and the performance requirements. Section III describes the TIA circuit design in detail. Section IV is dedicated to the measurement results and the conclusions are followed in Section V.

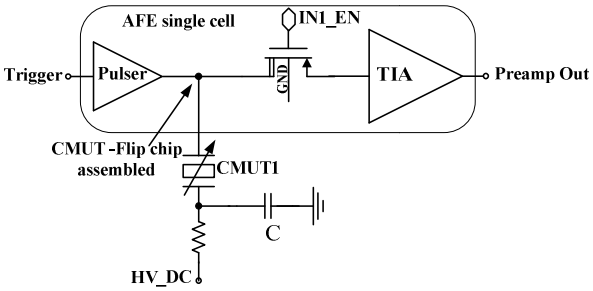
II. System Description

A. System Level and Block Level Overview

System architecture of a typical high resolution ultrasound imaging system is shown in Fig. 1. A Multi channel planar 2-D transducer array is interfaced to the AFEs by flip chip assembly process [3]-[4]. System architecture of a typical high resolution ultrasound imaging system is shown in Fig. 1. A multi channel planar 2-D array is interfaced to the AFEs by flip chip assembly process.



(a)



(b)

Fig. 2 (a) AFE system diagram showing the functional block level organization of the IC (b) AFE IC unit cell

A HV pulser HV isolation switch and a preamplifier constitute the core circuit of the AFE as shown in Fig. 2 (a). Another key multifunctional building block in the system a digital signal processing (DSP) block which primarily does all the control functions apart from driving and processing the signals within the system. DSP drives the HV pulsers [5] with a low voltage trigger pulse with programmable delays to facilitate beam forming [6]. High voltage pulses from the pulser actuate the transducer to produce acoustic waves and these waves are launched into an acoustic medium to characterize the properties. The wave propagates through the medium and will encounter wave reflections at impedance discontinuities within that medium. These reflected echo waves are received by the transducer in the sense mode and converted into electrical signals to further process by the receiver blocks of the system. The receiver is typically made up of various blocks such as the low-noise preamplifiers, time-to-gain (TGC) compensation amplifiers and analog to digital converters (ADC) to digitize the received signals. These digital signals are presented to the DSP to create a 3D visual image from the received echo information.

A 4X16 cells AFE IC is designed to interface to a 2-D array of CMUTs of same matrix dimension or a larger array by a flip chip assembly process. Fig. 2 (a) shows the functional Fig. 3.

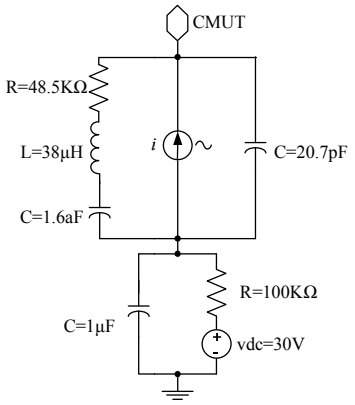


Fig. 3 Equivalent circuit model of CMUT

Blocks and their organization in the core area of the silicon chip. As in Fig. 2 (b), a unit cell of the AFE consists of a HV pulser and a HV protection switch and the preamplifier. The role of the protection swich is to prevent the HV pulse appearing at the low voltage preamplifier input during the actuation phase which can cause a permanent damage to the receiver blocks.

B. Specifications

The scope of this work is limited to the design of the low noise preamplifier for the AFE and hence we restrict the focus to the input and output interface to the preamplifier to develop design requirement specification. Fig. 3 shows an equivalent circuit of a CMUT cell and it resembles to an equivalent circuit model of a photo diode. A single CMUT element consists of multiple unit capacitors connected in parallel and each element in our design presents an equivalent deflected capacitance of 20.7 pF when a dc bias voltage (V_{DCbias}) is applied on its terminal. Resonant frequency of such a single cell is found to be 15MHz (3 dB bandwidth). In order to calculate the range of current signal that need to be faithfully amplified, we need to know the maximum and minimum of the echo signal received at the CMUT and the corresponding variation in the capacitance to find the current. Equivalent circuit model and the expression relating the capacitance variation to the output current is used to arrive at the design requirements for the front end amplifier. Proposed preamplifier is expected to drive a TGC block in the system.

C. Low Noise Amplifier and Protection Switch

In the sense mode, transducer receives the acoustic pressure waves reflected from the media boundaries (echo signals) and the received ultrasound pressure signals make the CMUT membrane to vibrate and to change its effective capacitance across the terminals. In response to the vibration, there will be an ac current generated in the capacitor which is proportional to the wideband pressure signal incident on the CMUT's movable top plate surface.

TABLE I
PREAMPLIFIER DESIGN SPECIFICATION

Parameter	Specification
Gain	81dBΩ(11K)
Bandwidth	7.5MHz to 22.5MHz (Fc-15MHz)
Input current	18.7nA to 36μA
Output voltage	400 mVpp
Input noise current	12nArms
Output load	200Ω//15pF
Area	300μmX300μm

V_{DCbias} represents the DC bias voltage applied to one of the plates of CMUT and ΔC stands for the incremental capacitance when the capacitance top plate is deflected due to membrane vibration.

$$I_{CMUT} = V_{DC\_BIAS}\frac{\partial(\Delta C)}{\partial t} = \frac{\partial(\Delta Q)}{\partial t} \quad (1)$$

As such the current signal is a wide band signal hence we need a low noise broadband amplifier to sense the low magnitude (few nano ampere to 10's of microampere) range input current signal. For a high impedance broadband source like CMUT, it is customary to use Transimpedance amplifier (TIA) for wideband current amplification [7]. TIA presents low input impedance and low input referred noise over a wider bandwidth. Low input impedance property of the TIA helps to maximize the received input current and thereby produce a larger voltage swing at the amplifier output.

From the experiments we found that the minimum echo pressure received for the application at the CMUT surface is 1.23e2 Pascal with -1dB/MHz/cm attenuation in the medium and it corresponds to a capacitance variation of 2.62aF. Using the minimum and maximum variation in capacitance with varying echo signals, the range of current in the CMUT is obtained and for the case of minimum current, the input noise requirements for the amplifier are calculated. Table I shows the transimpedance amplifier design specifications. HV DNMOS transistors are used as switches to protect the receiver stage from HV pulses during the actuation phase. It is important to choose smaller device sizes to ensure minimal signal losses and low noise performance due to the devices ON resistance Ron which is larger with large transistor width.

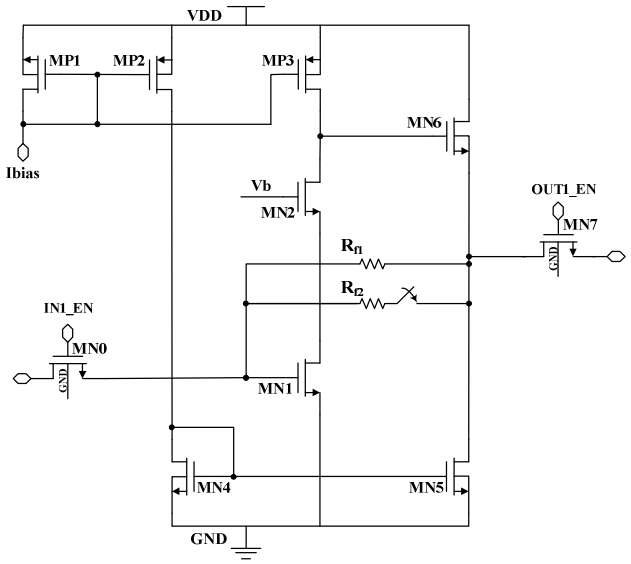


Fig. 4 Simplified TIA circuit schematic

III. LOW NOISE AMPLIFIER DESIGN

We chose TIA topology with resistor feedback to realize the front end low noise amplifier greatly due to its desirable properties such as the broadband characteristics, and the reported wide usage in ultrasound systems [2], [7], [8]. We use 1.8V CMOS transistors and achieve an output voltage swing of 400mVpp. Various TIA topologies have been used to interface the CMUT in the sense mode and a common source amplifier cascaded with a source follower is found to be most popular [7], [8] for the ultrasound applications. However when the frequency of operation and the required bandwidth is higher, the common source stage can only provide a limited bandwidth as the output pole frequency moves closer to origin due to the Miller capacitance effect at the input. A cascode common source stage is the solution to enhance the bandwidth. Fig. 4 shows the simplified circuit diagram of a resistive feedback TIA which is made up of a cascode common source amplifier followed by a source follower stage. MN1 and MN2 form the cascode common source gain stage and MP3 provide the required bias current to the branch. Output pole frequency for this stage can be obtained from (2) in which C_{GD1}, C_{GD2}, C_{DB2} are the parasitic capacitance at the drain to gate and the bulk terminal respectively for MN1 and MN2. C_L is the load capacitance of the subsequent source follower stage which is inherently low and r_{03} is the resistance presented by the active load MP3.

$$\omega_{pole\_cs\_cascode} = \frac{1}{r_{03}(C_{DB2}+C_L+C_{GD2})} \quad (2)$$

$$\omega_{TIA\_3dB} = \frac{1}{R_{IN}(C_{CMUT}+C_P)} \quad (3)$$

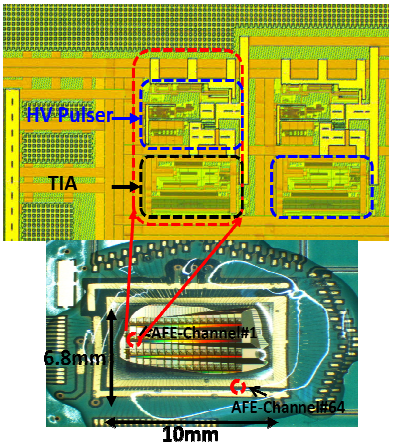


Fig. 5 4X16 AFE IC COB assembly on PCB and the chip micrograph

TIA's closed loop 3dB bandwidth is determined by (3) wherein $R_{IN} = \frac{R_f}{(A+1)}$ in which R_f is the feedback resistor and A is the magnitude of open loop gain of the amplifier and C_{CMUT} is the transducer capacitance and C_P is the input parasitic capacitor at TIA input. For a common source amplifier

$$C_P = (A+1)C_{GD} \tag{4}$$

Whereas for a cascoded common source amplifier magnitude of A=1 and therefore substituting into (4), for the cascode amplifier

$$C_P = (1+1)C_{GD} \tag{5}$$

Assuming C_{MUT} is resonant at the centre frequency in which case we may ignore the C_{CMUT} term in (3) and substituting (4) & (5) in (3) separately and comparing, we see that the cascode common source amplifier bandwidth is much higher (approximately A/2 times larger) than the common source amplifier and the choice is justified.

As we need to cover a broader range of input current (18.7nA to 36μA), we have provided a gain switch to facilitate a high gain mode and a low gain mode (gain lowered by a factor of 6dB from high gain value). Feedback resistor Rf1 and Rf2 set the closed loop transimpedance gain of the amplifier as 84 dBΩ (15.6KΩ) in the high gain mode and 78 dBΩ (7.8 KΩ) low gain mode. Noise analysis of the TIA [7] reveals that the predominant sources of noise contributors are the main transistor MN1 with minor contribution from MN2 and the feedback resistor R_f. Inorder to minimize the noise in the amplifier; it is required to maximize Rf and the g_{m1} of MN1 for a desired bandwidth of the amplifier as an increase in these parameters inversely affect the bandwidth. Typical input referred current noise in the simulation is found to be 12nArms integrated over a bandwidth of 15MHz. A single TIA cell and bias circuit consumes 5.5mA current from a 1.8V source.

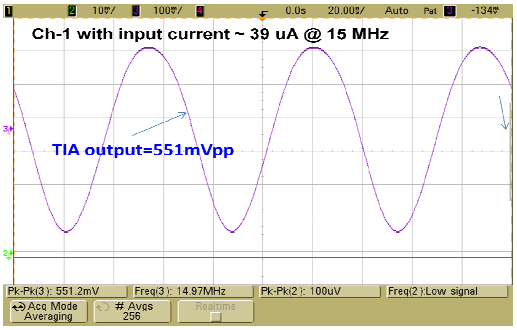


Fig. 6 4X16 AFE IC COB assembly on PCB

IV. Measurement Results

Fig. 5 shows the AFE chip assembled on to the PCB using chip on board (COB) method and also shown the chip micrograph highlighting a single channel of TIA and pulser in the 4X16 channel AFE. Measured output voltage (551mV) for an input current of 39uA is shown in Fig. 6. Measured gain and bandwidth plot is shown in Fig. 7. We found the bandwidth and gain is little inferior in the channels with longest trace lengths (for example channel #64) causing higher ohmic losses in the metal lines routing the power supply to those amplifier blocks. Fig. 8 shows the integrated input referred noise measured over 15MHz bandwidth .Noise spectrum is measured in a spectrum analyzer and using (6) we calculate the input referred noise over the bandwidth.

$$input\ noise = \left(\frac{Spot\ noise\ in\ \mu V}{(\sqrt{RBW})\frac{1}{R_f}}\right) * \sqrt{B.W} \tag{6}$$

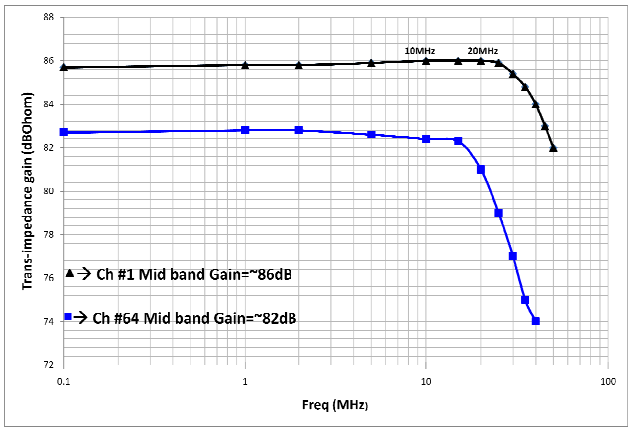


Fig. 7 Transimpedance gain measured in channel #1 and channel#64

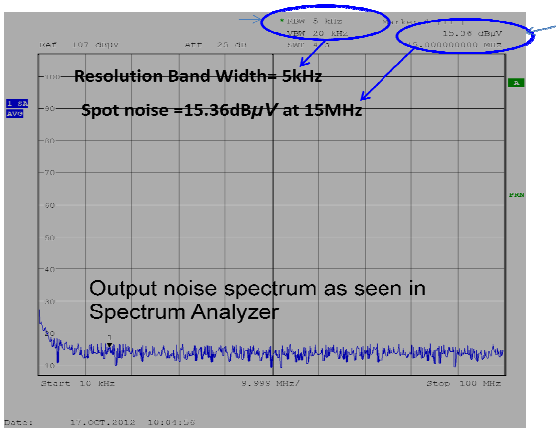


Fig. 8 Input referred noise measurement

Integrated noise value is found to be 15nArms and it is slightly more than simulated value of 12nArms.

Discrepancy in simulation and noise measurement is mainly attributed to (i) additional board and interconnect parasitic capacitance at the input of the amplifier. (ii) Measurement error-we use a high impedance RF probe to measure the noise spectrum and the method is not very accurate in measuring noise.

TABLE II
MEASUREMENT SUMMARY

Parameter	Simulated	*Measured*
Bandwidth (Ch-1)	0-25MHz	*0- ~30MHz*
Bandwidth (Ch-64)	0-25MHz	*0-20MHz*
Ch1-Gain(dBΩ)	85	*86*
Ch-64 Gain(dBΩ)	85	*82*
Input Noise	12nArms	*15nArms*
Current	5.5mA	6mA
Area	250μmX380μm	

V. CONCLUSION

A 4X16 channel AFE IC is implemented in 0.18-μm CMOS process. Transimpedance amplifier topology is employed to implement the 64 channel low noise front end amplifiers and achieved a transimpedance gain over 81dBΩ to meet the gain requirements. Gain variation across channels was observed with a worst case variation of 3 dB for the farthest channel from channel #1. The loss in gain is attributed to the ohmic losses in the power line metal conductor. Input referred noise power is found to be 15nArms integrated over 15MHz bandwidth and the measured value is slightly higher than the simulated value mainly due to the excessive board and interconnect parasitic at the amplifier input. Developed IC can be utilized to build functional handheld ultrasound 3D biomicroscope and many other similar sensor interface applications.

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