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Design of an Ultra Low Power Low Phase Noise CMOS LC Oscillator

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***Abstract*—**In this paper we introduce an ultra low power CMOS LC oscillator and analyze a method to design a low power low phase noise complementary CMOS LC oscillator. A 1.8GHz oscillator is designed based on this analysis. The circuit has power supply equal to 1.1 V and dissipates 0.17 mW power. The oscillator is also optimized for low phase noise behavior. The oscillator phase noise is -126.2 dBc/Hz and -144.4 dBc/Hz at 1 MHz and 8 MHz offset respectively.

***Keywords*—** LC oscillator, Low Power, Low Phase Noise

I. Introduction

OSCILLATORS are one of the most common functional blocks in communication systems. Integrated LC Voltage Controlled Oscillators (VCOs) are used as an input for mixers to up- and down-convert signals and have particular importance in fully integrated transceivers. Proper amplitude and low phase noise are two key criteria to achieve suitable performance for a VCO in any transceiver [1]. The strong combination of very low phase noise specifications with very low power consumption (battery operation) pushes designers to use LC-VCOs. A great research effort has been invested in the design of integrated voltage controlled oscillators (VCOs) using integrated or external resonators, but as their power consumption is still unacceptable, today's mobile phones commonly use external LC-VCO modules [2].

This work aims at the overall optimized design of integrated VCOs providing differential outputs with power consumption lower than external VCO modules and lower phase noise.

The paper is organized into six sections. Section 2 discusses the complementary CMOS LC VCO structure. Section 3 and 4 cover systematic LC-VCO design for low power and low phase noise. Section 5 presents the simulation results, followed by the conclusion in Section 6.

II. Complementary CMOS LC VCO

The complementary cross-coupled VCO has two main advantages compared with NMOS transistors only cross-coupled topology. First, with the additional PMOS pair, the complementary topology offers higher transconductance to compensate for the loss of the tank with less current consumption and hence is more power efficient. Second, matching the PMOS and NMOS transistors, the complementary topology provides better symmetry properties of the oscillating waveform, which decreases the upconversion of $1/f$ noise of devices to the $1/f^3$ phase noise region [3].The complementary CMOS oscillator is depicted in Fig. 1. When the oscillation condition is satisfied, oscillation starts to develop. As the oscillation amplitude grows larger, it will reach a point where the negative resistance is not enough to support the positive resistance (loss) of the LC tank if the supply voltage and ground do not first clip the maximum swing. This is where the amplitude stops growing and a stable oscillation is reached [4]. The complementary cross-coupled oscillator shows a better phase noise performance when compared to the NMOS- or PMOS-only cross-coupled oscillators for the same supply voltage and bias current when operating at the current limited regime [5]. This is mainly because the complementary cross-coupled oscillator of Fig. 1 presents a larger maximum charge swing q_{max} than that of the NMOS- or PMOS-only cross-coupled oscillators which overall enhances its phase noise performance [6]. The complementary CMOS LC VCO structure without tail (WT) has better phase noise performance than the fixed biasing (FB) structure. The main advantage of WT topology over the FB (fixed biasing) topology is that without the tail transistor flicker noise source, the only flicker noise source now is of the cross coupled transistors, which have an inherently lower flicker noise due to the switched biasing, resulting in better phase noise performance. Another disadvantage of the FB topology compared to WT topology, is that the tail transistor in the FB topology reduces the headroom available for oscillation which is not negligible for low voltage design. A smaller signal power has an adverse effect on the phase noise, as phase noise is essentially the noise to signal ratio of the VCO. For the FB topology, extra circuitry is needed to provide biasing voltage to the tail transistor. This increases the power consumption and also introduces noise sources to the VCO. The noise current coming from the biasing network will be mirrored into the tail transistor while the WT topology does not encounter this problem [7].

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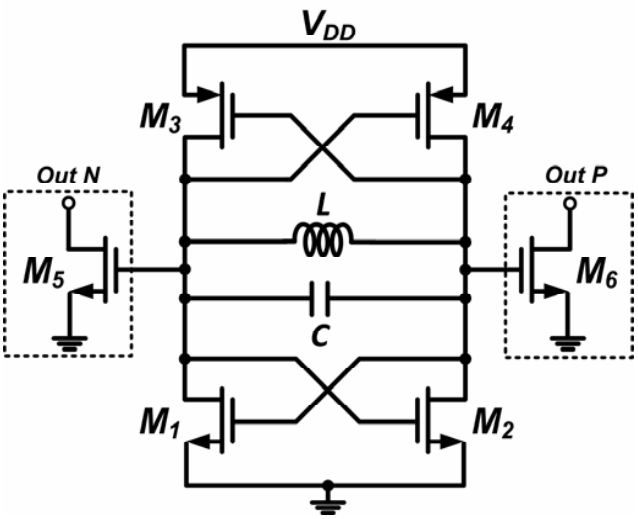

Fig. 1 Complementary CMOS LC Oscillator (M5, M6 placed in dashed lines are buffers.)

The transistors current in this oscillator are dynamically changed related to the oscillation amplitude. The crossed coupled NMOS and PMOS transistors provide enough negative parallel resistance on the tank circuit to keep the tank oscillation. The minimum g_m for the transistors is as much as inverse the equivalent parallel resistance of the tank circuit. Increasing the quality-factor (Q) of the tank circuit decreases the required minimum g_m and so the power consumption can be decreased [8]. But on-chip inductors have low-Q and increasing inductors' quality factor has physical limitations [9].

III. Power Optimization

Assuming the supply voltage of the circuit is V_{DD}, the dc voltage of output nodes will be near $V_{DD}/2$. If the oscillation amplitude is equal to v_m then the output voltages will be:

$$v_{gs1}=V_{DD}-v_{gs3}=V_{DD}/2+v_m\sin(\omega t)$$
$$v_{gs2}=V_{DD}-v_{gs4}=V_{DD}/2-v_m\sin(\omega t) \quad (1)$$

The Ml transistor turns on for $v_{gs1}\geq v_{th,n}$ and the M3 transistor turns on for $v_{sg3} \geq |v_{th,p}|$. The injected current to the tank circuit is the absolute difference of the currents of Ml and M3 and so we expect only one of these transistors conducts the current at a time to have bigger absolute injected current to the tank circuit. Conducting the current by each of Ml or M3 at the oscillation periods reduces the oscillator power consumption and the injected noise power from the transistors to the tank circuit.As it is clear from (1) for supply voltages greater than $(v_{th,n}+v_{th,p})$ Ml and M3 transistors are turned on in an overlap interval which wastes power and increases the injected noise power to the tank circuit. Increased noise power in the oscillator circuit increases the phase noise of the oscillator. Therefore, the main point to optimize the oscillator power consumption and reduce its phase noise is to control the transistors overlap interval. For this reason the supply voltage must be decreased at least to $(v_{th,n}+v_{th,p})$. With supply voltage of $(v_{th,n}+v_{th,p})$ the bias voltage at the output nodes will be close to $v_{th,n}$ which guarantees to have no overlap interval of Ml and M3 transistors. In that case, each of these transistors turns on for half of an oscillation period [8].Another noise source is resistance of the inductance [6]. The power of generated noise from inductance's resistance is $v_n^2 = 4KTR$ where K is Boltzmann constant, T is temperature and R is the value of resistance of the inductor. For specified frequency $f = 1/2\pi\sqrt{LC}$ decreasing the value of inductance make several advantages including:

- Decreasing the value of inductance leads to less resistance and hence the generated noise from it. The phase noise will be decreased, as a result.
- By decreasing the R value in inductor the required gm value also decreases. In consequence the required bias current and power are decreased.
- Smaller value of inductor leads to smaller mutual effect with other inductors on the chip.
- By reducing the value of inductor we must increase the value of capacitor. This increases q_{max} and so phase noise can be reduced.
- The value of capacitance per unit area is larger than inductance per unit area. By decreasing inductance value and increasing the value of capacitance in order to set the frequency at specified value, we can optimize (reduce) the required area in chip.

But lowering the value of inductance has limitations. A simple expression for the tank amplitude can be obtained assuming that the current in the differential stage switches quickly from one side to another. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair thus can be modeled as a current source switching between I_{bias} and $-I_{bias}$ in parallel with a RLC tank. R_{eq} is the equivalent parallel resistance of the tank. At the frequency of resonance, the admittances of the L and C cancel, leaving Req. Harmonics of the input current are strongly attenuated by the LC tank, leaving the fundamental component of the input current to induce a differential voltage swing with amplitude of $(4/\pi)I_{bias}R_{eq}$ across the tank, if one assumes a rectangular current waveform. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain [5]. In such cases, the tank amplitude can be better approximated as $I_{bias}R_{eq}$. So lowering L leads to reduce in R_{eq} value and hence reduce the tank amplitude.

In this oscillator the equivalent parallel resistance is $R_p = Q^2 \times r_s = 82 \times 4 = 256\Omega$. So the tank tranconductance is $g_{m,tank} \geq 1/R_p = 4$ mS. To meet the startup condition we set the startup coefficient $\alpha = 3.5$ [4]. Then the total transconductance of one NMOS and one PMOS should be $g_m=g_{mn}+g_{mp}=\alpha.(2g_{m,tank}) \approx 28$mS. To reduce $1/f$ noise up-conversion [10], we choose $g_{mn}=g_{mp}=14$mS. From these parameters and 0.18μm TSMC CMOS technology parameters, $\mu_n \approx 400 cm^2/VS$, $\mu_p \approx 130 cm^2/VS$, and $C_{ox} \approx 5.08 F/m^2$, when transistors work in saturation and setting $I_B=20$ μA we get:

$$\left(\frac{W}{L}\right)_n = \frac{g_{m,n}^2}{I_B \cdot \mu_n \cdot C_{ox}} = 49$$
$$\left(\frac{W}{L}\right)_p = \frac{g_{m,p}^2}{I_B \cdot \mu_p \cdot C_{ox}} = 150 \quad (2)$$

To limit short channel induced excess noise, the minimum length should be avoided, so we get transistors length = 0.3 μm.

IV. Phase Noise

Based on Hajimiri's model the phase noise is [10]:

$$L(\Delta\omega) = 10\log\left[\frac{\frac{i_n^2}{\Delta f}\sum_{n=0}^{\infty} c_n^2}{8q_{\max}^2(\Delta\omega)^2}\right] \quad (3)$$

In which, c_n is the nth harmonics coefficient of the oscillator ISF (impulse sensitivity function) Fourier series expansion and q_{max} is the maximum charge displacement in the tank circuit and $\overline{i_n^2}/\Delta f$ is the noise power spectrum.As mentioned in previous section lowering the value of inductor decreases the generated noise from it. Based on this the bias current required for compensating the loss of LC tank decreases which leads to decrease in the noise generated by active devices. For specified value of oscillation frequency, by decreasing inductance value we must increase capacitance value. Setting supply voltage to $v_{th,n}+v_{th,p}$=1.1V leads to minimize the overlap interval of NMOS and PMOS transistors and decreases the generated noise by them. All of them yield to reduce the value of phase noise.

V. Simulation results

To simulate the complementary CMOS LC oscillator, a 1.8 GHz oscillator using TSMC 0.18 μm CMOS process was designed. Circuit parameters of the oscillator are shown in Table 1. The design is based on low power low phase noise oscillator with supply voltage equal to 1.1 V. In this voltage oscillator dissipates 0.17 mW power and has -126.2 dBc/Hz, -144.4 dBc/Hz at 1 MHz and 8 MHz offset frequency respectively. Power consumption and phase noise versus supply voltage are shown in Fig. 2 and Fig. 3 respectively. The open-drain buffers M5 and M6 are employed to drive the 50Ω load of the ADS simulator.

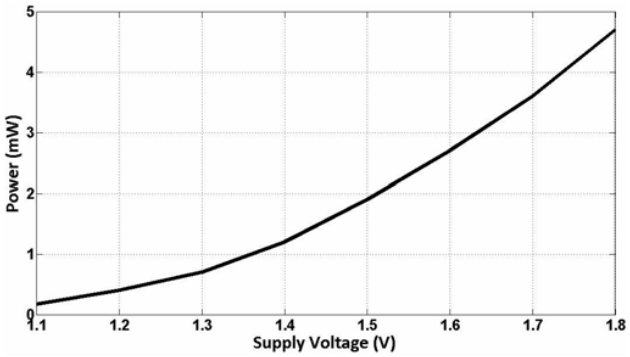

Fig. 2 Average power consumption of the oscillator versus the supply voltage

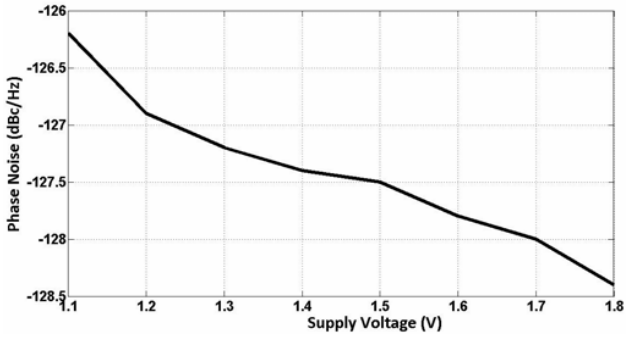

Fig. 3 Oscillator phase noise at 1MHz offset frequency versus supply voltage

A comparison between this work and state of the art oscillators is shown in Table II.

VI. Conclusion

The complementary CMOS LC oscillator was analyzed to design a very low-voltage low-phase-noise oscillator. The oscillator power consumption is decreased with reducing supply voltage and it tends to reach a constant value in low supply voltages. The designed complementary CMOS 1.8GHz, 1.1 V oscillator showed 0.17 mW power consumption and -126.2 dBc/Hz phase noise at 1 MHz offset frequency.

Table II
Performance Comparison of the Oscillator

	[11]	[12]	[13]	[14]	This Work
Technology	0.18 μm	0.18 μm	0.25 μm	0.18 μm	0.18 μm
Supply Voltage	1.2 V	0.45 V	1.5 V	1.5 V	1.1 V
Power Consumption (Main Core)	2.4 mW	0.43 mW	0.08 mW	0.95 mW	0.17 mW
Frequency	5.6 GHz	2.6 GHz	2.4 GHz	2.2 GHz	1.8 GHz
Phase Noise	-119.1 dBc/Hz At 1 MHz Offset	-105.9 dBc/Hz At 400 kHz Offset	-82.4 dBc/Hz At 1 MHz Offset	-124 dBc/Hz At 1 MHz Offset	-126.2 dBc/Hz At 1 MHz Offset

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