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Compensation Method Eliminating Voltage Distortions in PWM Inverter

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***Abstract*—**The switching lag-time and the voltage drop across the power devices cause serious waveform distortions and fundamental voltage drop in pulse width-modulated inverter output. These phenomenons are conspicuous when both the output frequency and voltage are low. To estimate the output voltage from the PWM reference signal it is essential to take account of these imperfections and to correct them. In this paper, on-line compensation method is presented. It needs three simple blocs to add at the ideal reference voltages. This method does not require any additional hardware circuit and off- line experimental measurement. The paper includes experimental results to demonstrate the validity of the proposed method. It is applied, finally, in case of indirect vector controlled induction machine and implemented using dSpace card.

***Keywords*—**Dead time, field-oriented control, Induction motor, PWM inverter, voltage drop.

I. Introduction

In some application such as vector control, the inverter output voltages are needed to calculate the desired state variables. Unfortunately, it is very difficult to measure the output voltages and it requires additional hardware. The most desirable method to obtain the output voltages is to use the reference voltages as the output ones. Generally the relation between the reference voltages and the output voltages has a nonlinear characteristic due to the distorted voltage generated by the imperfections of the voltage-source PWM inverter.

There are several causes to distort output voltage. Some is caused by the dead time that is necessary to ovoid short circuit across the legs of the inverter. The value of the dead time depends on the type and on the size of switching devices.

Another important factor is the voltage drop across the power switches. This voltage drop can be divided in two parts; one part is constant, which is referred to the threshold value; the other is the voltage drop, varying according to the load current, which is caused by the conduct resistance.

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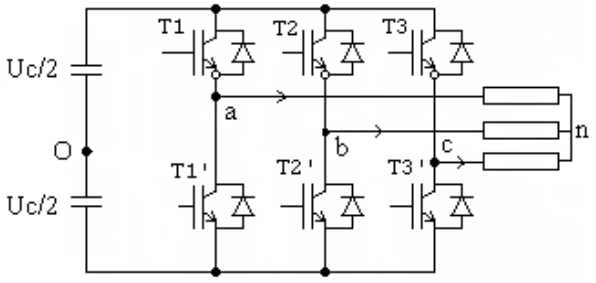

Fig. 1 Three phase voltage inverter source (VSI) with load

In variable speed drive systems, the reduction of the fundamental voltage causes reduction in output torque.

Effects of these imperfections have been described and analysed by Cardenas [1], Xing [2] and Hengbing [3]. It has been found that the dead time causes reduction in the fundamental component of the output voltage and introduces low order harmonics which are not intrinsically present in the ideal modulated wave form.

Moreover, the distorted voltage makes the current waveform very distorted and non-sinusoidal. Especially, the clamping of current around the zero crossing point. The detailed analysis of this phenomenon is by given by Jong-Woo [4].

In order to overcome these imperfections problems, various approaches have been presented. However, most studied approaches can only be implemented on-line. It is difficult to compensate the dead time effects perfectly by off-line methods: the switching time and voltage drops of the power devices vary with operating conditions such as the DC link voltage, phase current, operating frequency, and motor speed.

Among on-line methods, it can be quoted that presented by Ciron [5] which consist to modify adequately the reference space vector of the feeding voltage according the prediction of the phase currents. Another method is presented by Hengbing [3] which consists to adjust a factor k to minimize the currents harmonics on the filtered d and q components. One also will be able to consult the methods proposed by Jong-Woo [6] and Hyun-Soo[7], where it carried out compensation on the Park components V_{ds} and V_{qs}.

A method requiring additional hardware circuit is given in the article of Bin Zong [8]. Using this method the IGBT gate driver monitors the on/off state of the IGBT's anti-parallel diode and keeps the switch off if its parallel diode is

conducting current. The upper and lower IGBT gate drivers receive the complementary PWM signal without dead time.

In this paper a new on-line dead time and voltage drop compensation method is presented. It is based on the average-value theory, in which the lost volt-second are averaged over an entire PWM cycle and added to the reference voltage according to the direction of the load current. The power switches, are modelled by an equivalent average model, valid at the same time, for the transistor IGBT and its anti-parallels diode. For more precision, resistance of feed wires is taken into account and integrated in the equations. The proposed method is very simple for implementation under dSpace, and it provided a very good compensation compared to its simplicity.

II. Voltage Drop Analysis and Compensation

In PWM inverter system, there exist the voltage drops of the power devices that distort the output voltage and cause reduction of the fundamental component. This voltage drop can be divided in two parts; one part is constant, which is referred to the threshold value; the other is the resistance voltage drop, varying according to the load current.

If the current i_{as} flows to load ($i_{as}>0$) (Fig. 1), the pole voltage V_{a0} is defined by its switching function:

$$V_{a0} = \frac{U_c}{2} - V_{ce} \quad (\text{When } S_a = 1) \tag{1}$$

$$V_{a0} = -\frac{U_c}{2} - V_d \quad (\text{When } S_a = 0) \tag{2}$$

Where:
V_{ce} : voltage drop of the IGBT switch
V_d : voltage drop of the anti-parallel diode
S_a : 1 (upper switch is on), 0 (lower switch is on)

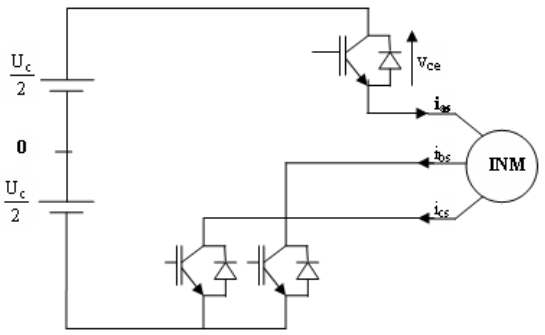

Fig. 2 Conduction sequence: $i_{as}>0$, $i_{bs}<0$, $i_{bs}<0$

If the current i_{as} flows to load ($i_{as}<0$), the pole voltage V_{a0} is varied as:

$$V_{a0} = \frac{U_c}{2} + V_d \quad (\text{When } S_a = 1) \tag{3}$$

$$V_{a0} = -\frac{U_c}{2} + V_{ce} \quad (\text{When } S_a = 1) \tag{4}$$

Then the pole voltage V_{a0} can be summarized by the following formula:

$$V_{a0} = (U_c - V_{ce} + V_d)(S_a - \frac{1}{2}) - \frac{1}{2} sign(i_{as})(V_{ce} + V_d) \tag{5}$$

The voltage drop of the active switch and the anti-parallel diode linearly increase with current. At the normal operating they can be modelled as follow:

$$V_{ce} = V_{ce0} + R_{ce}|i_{as}| \tag{6}$$

$$V_d = V_{d0} + R_d|i_{as}| \tag{7}$$

Where:
V_{ce0}: threshold voltage of the transistor
R_{ce}: conduct resistance of the transistor
V_{d0}: threshold voltage of the anti-parallel diode
R_d: conduct resistance anti-parallel of the diode

The suggested model to compensate the voltage drop is based on following simplifications:

$$(U_c - V_{ce} + V_d)(S_a - \frac{1}{2}) = \frac{U_c}{2} \tag{8}$$

$$V_{ce} + V_d = V_{ce0} + V_{d0} + R_{ce}|i_{as}| + R_d|i_{as}| = V_D + R_D|i_{as}| \tag{9}$$

Where:

$$V_D = \frac{V_{ce0} + V_{d0}}{2};\ R_D = \frac{R_{ce} + R_d}{2} + R \tag{10}$$

R: wires resistance connecting the DC link to inverter.

Then the pole voltage error is given by:

$$\Delta V_{a0} = \frac{U_c}{2} - V_{a0} = sign(i_{as})(V_D + R_D|i_{as}|) \tag{11}$$

The magnitude of the phase voltage error can be expressed as:

$$\Delta V_{an} = V_{a0} - V_{n0} = 1/3\left[2\Delta V_{a0} - \Delta V_{b0} - \Delta V_{c0}\right] =$$
$$1/3\left[2\,sign(i_{as})(V_D + R_D|i_{as}|) - sign(i_{as})(V_D + R_D|i_{bs}|)\right.$$
$$\left. - sign(i_{cs})(V_D + R_D|i_{cs}|)\right] \tag{12}$$

Phase voltage drop ΔV_{an} must be corrected at the inverter input by adding at the reference the term:

$$\Delta V_{a0ref} = 2sign(i_{as})(V_D + R_D|i_{as}|)/U_c \tag{13}$$

Matlab-Simulink diagram transcribing the equation (13) and implemented to compensate the voltage drop across the switches is given at Fig. 3.

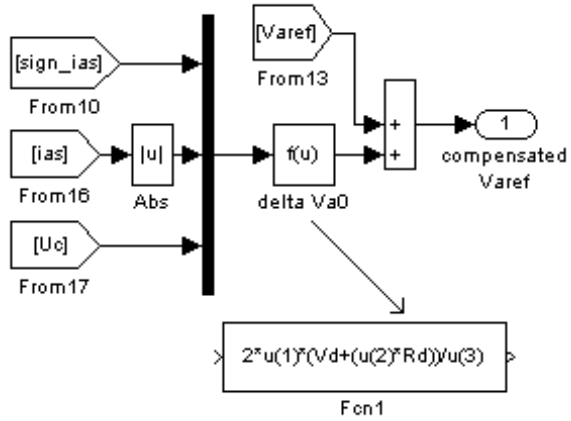

Fig. 3 Implemented Simulink-diagram to compensate the voltage drop across the power devices

The formulas and the reasoning, carried out previously, relate to the phase 'a'. These features are valid for the two other phases.

III. Dead Time Analysis and Compensation

Because of non-ideal characteristic of the switching device such as turn on/off time (t_{on}, t_{off}), the dead time T_d is a small time period during which both the upper and lower IGBT of the inverter phase leg are off. Need to be inserted in switching signals to prevent a short circuit in the DC link voltage. The dead time can causes problems such as the waveform distortion and the fundamental voltage loss of the inverter.

Fig. 4 shows the real gate signal pattern for the upper and lower switch taking account the dead time. The current i_{as} is positive. The output voltage is also shown in bottom of the figure. From this, the pole voltage (referred to middle point o of the DC link) error $\Delta V'_{a0}$ can be obtained by considering the surface A and B. Over one switching cycle T_H, it is worth:

$$\Delta V'_{a0} = \frac{1}{T_H}(S_A - S_B) = \frac{(T_d + T_{on} - T_{off})}{T_H} U_c \qquad (14)$$

A similar reasoning for a negative current, leads to the following formula:

$$\Delta V'_{a0} = \frac{1}{T_H}(S_A - S_B) = -\frac{(T_d + T_{on} - T_{off})}{T_H} U_c \qquad (15)$$

Note that if i_{as} is positive, compared with the ideal switching signal, there is a voltage loss during the dead time. By against, if i_{as} is negative, there is a voltage increase at the inverter output.

From expressions (12) and (13), the output voltage loss caused by the dead time and switching time delays can be written as follows:

$$\Delta V'_{a0} = sign(i_{as}) \frac{(T_d + T_{on} - T_{off})}{T_H} U_c \qquad (16)$$

The phase voltage error (referred to point n of the load) of become:

$$\Delta V_{an} = \frac{1}{3} \frac{(T_d + T_{on} - T_{off})}{T_H} U_c \left[-2\,sign(i_{as}) + sign(i_{bs}) + sign(i_{cs}) \right] \qquad (17)$$

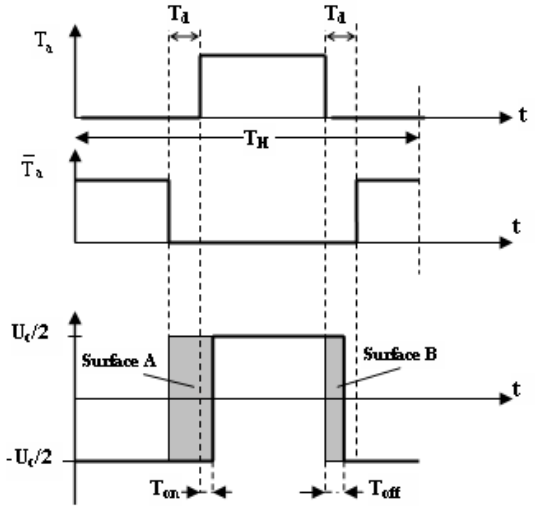

Fig. 4 Pole voltage error ΔV_{a0} for $i_{as}>0$

This voltage must be corrected at the inverter input control by modifying the reference by the term:

$$\Delta V'_{a0} ref = 2 sign(i_{as}) \frac{(T_d + T_{on} - T_{off})}{T_H} \qquad (18)$$

Note that the turn on/off time of the IGBT is given by:

$$\begin{aligned} T_{on} &= T_{d(on)} + T_r \\ T_{off} &= T_{d(off)} + T_f \end{aligned} \qquad (19)$$

Where:
$T_{d(on)}$: turn-on delay time; T_r : rise time
$T_{d(off)}$: turn-off delay time; T_f : fall time

These data can be consulted on the component's datasheet [10].

The Matlab-Simulink diagram transcribing expression (18), used to compensate, at the same time, the lag-time and voltage drop [9], is shown at Fig. 5.

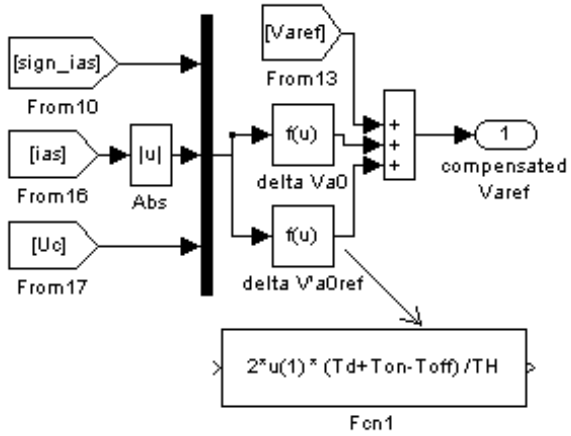

Fig. 5 Implemented Simulink diagram to compensate voltage drop and lag-time

IV. Theoretical Value of the Output Voltages

The reference voltages, applied at the inverter input control are written as the following form:

$$\begin{cases} V_{aref} = r\ \sin(\omega_s.t) \\ V_{bref} = r\ \sin(\omega_s.t\ -\ 2\pi/3) \\ V_{cref} = r\ \sin(\omega_s.t\ -\ 4\pi/3) \end{cases} \quad (20)$$

ω_s: pulsation of the reference voltage
r: PWM modulation depth ($-1 \le r \le 1$).

The corresponding phase voltages, concerning the fundamental component, are written as [11]:

$$\begin{cases} V_{an} = (r\ U_c/2)\sin(\omega_s.t) \\ V_{bn} = (r\ U_c/2)\sin(\omega_s.t\ -\ 2\pi/3) \\ V_{cn} = (r\ U_c/2)\sin(\omega_s.t\ -\ 4\pi/3) \end{cases} \quad (21)$$

V. Experimental Implementation

To valid the proposed compensation method, an experiment has been set up. dSPACE card based on a Numeric-intensive Texas instrument TMS320C31 floating point DSP is used. The control and compensation algorithms are transcribed in Matlab-Simulink. The real time interface (RTI) is used to build real time code, and to download and execute this code on dSPACE hardware [12].

For the power unit, a voltage-source insulated-gate-bipolar-transistor-based inverter has been used to feed the induction motor.

The voltages are measured by Hall Effect voltage transducers provided with forth order Butterworth low-pass filter to monitor only the fundamental signal. The filter cut-off frequency is regulated at f_c =500Hz.

The experiment is divided into three parts. The first one has been done to check the proposed compensation method for the voltage drop across the switches. In this case the dead time is not considered as the DC link voltage is chose too low and the amplitude of the reference voltage r is near 1. The other experiment concerns the validation of the lag-time compensation method. To neglect the voltage drop across the power device in front of the dead- time one, the DC link voltage is choose too high and r is selected too small. The last experiment is to observe the quantities of the machine when it functions at low speed with field oriented control. The signals waveforms are compared before and after the compensation.

The system used for the experimental checking, conceived to validate the control strategies of electric machines, is shown at Fig. 6.

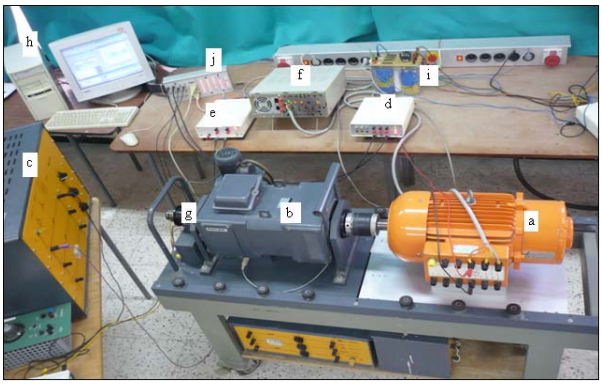

Fig. 6 Photo of the experimental system: (a: induction machine, (b,c): system of load, (d,e): current and voltage transducers, f: IGBT based-inverter, g: incremental coder, h: PC including dSPACE card, i: three-phase rectifier and capacitive filter, j: dSPACE external panel

A. Voltage Drop Compensation Results

This experiment is done under these following conditions: to minimize the dead time effect, at this stage, the DC link voltage is adjusted to a low value U_c= 30V.The PWM modulation depth is r =0.8. The power device is an IGBT power module with super-fast free-well diodes [10]. The load is a three phase induction machine of 3kW. The motor functions at low speed as the frequency of the reference voltage is choose equal to 2 Hz. The current across the motor is 4A.

The data sheet of the IGBT power module gives the following value [10]:
V_{ce0} = 1.5V R_{ce} = 0.005Ω
V_{do}= 0.8V R_d = 0.007Ω
R=0.1Ω (estimated value of the feed wires resistance)
Which yields: V_D=1.2V, R_D=0.106Ω.

Results with no compensation: Fig. 7 gives the actual and reference phase voltage waveforms before compensation. The difference between the two curves, which represent the voltage drop in the power switches, is given at Fig. 9. It can be seen that more than 20% voltage loss is introduced. We note until 3V of maximum voltage drop, knowing that, the reference voltage peak worth 12V! We can also note a

dephasing between the reference voltage and the actual voltage. A distortion of the actual signal is also noticed.

Results with compensation: Fig. 8 shows actual and desired phase voltages waveform obtained after compensation. We notice that the two curves are superimposed. The phase voltage loss becomes lower than 0.5V as shown on Fig. 9. Also, the results indicate that the phase shift is completely eliminated. It can be said that the IGBT conduct voltage drop is compensated correctly.

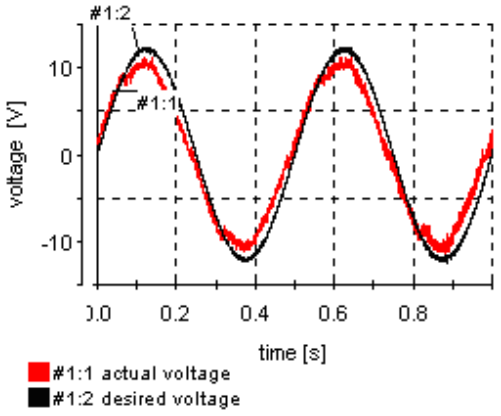

Fig. 7 Actual and reference phase voltage without compensation

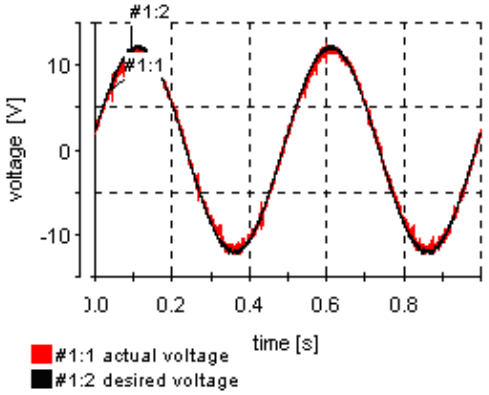

Fig. 8 Actual and desired phase voltage with compensation

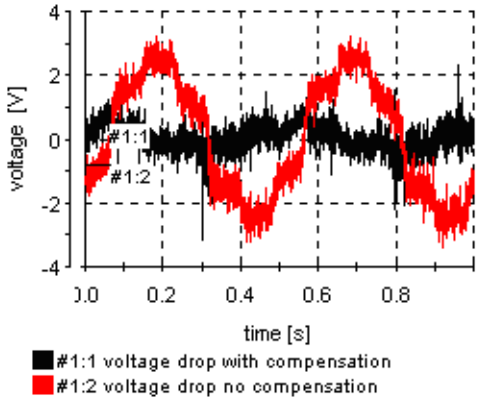

Fig. 9 Phase voltage drop ΔV_{an} without and with compensation

B. Dead Time Compensation Results

The operating conditions are: to accentuate the dead-time effect for this situation, the DC link voltage is regulated with high value U_c=180V but the PWM modulation depth is too low and worth r=0.2. To operate with a nominal flux, the motor feed frequency is chosen equal to 2Hz. To ovoid short-circuits in the inverter legs, the envisaged dead time is 4.5µs.

Moreover, the power devices data sheet gives [10]:

$T_{d(on)}$ = 250ns T_r = 350ns → T_{on} = 600ns

$T_{d(off)}$ = 300ns T_f =350ns → T_{off} = 650ns

The carrier frequency is 5 kHz yields T_H=200µs

Results with no compensation: Fig. 10 shows the actual and desired phase voltage waveforms when the delay times T_d, T_{on}, and T_{off}, are note compensated. Three important effects are to be noticed. The first is an important distortion of the actual signal. Low order harmonics are introduced. Non negligible angle shift between the two signals is also generated. Finally, appreciable voltage drop is caused by the dead-time. The peak value of the voltage loss is near 8V, knowing that the reference voltage not exceeding 18 Volts. So, there is 45% of error (See Fig. 12).

Results with compensation: Fig. 11 gives the output voltage waveforms when the delay times are taken account and compensated. The improvement is apparent. The actual voltage is almost sinusoidal and superimposed with the desired voltage. None phase shift is remained. Moreover the voltage error is reduced near 0 volt (see Fig. 12). So, the results verify the effectiveness of the proposed method.

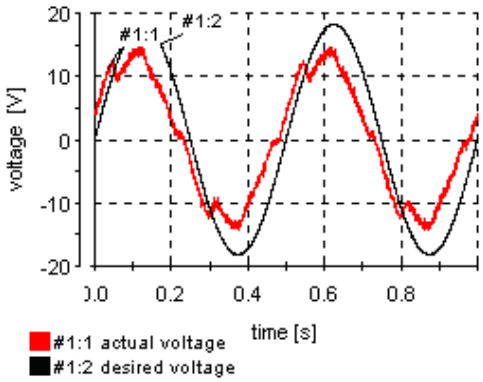

Fig. 10 Actual and desired phase voltage without compensation of dead time

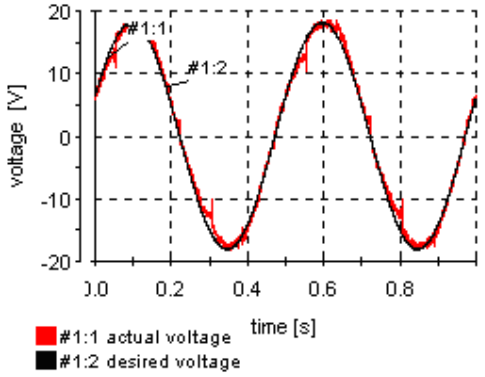

Fig. 11 Actual and desired phase voltage with dead time compensation

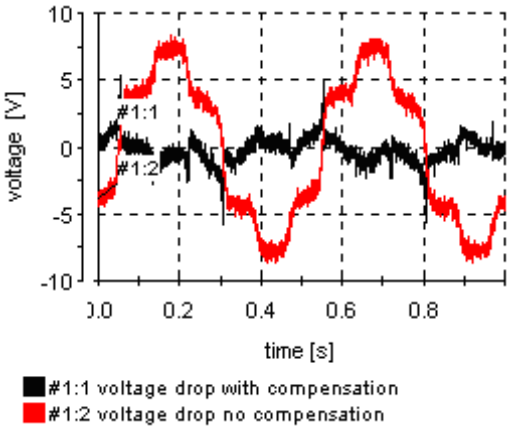

Fig. 12 Phase voltage drop without and with compensation

C. Compensation Result in Field-Oriented Speed Control Induction Machine

The aim of this experiment is to implement and check the validity of the compensation method in field-oriented speed control induction machine. The tests are done at low speed. The reference speed is varying between ±15 rpm with load.

Speed Responses experimental results, without and with compensation, are presented at Fig. 13 and Fig. 14. It can be noticed a good improvement of the speed response after the applying the compensation method.

Fig. 15 and Fig. 16 present the reference phase voltage and the measured one before and after compensation. It can be seen, at Fig. 16, a superimposition of the two waveforms when the compensation method is applied. So, the inverter nonlinearities are almost completely compensated.

In Figs. 17 and 18, the Park components V_{ds} and V_{qs} reference voltages are shown, without and with compensation. The V_{ds} component, generating the motor's magnetic flux, worth 5V before compensation and worth -2.5V after compensation. The made relative error on V_{ds} is of 300%! As for the V_{qs} component, producing the electromagnetic torque, it is worth 14V and 7V respectively without and with the compensation. The made relative error on V_{qs} is of 100!

An important conclusion can be drawn from the preceding observations: it is aberrant to replace the actual values of the v_{ds} and v_{qs} by their respective references if we do not take the care to compensate correctly the imperfections of the inverter, especially at low speeds, when the motor's applied voltages are around twenty volt or less.

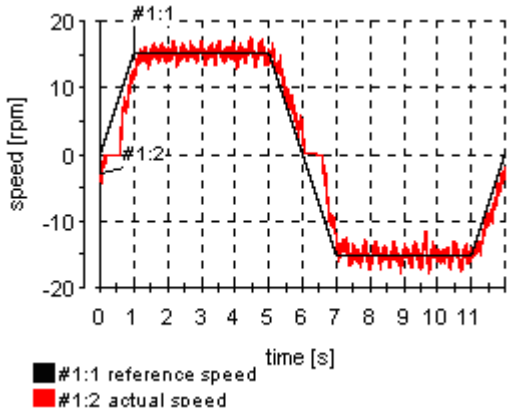

Fig. 13 Speed inversion without compensation

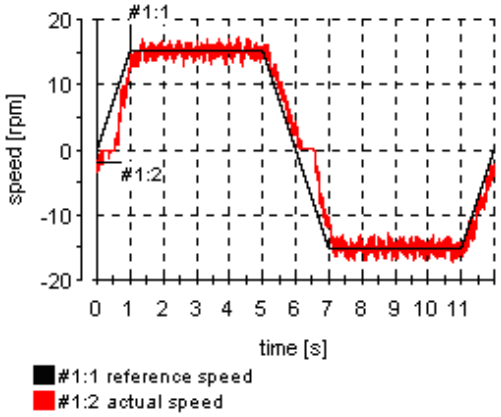

Fig. 14 Speed inversion with compensation

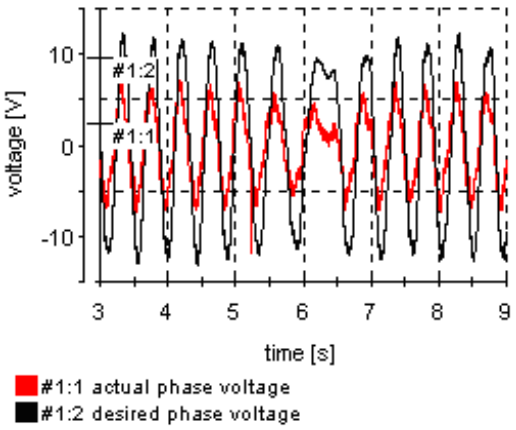

Fig. 15 Desired and actual phase voltage without compensation

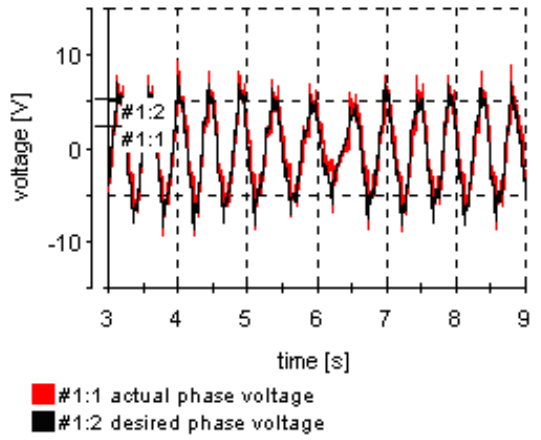

Fig. 16 Desired and actual phase voltage with compensation

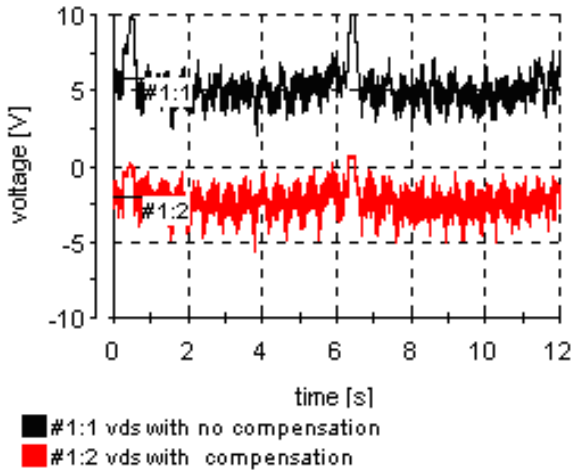

Fig. 17 Reference voltage V_{ds} with and without compensation

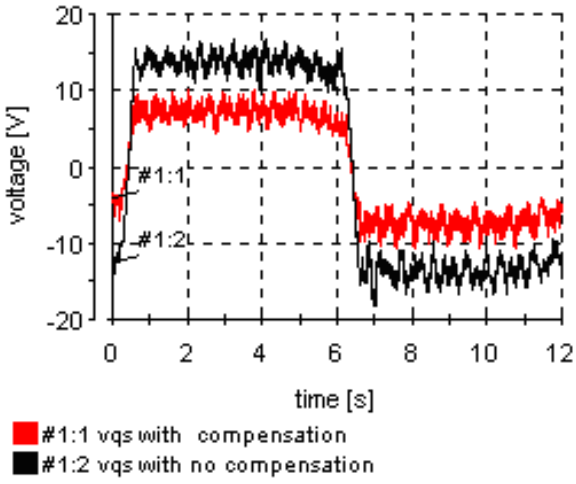

Fig. 18 Reference voltage V_{qs} with and without compensation

VI. Conclusion

In this paper the distortion voltage in PWM inverter is approached. It is caused by the non-ideal characteristics of the switches and mainly by the introduced dead time.
Moreover than waveform distortion, voltage loss and shift angle are generated on the output voltage.

To overcome these problems, an on-line compensation method is presented and checked by experiment. It is based on the average model of the power switches. The lost voltage are also averaged over an entire PWM cycle and added to the reference voltage according to the direction of the load current.

Experimental results show considerable improvement in the output voltage. The waveforms became sinusoidal and the voltage drops are close to zero. Thus, the validity of the proposed method is verified.

The proposed method produces the same inverter output voltages as the reference voltages. A high performance vector control induction machine drive can operate, even in the low speeds range, without phase voltage measurements and only with the usual two current measurement transducers.

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