International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:3, No:3, 2009

Gate Tunnel Current Calculation for NMOSFET Based on Deep Sub-Micron Effects

Ashwani K. Rana, Narottam Chand, Vinod Kapoor

***Abstract*—**Aggressive scaling of MOS devices requires use of ultra-thin gate oxides to maintain a reasonable short channel effect and to take the advantage of higher density, high speed, lower cost etc. Such thin oxides give rise to high electric fields, resulting in considerable gate tunneling current through gate oxide in nano regime. Consequently, accurate analysis of gate tunneling current is very important especially in context of low power application. In this paper, a simple and efficient analytical model has been developed for channel and source/drain overlap region gate tunneling current through ultra thin gate oxide n-channel MOSFET with inevitable deep submicron effect (DSME).The results obtained have been verified with simulated and reported experimental results for the purpose of validation. It is shown that the calculated tunnel current is well fitted to the measured one over the entire oxide thickness range. The proposed model is suitable enough to be used in circuit simulator due to its simplicity. It is observed that neglecting deep sub-micron effect may lead to large error in the calculated gate tunneling current. It is found that temperature has almost negligible effect on gate tunneling current. It is also reported that gate tunneling current reduces with the increase of gate oxide thickness. The impact of source/drain overlap length is also assessed on gate tunneling current.

***Keywords*—**Gate tunneling current, analytical model, gate dielectrics, non uniform poly gate doping, MOSFET, fringing field effect and image charges.

I. Introduction

THE advance in complexity and efficiency of CMOS design has been achieved throughout the last decades by scaling the geometric dimensions of the metal oxide-semiconductor field-effect-transistor (MOSFET)[1]. Reducing the gate length increased drive currents while it also necessitates a decrease of the gate oxide thickness to maintain electrostatic control of the charges induced in the channel [1]. Today the oxide layer thickness have reached the nanometer range, causing unwanted effects like gate leakage currents to become increasingly important and adversely affect the device behavior[2]. As the thickness of gate oxide layer decreases, the gate current increases in an exponential manner. This increase in current not only adversely affects the performance of the device but also increases the off-state power dissipation of a highly integrated chip. Thus, predicting the gate tunneling current is important for the development of advanced MOS devices in nano regime. The first principle computation are based upon the self-consistent solution of Poison's and Schrodinger equation, gives a valuable insight into the underlying physics of the tunneling mechanism [3]-[6]. However, a full solution of above mechanism is highly computationally intensive and hence not feasible within a compact modeling context where high computational efficiency is required.

The gate leakage current is very important in ensuring the performance of any designed VLSI circuits and is believed to be one of the most constraining limits for continued down scaling of silicon dioxide as a gate dielectric [7]. In ultra short nano scale MOSFETs, the source/drain extension (overlap region) under poly silicon gate represents a significant fraction of the device as they do not scale with the same rate as the gate length [8].The overlap component of the gate tunneling current dominates over the small gate bias since the gate oxide field is much stronger in the overlap region as compared to the channel region. Hence accurate estimation of this gate leakage current component is essential to appreciate the total off-state power dissipation.

Numerous models have been developed numerically [8], [9] in the past for calculating the tunneling current, but this approach is not always practical and is timing consuming. Schuegraf *et al* [10-11] have derived a simple analytical formula to represent direct tunneling through a trapezoidal barrier. However, this model suffers from various limitations such as (i) gate current dies not approach to zero as gate voltage goes to zero and does not fit experimental data at sub 1-V gate bias range (ii) the assumption of constant effective mass for all energies is not accurate (iii) non consideration of quantum effects. Lee and Hu [12-13] proposed a semi-empirical model by introducing the correction function to Schuegraf's analytical model to take care of above-mentioned secondary effect. However, this model has not considered the edge direct tunneling current (EDT). In [14], direct tunneling current expressions have been developed both for channel gate tunneling current and EDT including poly-depletion effect and quantization effect with a four adjustable parameter. This model does not include (i) the non-uniform dopant profile in poly-gate in vertical direction resulted due to low energy ion implantation, (ii) gate oxide barrier lowering due to image charges across the Si/SiO_2 interface. These deep sub-micron effect (DSME) are inevitable for nano scale

Ashwani K. Rana is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur-177005, H.P., India, (corresponding author to provide phone: 91-01972-304638; fax: 92-01972-223834; e-mail: ashwani@ nitham.ac.in).

Narottam Chand is with Department of Computer Science and Engineering, National Institute of Technology, Hamirpur-177005, H.P., India (e-mail: nar@nitham.ac.in).

Vinod Kapoor is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur-177005, H.P., India, (e-mail: kapoor@nitham.ac.in).

devices operating into deep sub-50 nm regime. Therefore, it is mandatory to include these DSME effects in nano scale MOSFET to achieve an accurate estimation of gate tunneling current.

In present work, an effective and compact model has been developed for analyzing the gate tunneling current of nano scale NMOSFET through sub-1nm gate oxide by considering the DSME effect that are difficult to ignore at nano scale regime.

The rest of the paper is organized as follows. In Section II, the impact of the inevitable deep sub-micron (DSME) effect on gate tunnel current are presented. In Section III, modeling of the gate tunneling current is established. The device structure and design used for simulation set up is presented in Section IV. The results obtained are discussed in Section V. Finally, concluding remarks are offered in Section VI.

II. IMPACT OF NANOSCALE EFFECT (NSE) ON GATE TUNNELING CURRENT

This section evaluates the impact of deep sub-micron effect on gate tunneling current as these effect are inevitable when MOSFET is driven in nano domain.

A. Impact of Nonuniform Dopant profile in Poly gate

It is discussed in [15] that with device scaling low energy implants are prevalent to attain ultra shallow source/drain junctions and to prevent dopant penetration through thinner poly-silicon gate. As a result the dopant activation anneals are constrained to minimize dopant diffusion through gate oxide. This, in turn, can potentially cause a highly non-uniform vertical dopant distribution in poly-silicon gate due to limited dopant diffusion. A non-uniform distribution of the dopants in poly-silicon gate, as a function of position from the top to the gate oxide interface with the corresponding energy-band diagram is shown in Fig. 1.

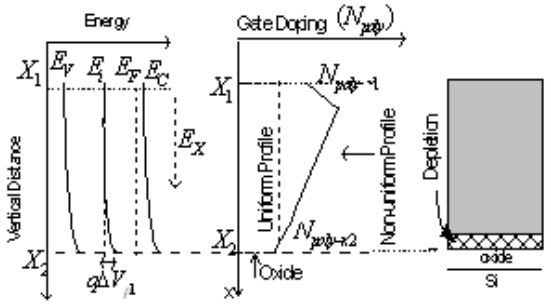

Fig.1. Nonuniform dopant distribution in vertical direction and corresponding band diagram, showing built-in electric field (E_x) and potential drop in poly-gate region.

An doping profile due to uniform doping in poly gate and due to some arbitrary doping in poly gate have been simulated in the Santaurus simulator as shown in Fig. 2 and Fig. 3 respectively. An estimate of the potential drop due to the non-uniform graded dopant profile (arbitrary doping profile) in vertical direction in poly-silicon gate has been calculated to be 0.12 V (Fig. 4 when N_d changes by two orders of magnitude. (say from 10^{22}cm^{-3} to 10^{20} cm^{-3}).

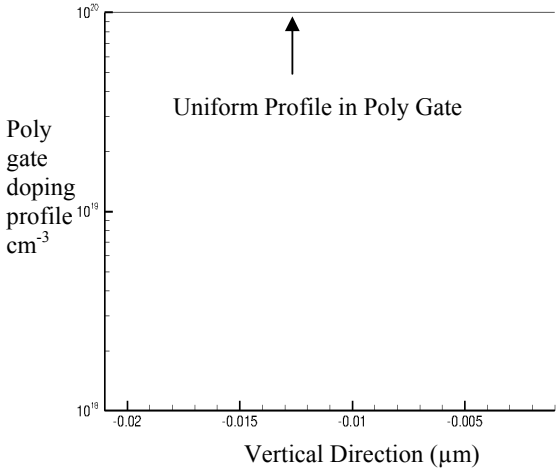

Fig. 2. Uniform poly gate dopant profile in vertical direction for dopant density of 10^{20} cm^{-3}

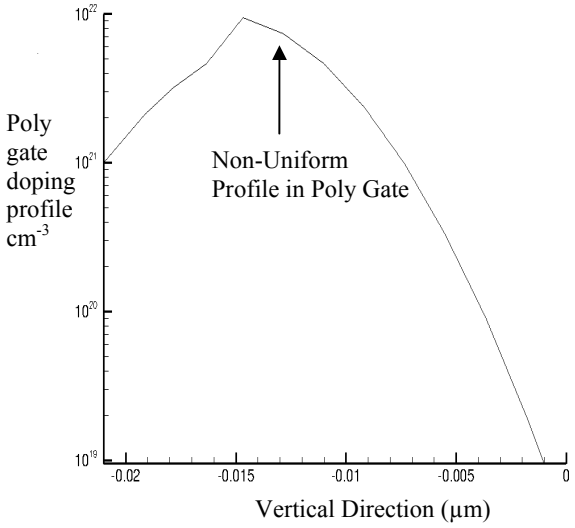

Fig. 3. Non-Uniform poly gate dopant profile(arbitrary doping profile) in vertical direction for dopant density from10^{22} cm^{-3} to 10^{20} cm^{-3}

This is an additional voltage drop across the poly-silicon-gate as compared to voltage drop of uniform doping profile at 10^{20}cm^{-3}, even though both the profiles have the same dopant concentration at the oxide interface. This additional voltage drop needs to be included in the modeling of the gate leakage current.

B. Impact of Image Force Barrier Lowering

The emission of electron from Si to SiO_2 causes build up of image charge at the oxide side of the Si–SiO_2 interface as

carrier approaches the Si-SiO_2 interface. The potential associated with these charges reduces the effective barrier height. This barrier reduction tends to be rather small compared to the barrier height itself. Nevertheless, this barrier reduction is of interest since it depends on the applied voltage and doping in the semiconductor. The barrier lowering increases with an increasing external field applied across the oxide and doping level of the substrate. The image force induced barrier lowering is usually small in non degenerate semiconductors, as well as in relatively thick insulator layers. Note that this barrier lowering is only experienced by a carrier while approaching the interface and will therefore not be noticeable in a capacitance-voltage measurement. The band diagram showing the image force induced barrier lowering is shown in Fig. 5.

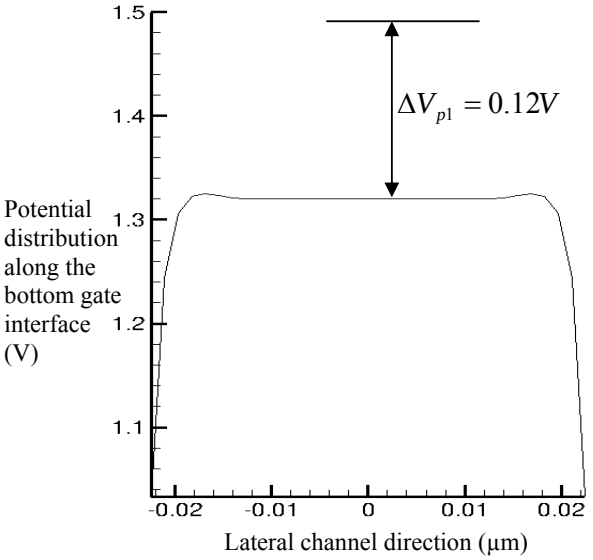

Fig. 4. Potential distribution along the bottom gate interface, showing the drop of 0.12 V due to non uniform doping profile in the poly gate.

The calculation of the barrier reduction assumes that the charge of an electron close to the oxide-semiconductor interface attracts an opposite surface charge, which exactly balances the electron's charge so that the electric field surrounding the electron does not penetrate beyond this surface charge. The time to build-up the surface charge and the time to polarize the semiconductor around the moving electron are assumed to be much shorter than the transit time of the electron. This scenario is based on the assumption that there are no mobile or fixed charges around the electron as it approaches the metal-semiconductor interface. The electron and the induced surface charges are shown in Fig. 6.

It can be shown that the electric field in the semiconductor is identical to that of the carrier itself and another carrier with opposite charge at equal distance but on the opposite side of the interface. This charge is called the image charge. The difference between the actual surface charges and the image charge is that the fields in the metal are distinctly different. The image charge concept is justified on the basis that the electric field lines are perpendicular to the surface of a perfect conductor, so that, in the case of a flat interface, the mirror image of the field lines provides continuous field lines across the interface.

Since the experimental results [16] exhibit a behavior proportional to the square root of the applied oxide field, the classical image force theory is considered to be valid. Therefore, The reduction in the barrier height at the Si–SiO_2 interface from ϕ_b = 3.15 eV by an amount $\Delta\phi_b$ is given [17,18] by

$$\Delta\phi = \sqrt{\frac{qE_{ox}}{4\pi\varepsilon_{ox}}} = \sqrt{\frac{qV_{ox}}{4\pi\varepsilon_{ox}T_{ox}}} = \left(\frac{2q^3 N_{eff}\phi_{bs}}{16\pi^2\varepsilon_{ox}^3}\right)^{1/4} \quad (1)$$

Therefore, effective gate oxide barrier becomes

$$\phi_{b\_eff} = \phi_b - \Delta\phi \quad (2)$$

where is the permittivity of SiO_2 and ϕ_b is the oxide barrier height without image force induced barrier lowering. This is called the image-force-induced barrier-lowering effect. Since it modulates the barrier height, it also modulates the gate tunneling current, as the tunneling exponentially depends on barrier height of gate oxide (Φ_{ox}).

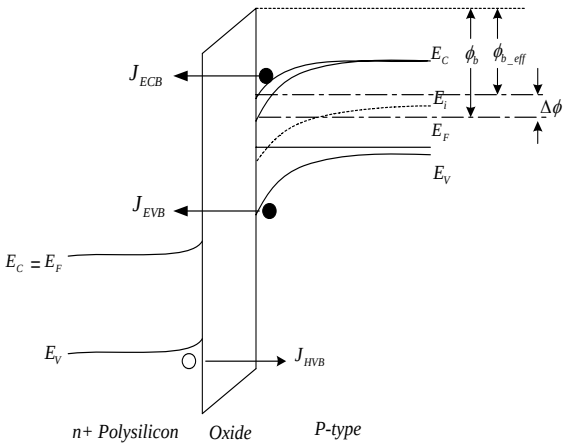

Fig. 5 Energy Band Diagram, showing the oxide interface barrier lowering due to image charges

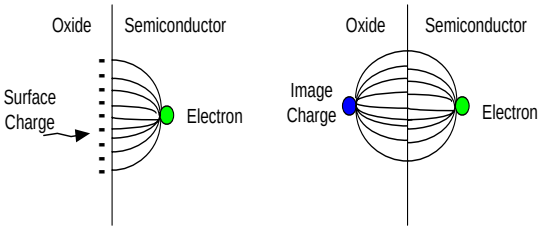

Fig. 6. The electron and the induced surface charges representation

III. ANALYTICAL MODEL FOR GATE TUNNELING CURRENT

In ultra short-channel MOSFETs, in addition to gate to channel direct tunneling current, the source/drain extensions (overlap regions) direct tunneling current known as edge direct tunneling current (EDT) has been identified as the principal source of off-state power dissipation in VLSI chips because source/drain extensions (overlap regions) under poly-silicon gate represent a significant fraction of the device as they do not scale at the same rate as gate length [19]. Therefore, the evaluation of EDT is critical for state of the art MOSFETs. Modeling of the direct tunneling current analytically have been largely based on the WKB approximation [10].The discrepancies that were present in the original WKB approximation [10] has been rectified in [12],[13] by introducing few adjusting parameters. This model is more consistent and covers the entire gate bias range. The robustness of the model has been verified with experimental and numerical data. In our work, we adopt this model to evaluate the direct tunneling current from channel and overlap region in nano scale regime where poly gate dopant non-uniformity, gate length effects and gate oxide barrier lowering due to image charges across the Si/SiO_2 interface can not be ignored. In this scheme, the value of α for channel and overlap region has been used as 0.6 and 0.45 respectively to match the overall best fit with Santaurus simulation and also with the experimental results reported in [14].The T_{ox} refers to the physical oxide thickness and effective mass of the carrier in the oxide has been used as 0.40 m_o through this work. The total gate leakage current is given by

$$I_g = I_{gc} + I_{gso} + I_{gdo} \tag{3}$$

where I_{gc} is the gate-to-channel tunneling current, I_{gso} is the gate-to-source overlap region gate tunneling current and I_{gdo} is the gate-to-drain overlap region tunneling current. Since drain to source V_{ds} is taken to be zero for simplification, so I_g can be modified as below

$$I_g = I_{gc} + I_{ov}; I_{ov} = 2I_{gso} \tag{4}$$

The channel current I_{gc} and EDT current I_{ov} per micrometer can be written as:

$$I_{gc} = J_{ch} \times L_{eff} \tag{5}$$

$$I_{ov} = J_{ov} \times L_{ov} \tag{6}$$

The effective channel length is given as

$$L_{eff} = L_g - 2L_{ov} \tag{7}$$

where L_g is the total gate length, L_{ov} is the overlap gate length and L_{eff} is the effective gate length The channel current density (J_{ch}) and overlap current density (J_{ov}) are modeled as follows.

$$J_{(ch,ov)} = AC_{F(ch,ov)}T_{WKB(ch,ov)} \tag{8}$$

where $A = \dfrac{q^3}{8\pi\phi_b\varepsilon_{ox}}$, $C_{F(ch,ov)}$ is the correction term incorporated in [12], [13] and $T_{(ch,ov)}$ is the modified WKB transmission probability and are modified for channel and overlap region as follows:

$$C_{(ch,ov)} = \exp\left[\frac{20}{\phi_{b\_eff}}\left(\frac{|V_{ox(ch,ov)}| - \phi_{b\_eff}}{\phi_{b\_eff}} + 1\right)^{\alpha(ch,ov)}\left(1 - \frac{|V_{ox(ch,ov)}|}{\phi_{b\_eff}}\right)\left(\frac{V_g}{Tox}\right)\right] N_{DTC(ch,ov)} \tag{9}$$

$$T_{WKB(ch,ov)} = \exp\left[\frac{-8\pi\sqrt{2m_{ox}}\phi_{b\_eff}^{3/2}\left[1 - \left(1 - \dfrac{|V_{ox(ch,ov)}|}{\phi_{b\_eff}}\right)\right]^{3/2}}{3hq|E_{ox(ch,ov)}|}\right] \tag{10}$$

$$N_{DTC(ch)} = \begin{cases} \dfrac{\varepsilon_{ox}}{t_{gi}}\left\{n_{acc}v_t.\ln\left[1 + \exp\left(-\dfrac{(V_g - V_{FB})}{n_{acc}v_t}\right)\right]\right. \\ for V_g < 0 \\ \dfrac{\varepsilon_{ox}}{t_{gi}}\left\{n_{inv}v_t.\ln\left[1 + \exp\left(-\dfrac{(V_g - V_{th})}{n_{inv}v_t}\right)\right]\right. \\ for V_g > 0 \end{cases} \tag{11}$$

$$N_{DTC(ov)} = \begin{cases} \dfrac{\varepsilon_{ox}}{t_{gi}}\left\{n_{acc}v_t.\ln\left[1 + \exp\left(-\dfrac{V_g}{n_{acc}v_t}\right)\right]\right. \\ for V_g < 0 \\ \dfrac{\varepsilon_{ox}}{t_{gi}}\left\{n_{acc}v_t.\ln\left[1 + \exp\left(-\dfrac{V_{ge}}{n_{acc}v_t}\right)\right]\right. \\ for V_g > 0 \end{cases} \tag{12}$$

Where α is the fitting parameter depending upon channel or source/drain overlap tunneling, n_{inv} and n_{acc} are the swing parameters, V_{FB} represents the flat band voltage, $N_{DTC(ch,ov)}$

denotes the density of carrier in channel /overlap region depending upon MOSFET biasing condition and V_{ge} is the effective gate voltage excluding poly gate non-uniformity and gate length effect and is equal to $V_g - V_{poly}$.

The default values of n_{inv} and n_{acc} are S/v_t (S is the sub threshold swing) and 1 respectively. The correction factor ($C_{F(ch,ov)}$) and transmission probability $\left(T_{WKB(ch,ov)}\right)$ are different for channel and source/drain overlap region because both channel and overlap component have different value of $V_{ox(ch,ov)}$ and $N_{DTC(ch,ov)}$. It is because of the fact that overlap region has almost zero flat band voltage as both SDE region and overlying poly-gate Si are heavily doped n^+ regions. The $N_{DTC(ch,ov)}$ has been given differently for both region as in eqns.(11) and (12). The gate oxide voltage (V_{ox}) for the channel and SDE overlap are calculated as follows.

Case (i): when $V_g > 0$

In this biasing condition MOSFET device, there is a depletion layer in the poly gate thereby causing an additional potential drop across the gate. The SDE region enters into accumulation and substrate region enters into the week inversion below V_{th} and strong inversion beyond V_{th}.Therefore both the channel and EDT component are present and are comparable.

Case (ii): when $V_{FB} < V_g < 0$

Here, gate tunneling current is dominated by the EDT where electric field is such that electron are directed from the accumulated poly-gate into the overlap region. On other hand, substrate is in depletion /weak inversion and constitutes negligible tunneling current. This region of biasing is primarily responsible for off-state power dissipation. Thus, EDT plays an important role in the evaluation of off-state power dissipation

Case (ii): when $V_g < V_{FB}$

In this region of operation, substrate goes into accumulation. As a result both current components become comparable. The voltage across the gate oxide for different region of operation is as follows.

$$V_{gi} = \begin{cases} (V_g - \phi_s - V_{FB}) \, for V_g < 0 \\ (V_{ge} - \phi_s - V_{FB}) \, for V_g > 0 \end{cases} \quad (13)$$

Where ϕ_s is the surface band bending of the substrate and are calculated for channel and overlap region depending upon the biasing condition of the MOSFET device including the poly non-uniformity, gate length effects and image force barrier lowering.

The accurate surface potentials expressions in case of channel in weak inversion/depletion, strong inversion and in accumulation can be taken from [20]. The surface potential in accumulation in the overlap region has been derived as follows. This expression excludes the effect of minority carrier in the heavily doped overlap region.

$$\phi_{s(acc)}^{ov} = \frac{\left(V_g - V_{FB(ov)}\right) - \beta_{ov}}{1 - \frac{\beta_{ov}}{2v_t}} \quad (14)$$

Where $\beta_{ov} = \gamma_p \sqrt{v_t}$ (15)

$$\gamma_p = \frac{\sqrt{2\varepsilon_{si} q N_{ploy}}}{C_{ox}} \quad (16)$$

The ϕ_s takes a sign of positive or negative depending upon the band bending in the substrate/overlap region. The gate effective voltage including the effect of nonuniform dopant distribution in the gate is derived as follows.

$$\therefore V_{ge} = (V_{FB} + \phi_{so} - \Delta V_{p1} - \Delta V_{p2}) + \frac{\left(q\varepsilon_{si} N_{poly} T_{ox}^2\right)}{\varepsilon_{ox}^2}\left[\sqrt{1 + \frac{2\varepsilon_{ox}^2 (V_g - V_{FB} - \phi_{so})}{q\varepsilon_{si} N_{poly} T_{ox}^2}} - 1\right] \quad (17)$$

This equation includes the non uniformity in the gate dopant profile through a term ΔV_{p1} and fringing field effect *i.e* gate length effect through a term ΔV_{p2}. The ϕ_s by taking the quantization effect into account, is given [21] as follows

$$\phi_{so} = 2\phi_b + \Delta\phi_s^{QM} - V_{BS} \quad (18)$$

where $\Delta\phi_s^{QM}$ can be taken from [20]

IV. SIMULATION SET UP

Fig. 7 shows the schematic of device structure of N-MOSFET used in this study. The deep S/D region is composed of a heavily doped silicon and a silicide contact. The doping of the silicon S/D region is assumed to be very high, $1x10^{20}$ cm^{-3}, which is close to the solid solubility limit and introduces negligible silicon resistance. The dimension of the silicon S/D region is taken as 20 nm long and 50 nm high. This gives a large contact area resulting in a small contact resistance.

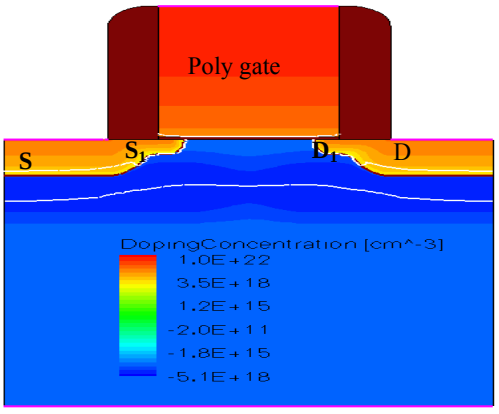

Fig. 7. NMOSFET device structure used in simulation

The heavily doped silicon called deep S/D region extend into the silicon film at both ends and constitute the extended S/D for the device. The lengths of these extended regions at both ends are equal and are denoted by S_1 and D_1. S/D implantation is performed after defining the gate and the oxide spacer. Boron ions were implanted into the channel region to reduce the leakage current and to keep a low accepter concentration in the non-overlapped channel region. The doping concentration of the acceptors in silicon channel region is assumed to be graded due to diffusion of dopant ions from heavily doped S/D region with a peak value of $1x10^{18}$ cm^{-3} and $1x10^{17}$ cm^{-3} near the channel. The halo implantation done around the S/D also reduces short-channel effects, such as the punch-through current, DIBL, and threshold voltage roll-off, for different non-overlap lengths.

The MOSFET has a 50-nm-thick n+ poly-Si gate with metallurgical gate length of 25 nm and a 1-nm gate oxide. The oxide spacer has been assumed to reduce the gate capacitance. Here, Lo represents the overlap length, which is controlled by the S/D implantation energy. Lo = 5 nm optimized with off current is used in this work. The MOSFET with L_{met} of 25 nm was designed to have a V_T of 0.23 V. We determined V_T by using a linear extrapolation of the linear portion of the I_{DS}-V_{GS} curve at low drain voltages. The operating voltage for the devices is 1V. The simulation study has been conducted in two dimensions, hence all the results are in the units of per unit channel width.

MOSFET devices in nano regime are characterized by several aspects typical of the nanometer scale: short channel effects, quantum confinement in the channel, tunnel current through the gate dielectric, source-to-drain tunnel current, inelastic scattering along the channel and far-from-equilibrium transport. From this point of view TCAD models [21] that are adequate to represent the device physics appropriately during simulation at nano regime are included. There are several model in literature that addresses the problem in different way. Along the transport direction, however, Santaurus (TCAD Simulator) provides the choice of four different transport models: (i) drift-diffusion (DD) model, (ii) thermodynamic (TD) transport model (iii) hydrodynamic (HD) transport model and (iv) Quantization models- Among them drift-diffusion model simulation runs the fastest, however, does not take care of quantum effect for nano devices. Thermodynamic transport (TDT) model is suitable for the simulation of power devices. Hydrodynamic transport (HDT) is especially useful in simulating devices ranging from deep-submicron MOSFETs beyond 0.18µm generation and hetrostructure. It includes the simulation of non local effects such as velocity overshoots and substrate current levels. Quantization model Density gradient transport(DGT) on the other hand has three different models: (i) van Dort model(VD)model, (ii) density gradient (DG) model and (iii) modified local-density approximation (MLDA) model. They differ in physical sophistication, numeric expense and robustness. The van Dirt model is numerically robust, fast and well describes the terminal characteristics but does not give correct density distribution in the channel. Density gradient (DG) model is numerically robust but significantly slower than the van Dort model. It, however, gives reasonable description of the terminal characteristics and charge distribution inside the device and also describe the 2D and 3D quantization effects. The modified local-density approximation (MLDA) model is numerically robust and fast model but it sometimes fails to calculate the accurate carrier distribution in the saturation region because of its one-dimensional characteristics. Comparison of some of these transport models can be found elsewhere [22]

Scattering inside the intrinsic device is treated by a simple Brooks–Herring model, which gives a phenomenological description of scattering. This simple model can capture the essential physics realistically. Due to heavy doping of the extended S/D inside the intrinsic device and due to its graded nature along the channel, a doping dependent mobility is expected. For this reason, the Canali model which originates from the Caughey–Thomas formula, but has temperature-dependent parameters, is used. Thus, the simulation of the device is performed by using Santaurus design suite with drift-diffusion, density gradient quantum correction and advanced physical model being turned on.

V. RESULTS AND DISCUSSION

Computation have been carried out for a n-channel fully depleted nanoscale MOSFET to estimate the gate tunneling current due to overlap of source/drain region with gate area overlap in addition to gate-to-channel component of gate tunneling current.

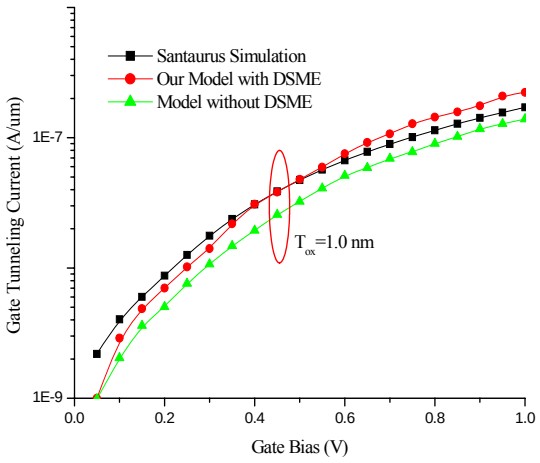

Fig. 8. Comparison of model with simulated data for gate oxide thickness of T_{ox} = 1.0 nm, metallurgical gate length of L_{met}=25nm and S/D overlap length of L_{ov}=10 nm in nano scale regime

The impact of nanoscale effect (NSE) on gate leakage current has been evaluated. The source/drain overlap length of the nano device under consideration is optimized with regard to off current of the device. The variation of gate tunneling current with source/drain overlap length for a given values of gate bias and oxide thickness has been presented. The variation of gate tunneling current with temperature and substrate bias for a given values of gate bias and oxide thickness has, also, been presented. Further, the variation of

gate leakage current with gate bias for different value of substrate doping has been reported in the results. The variation of gate tunneling current with and without halo doping is also observed.

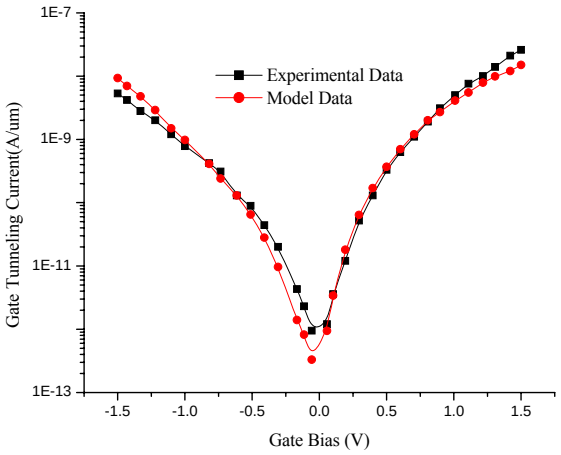

Fig. 9 . Comparison of the model with experimental data for N_{sub}=4.1x1017(cm^{-3}) and N_{Poly}=5x1019 cm^{-3}

The comparision between the simulated data and the model value for gate tunneling current is presented in Fig. 8. for value L_{met} = 25 nm, L_{ov}=10 nm, T_{ox}=1.0 nm. The substrate doping has been taken to be 1x10^{17} cm^{-3} while that of polysilicon gate is 1x10^{22} cm^{-3} at the top and 1x10^{20} cm^{-3} at bottom of the polysilicon gate i.e. interface of oxide and silicon. The model value while considering the nano scale effect shows good agreement with the simulated value over the entire positive gate bias range, certifying the high accuracy of the propsed analytical modelling. It is also shown that model value without nano scale effect(NSE) does not shows good agreement with simulated value, emphasizing the need of inclusion of nano scale effect.

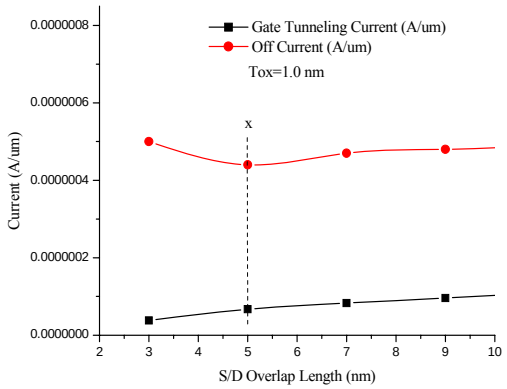

Fig. 10. Gate tunneling current and off current vs gate bias for T_{ox}=1.0 nm, N_{sub} = 1x10^{17} m^{-3}, L_{met}=25nm and L_{ov}=10nm in nano scale regime

Similarly, the model is also verified in Fig. 9. with experimental data published in [12] for value L_g=0.17 µm, L_{ov}=10 nm ,T_{ox}=1.85 nm and W_g=10 µm. The substrate doping and polysilicon gate doping has been taken to be 4.1x10^{17} cm^{-3} and 5x10^{20} cm^{-3} respectively. The model value also shows good agreement with the experimental data over the entire gate bias range , certifying the high accuracy of the propsed analytical modelling.

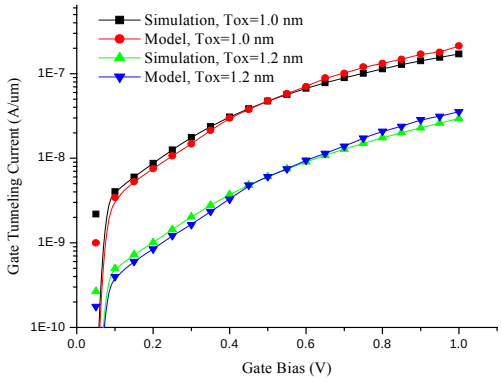

Fig. 11. Gate tunneling current vs gate bias for different gate oxide thickness in nano scale regime at L_{met}=25nm and L_{ov}=5.0 nm

Fig. 10. shows the variation of the gate tunneling current and off current of the NMOS device with S/D overlap length for optimization of S/D overlap length at a given gate bias of 0.6 V and gate oxide thickness of 1.0 nm. It is observed that off current for a device under consideration is slightly less at S/D overlap length of 5 nm. Therefore, S/D overlap length of 5.0 nm is considered for the further simulation and model data calculation.

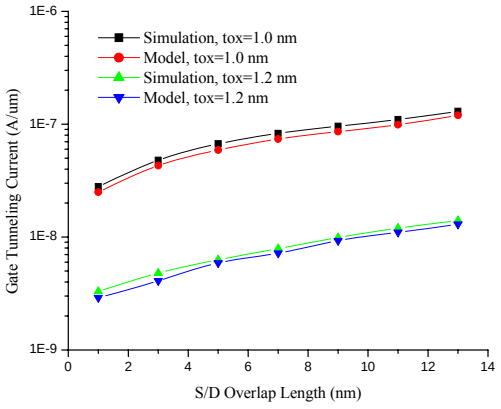

Fig. 12. Gate tunneling current vs S/D overlap length for different gate oxide thickness in nano scale regime at V_g=0.6 V, L_{met}=25nm and L_{ov}=5.0 nm

The I_g-V_g characteristics for various gate oxide thicknesses are shown in Fig. 11. It can be observed that gate tunneling current increases exponentially with increase in the gate bias and decreases with increase in gate oxide thickness. This is because electric field responsible for gate tunneling increases with increases in gate bias and decrease with gate oxide thickness. It can also be seen that for a gate bias of zero volt,

the gate tunneling current shows a drastic reduction. This is because of the fact that the transverse electric filed gets reduced substantially at such an applied gate bias. It is further observed that at high gate biases, there is a tendency of saturation of gate tunneling current.

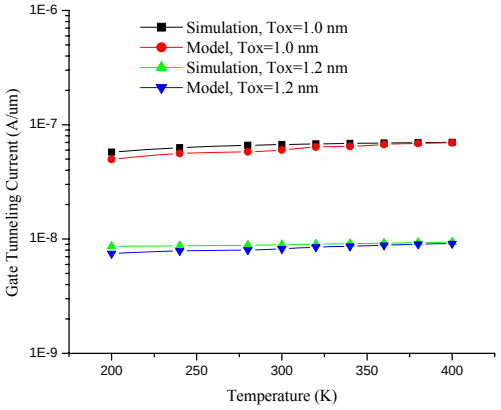

Fig. 13. Gate tunneling current vs temperature for different oxide thickness in nano scale regime at V_g=0.6 V, L_{met}=25nm and L_{ov}=5.0 nm

In Fig. 12., the scalability of the gate overlap length has been presented in context of gate leakage current. The gate leakage shows increasing trend with gate to S/D overlap length. Since gate tunneling current through S/D overlap region is comparable with channel-to-gate region current at nano domain, therefore, gate leakage current increases as the area of S/D overlap region increases because it tends to increase the charge carrier concentration which is responsible for tunneling. It is desirable to minimize the overlap length particularly in those applications where leakage requirements are very restrictive.

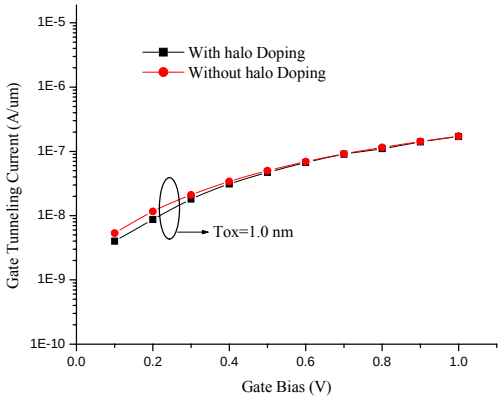

Fig. 14. Gate tunneling current vs gate bias in nano scale regime for T_{ox} = 1.0nm, V_g=0.6 V, L_{met}=25nm and L_{ov}=5.0 nm

Fig. 13 shows the variation of the gate leakage current with temperature in an NMOS transistor for different gate oxide thickness at a given gate bias . The gate leakage current is almost insensitive to temperature variation since the electric field across the oxide does not strongly depend upon the temperature.

Halo doping for modern MOS devices has been used widely around the S/D to reduces short-channel effects, such as the punch-through current, DIBL, and threshold voltage roll-off and their effect on tunneling current cannot be overlooked. Fig. 14 shows the variation of the gate leakage current with gate bias for a given oxide thickness of T_{ox} = 1.0 nm with and without halo doping. The gate leakage current is almost insensitive to halo doping because carrier concentration in channel region does not strongly depend upon the halo doping.

VI. CONCLUSION

We have derived an analytical model of gate tunnel current in nano domain through ultrathin gate oxides under the conditions that the effective mass approximation holds. It is reported that the ignorance of deep sub-micron (DSME) effect while modeling the gate leakage current may lead to serious error during the analysis of VLSI circuits. It is found that the source/drain overlap length of the nano device has to be taken into account particularly in those applications where off-state power plays an important role in determining the performance of the device. The results also indicate that gate leakage current is almost insensitive to temperature variation and halo doping.

REFERENCES

[1] H.S.P. Wong, D.J. Frank, P.M. Solomon, C.H.J. Wann, J.J. Welser, Proc. IEEE 87 (4) (1999) 537.

[2] SIA: ITRS Roadmap, 2005 Edition.

[3] C. -H. Choi, K. Y. Nam, Z. Yu, and R. W. Dutton, "*Impact of gate direct tunneling current on circuit performance: A simulation study*," IEEE Trans. Electron Devices, vol. 48, pp. 2823–2829, Dec. 2001.

[4] F. Rana, S. Tiwari, and D. Buchanan, "*Self-consistent modeling of accumulation layers and tunneling currents through very thin oxides,*" Appl. Phys. Lett., vol. 69, pp. 1104–1106, 1996.

[5] S. -H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "*Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFETs,*" IEEE Electron Device Lett., vol. 18, pp. 209–211, May 1997.

[6] W. -K. Shih et al., "*Modeling gate leakage current in nmos structures due to tunneling through an ultra-thin oxide,*" Solid State Electron., vol. 42, pp. 997–1006, June 1998.

[7] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "*Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits,*" Proceedings of the IEEE, vol. 91, no. 2, pp. 305-327, Feb. 2003.

[8] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, "*Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors,*" in Tech. Dig. VLSI Sym., 2000, pp. 174–175.

[9] Y. Ando and T. Itoh, "*Calculation of transmission tunneling current across arbitrary potential barriers,*" J. Appl. Phys., vol. 61, no. 4, p. 1497, 1987

[10] K. F. Schuegraf, C. C. King, and C. Hu, *"Ultra-thin silicon dioxide leakage current and scaling limit,"* Symposium on VLSI Technology Digest of Technical Papers, pp. 18-19, 1992.
[11] K. F. Schuegraf and C. Hu, "*Hole injection SiO2 breakdown model for very low voltage lifetime extrapolation,"* IEEE Transactions on Electron Devices, vol. 41, no. 5, May 1994.
[12] W. -C. Lee and C. Hu, *"Modeling gate and substrate currents due to conduction- and valence-band electron and hole tunneling,"* Symposium on VLSI Technology Digest of Technical Papers, pp. 198, 2000.
[13] W. -C. Lee and C. Hu, *"Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," I*EEE Transactions on Electron Devices, vol. 48, no. 7, Jul. 2001.
[14] Xin (Ben) Gu, Ten-Lon Chen, Gennady Gildenblat,, Glenn O. Workman, Surya Veeraraghavan, Shye Shapira, and Kevin Stiles, *"A Surface Potential-Based Compact Model of n-MOSFET Gate-Tunneling Current,"* IEEE Transactions on Electron Devices, vol. 51, no. 1, January 2004
[15] Chang-Hoon Choi, P. R. Chidambaram, Rajesh Khamankar, Charles F. Machala, Zhiping Yu, and Robert W. Dutton, *"Dopant Profile and Gate Geometric Effects on Polysilicon Gate Depletion in Scaled MOS,"*IEEE Transactions on Electron Devices, vol. 49, no. 7, July 2002[2]
[16] H. J. Wen, R. Ludeke, D. M. Newns, and S. H. Lo, J. Vac. Sci. Technol. A 15(3), May/Jun 1997.
[17] L. E. Calvet, R. G. Wheeler, and M. A. Reed, Applied Physics Letters, vol 80, No 10, March 2002.
[18] S. M. Sze, *"Metal-Semiconductor Contacts", in Physics of Semiconductor Devices, (*Publishers: J Wiley & Sons, Singapore), 2nd Edition 1981, pp 250 – 254
[19] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, *"Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors,"* in Tech. Dig. VLSI Sym., 2000, pp. 174–175
[20] Fabien Pr_egaldiny , Christophe Lallement, Daniel Mathiot," *Accounting for quantum mechanical effects from accumulation to inversion, in a fully analytical surface potential-based MOSFET model,"* Solid-State Electronics 48 (2004) 781–787
[21] Taur, Y., and Ning, T.H, (Cambridge University Press, New York, 1998
[22] Santaurus Process and Device Simulator

Ashwani K. Rana was born in Kangra, H.P., India in 1974. He received his B.Tech degree in Electronics and Communication Engineering NIT , Hamirpur, India in 1998 M.Tech degree in VLSI Technology from Indian Institute of Technology, Roorkee, India in 2006. He is currently pursuing the Ph.D degree in nano devices from National Institute of Technology, Hamirpur, India.

Presently he is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India, as an Assistant Professor.

His research interest include modeling of semiconductor devices, low power high performance VLSI circuit design and emerging integrated circuit technologies. He has more than 10 publications in International/National Journal & conferences and guided more than 10 M.Tech students in these areas. He is member of ISTE.

Dr. Narottam Chand received his PhD degree from IIT Roorkee in Computer Science and Engineering. Previously he received MTech and BTech degrees in Computer Science and Engineering from IIT Delhi and NIT Hamirpur respectively.

Presently he is working as Head, Department of Computer Science and Engineering, NIT Hamirpur. He also served as Head, Institute Computer Centre, NIT Hamirpur from February 2008 to July 2009. He has coordinated different key assignments at NIT Hamirpur like Campus Wide Networking, Institute Web Site, Institute Office Automation.

His current research areas of interest include mobile computing, mobile ad hoc networks and wireless sensor networks. He has published more than 50 research papers in International/National journals & conferences and guiding six PhDs in these areas. He is member of ISTE, CSI, International Association of Engineers and Internet Society.

Dr. Vinod Kapoor was born at Mandi town in Himachal Pradesh, India. He received his BE Degree in Electronics & Communication Engineering from National Institute of Technology (formerly Regional Engineering College), Durgapur, Bengal, in the year 1987 and Masters Degree Electronics & Control from Birla Institute of Technology & Science, Pilani (Rajasthan) in the year 1996. He did his Ph. D. from Kurukshetra University, Kurukshetra in the field of Optical Fiber Communication in Sept.2006.He also obtained his MBA degree with specialization in Human Resources Management in the year 2002.

He is presently Professor in the Department of Electronics & Communication Engineering NIT Hamirpur, India. He has coordinated different key assignments at NIT Hamirpur like Training & Placement Officer, Chief Warden (Hostels), organizing short term courses.

His research interest includes optical fiber communication and optoelectronics/nano devices. He has published more than 15 research papers in International/National journal & conferences and guiding four Ph.Ds in these areas. He is member of ISTE, IETE and IE.