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Design of OTA with Common Drain and Folded Cascade Used in ADC

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***Abstract*—**In this report, an OTA which is used in fully differential pipelined ADC was described. Using gain-boost architecture with difference-ended amplifier, this OTA achieve high-gain and high-speed. Besides, the CMFB circuit is also used, and some methods are concerned to improve the performance. Then, by optimization the layout design, OTA's mismatch was reduced. This design was using TSMC 0.18um CMOS process and simulation both schematic and layout in Cadence. The result of the simulation shows that the OTA has a gain up to 80dB,a unity gain bandwidth of about 1.437GHz for a 2pF load, a slew rate is about 428V/μs, a output swing is 0.2V~1.35V, with the power supply of 1.8V, the power consumption is 88mW. This amplifier was used in a 10bit 150MHz pipelined ADC.

***Keywords*—**OTA, common drain, CMFB, pipelined ADC

I. Introduction

AS the continuous development of modern electronic technical, the base-band frequency and the bandwidth of modern communication system are much bigger than it is used before. These changes cause that requirements of designing the analog-digital convert which is the bridge between the analog part and the digital part of the communication system is much stricter than before. To meet the requirement of both high-accuracy and high-speed, Op-amp, the core part of the ADC, must be designed with high-gain, high-bandwidth and short settle-time at the same time [1]. This is a challenge in today's circuit design.

In order to design Op-amp with high-bandwidth and high-gain, in 1990, Bult, K. successfully design an architecture named gain-boost architecture which can easily improve the gain without harm the bandwidth. By using this architecture, it is easy to design op-amp which can meet the requirement of gain, therefore, the difficult of designing op-amp move to how to improve the bandwidth and settle-time [2].

In this paper, an op-amp based on gain-boost architecture which is designed to be used in a 10 bit 150Msps pipelined ADC is presented. The op-amp has the gain of 80dB, the bandwidth of 1.437GHz and the settle-time of 2ns. All the circuit and layout are designed and simulated under Cadence environment with TSMC 0.18um CMOS technique for mix signal circuit design.

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II. Circuit Design

To achieve the requirements of gain, the op-amp is designed with the gain-boost architecture. A Folded-Cascode amplifier with gain-boost architecture using by this design is presented in Fig. 1. M5 M6 are using for input; M0 is using for current source under input; M1 M2 M3 M4 M11 M12 for the current source; M13 M14 are using for the common-gate circuit; M7, M8, M9, M10 for the cascode current source which is using as a load. Vbn1 Vbp1 Vbp2 is provided by bias circuit, Vbfb is provided by the switched-capacitor common-mode feedback, Vb13 , Vb14, Vb7, Vb8 are connected with the gain-boost amplifier. Because NMOS has higher capacity of carrier mobility, using NMOS as input could improve gain and bandwidth of the op-amp [3].

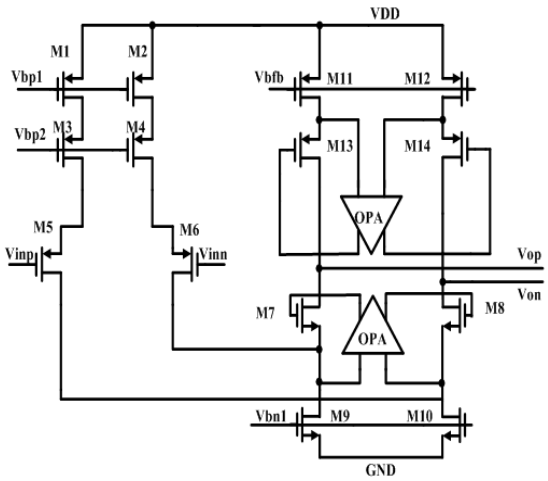

Fig. 1 The main form of the amplifier

While there is no gain-boost using in this structure, the main amplifier has a voltage gain shown in (1) [4].

$$|A_{v1}| = g_m R_{out} = g_{m5,6}\{R_{up} \parallel R_{bottom}\} \quad (1)$$

Here the equivalent resistances of R_{up} and R_{bottom} are calculated below in (2) and (3).

$$R_{up} = \left(g_{m13,14} + g_{mb13,14}\right) R_{o13,14} R_{o11,12} \quad (2)$$

$$R_{bottom} = \left(g_{m7,8} + g_{mb7,8}\right) R_{o7,8} (R_{o9,10} \parallel R_{o5,6}) \quad (3)$$

Assuming that all of the trans-conductance and output resistance are equal, then $A_v = (g_m R_{out})^2$, it can be seen that compare with amplifier with basic current source as a load, the

output resistance was increases about $g_m R_{out}$ times, so the structure of cascode op-amp can provide high gain.

As we discussed in the beginning, design a op-amp with high-gain is just one part of the requirement, we must make sure that the bandwidth and the phase of the amplifier was not harmed by the gain-boost architecture. In order to reduce the harm the gain-boost architecture take to the circuit, first of all, we measure the total capacitance at the gate of the M7, M8, M13 and M14 which equal to Cgs add to Cds, these capacitors are the load capacitance of the gain-boost amplifier. Secondary, designing the gain-boost amplifier that GBW equal to the GBW of the main amplifier. Thirdly, in order to push the second pole of the gain-boost amplifier to a frequency greater than 5 times of the main-amplifier's GBW, the phase margin of the gain-boost amplifier should be more than 80° [5].

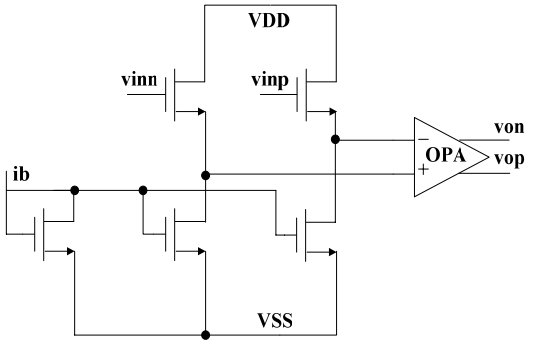

Fig. 2 The whole structure of the folded cascade OTA

The structure of the folded cascade OTA is indicated In Fig. 2. By using the cascade stage and common-drain stage, the driving ability is better than before and the bandwidth has been broadened while the dominant will not be influenced. But the common-mode level of the input has a necessary to be greater than 1.5v as a tradeoff to achieve the benefit above.

In Fig. 3, the PMOS gain-boost amplifier and its CMFB circuit using in this paper is presented. Using differential amplifier and this kind of CMFB circuit have many advantages. First of all, it is easy to achieve the requirements for the gain-boost amplifier. By using fold-cascode structure, this difference-ended amplifier can easily achieve a gain of 40dB with small channel length. Secondary, compare with using single-ended amplifier, the size of the differential amplifier is small than former. Thirdly, the output range of the gain-boost amplifier is smaller than the main amplifier, so using the differential input continuous time CMFB circuit can have both shorter settle time and smaller jitter in output common-mode voltage comparing with CMFB circuit. At the same time, using differential input continuous time CMFB circuit need smaller die size and power consumption than CMFB circuit using resistor for sampling.

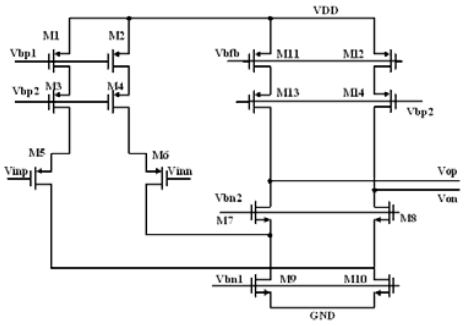

Fig. 3 The PMOS gain-boost amplifier

Beside those two parts, another part of circuit which must be seriously considered during circuit design is the SC CMFB circuit using both in main amplifier and the gain-boost amplifier. The folded cascode amplifier needed a extremely precise bias voltage to make sure that the output common-mode are stabilized at a suitable value, thus, it is necessary to introduce a common mode feedback circuit in order to make the output common-mode of the entire circuit meet the requirement. Common-mode feedback circuit is divided into continuous-time common-mode feedback and switched-capacitor common-mode feedback. Since the switched-capacitor common-mode feedback has no static power consumption, and has a smaller influence on amplifier, therefore in this design, a switched-capacitor common-mode feedback circuit is introduced for CMFB circuit [6]. Fig. 4 shows the schematic of a CMFB circuit. out + and out- are the differential output voltage signal, clock1 and clock2 are two non-overlap clock signal, Vcm is the reference voltage for the output common-mode voltage. Vb provide by bias circuit and Vbfb are output of the CMFB circuit which is using to stabilize the output common-mode voltage.

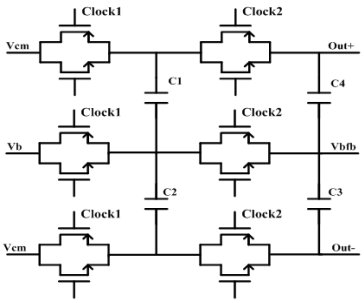

Fig. 4 common-mode feedback with switched-capacitor

III. Layout Design

The whole circuit includes a main amplifier, two gain boost amplifiers, three common-mode feedback, bias circuit of the main amplifier and two gain-boost amplifiers. The layout problem while designing the layout is to maintain the performance which will harm by the non-ideal characters. To achieve this goal, two gain boost amplifiers are located near its input and output point in the main amplifier in order to make wine between them are short. The two gain-boost amplifiers are put aside on the main amplifier respectively, so that the whole layout is symmetric. The switched-capacitor common-mode feedback is placed at the left of the main amplifier so that to

make the connection wine between Out+, Out-, vb1 of the CMFB circuit and the main amplifier shortest. Main amplifier use the matching form of ABBA, the use of dual power supply guarantee the differential-mode signals have a better match, and the bias circuit of the main amplifier is put on the bottom of the main amplifier CMFB, so that the shape of the layout is more order and the area is smaller. The whole layout is shown in Fig. 5.

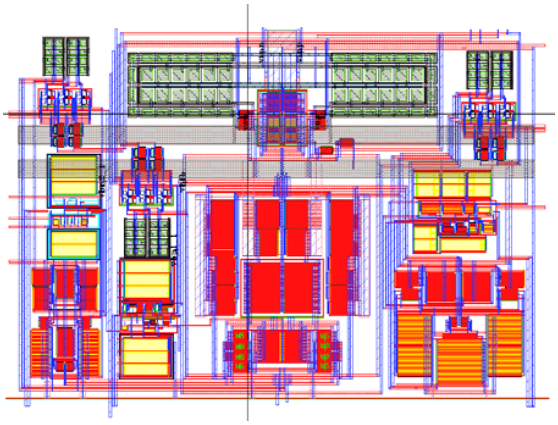

Fig. 5 The whole Layout

IV. Circuit Simulation Results

The whole amplifier was design under TSMC 0.18 CMOS mix-signal process, and simulate using Specture under Cadence. Supply voltage is 1.8V, load capacitor is 2pF.

AC simulation result shows that DC-gain is 80 dB, unity gain bandwidth is 1.437GHz, Phase Margin is 62 °, AC simulation result was shown in Fig. 6.

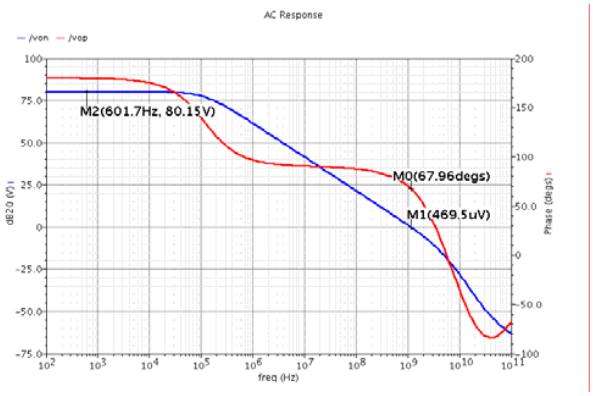

Fig. 6 AC response

V. Conclusion

In this paper, a folded cascade amplifier with gain boost structure is described. Instead of using single-ended amplifier, in this paper, a fully differential amplifier is used. Besides, a SC CMFB circuit is used to reduce the jitter of the common-mode voltage. The result of schematic simulation is setting out below: gain up to 80dB, unity gain bandwidth of about 1.437GHz for a 2pF load, a slew rate is about +428V/μs, output swing is 0.2~1.35V, with the power supply of 1.8V, the power consumption is 88mW. The main characteristics of the amplifier are shown in Table 1.This amplifier was used in a 10bit 150MHz pipelined ADC with under-sampling technical.

TABLE I
Main Characteristics of the Op-amp

Op-amp specification	Simulation
DC Gain	>80dB
Phase Margin	62.3
Unity Gain Frequency	1.437GHz
Output Swing	0.2V~1.35V
Slew rate	428V/μs
Supply Voltage	1.8V
Power Consumption	88mW
Load Cap	2pF

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