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Doping Profile Measurement and Characterization by Scanning Capacitance Microscope for Pocket Implanted Nano Scale n-MOSFET

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Abstract—This paper presents the doping profile measurement and characterization technique for the pocket implanted nano scale n-MOSFET. Scanning capacitance microscopy and atomic force microscopy have been used to image the extent of lateral dopant diffusion in MOS structures. The data are capacitance vs. voltage measurements made on a nano scale device. The technique is non-destructive when imaging uncleaved samples. Experimental data from the published literature are presented here on actual, cleaved device structures which clearly indicate the two-dimensional dopant profile in terms of a spatially varying modulated capacitance signal. First-order deconvolution indicates the technique has much promise for the quantitative characterization of lateral dopant profiles. The pocket profile is modeled assuming the linear pocket profiles at the source and drain edges. From the model, the effective doping concentration is found to use in modeling and simulation results of the various parameters of the pocket implanted nano scale n-MOSFET. The potential of the technique to characterize important device related phenomena on a local scale is also discussed.

Keywords—Linear Pocket Profile, Pocket Implanted n-MOSFET, Scanning Capacitance Microscope, Atomic Force Microscope.

I. Introduction

AS MOSFETs are scaled down in to the nano scale regime, the two-dimensional (2-D) distribution of dopants becomes a very important factor affecting their performance. For example, the revers short channel effect (RSCE) [1], believed to be caused by the enhanced diffusion of dopants near the source/drain junction regions [1]-[3], is a 2-D problem that directly affects device characteristics. Moreover, recent development of devices having lateral doping features in the channel and source/drain regions, such as, pockets or halos [4],[5] also require an understanding of how dopants diffuse in 2-D during the fabrication process. A technique that allows one to obtain the 2-D doping profile of advanced MOS devices is therefore essential. Applications include process calibration, process monitoring, process troubleshooting as well as device design and optimization. Characterization is a follow-on activity to model development and implementation. Similarly, design verification is a follow-on activity to the design process and can be viewed as validating models developed and implemented during an earlier design phase. A number of techniques that determine one-dimensional (1-D) doping profiles have been developed and are widely used. Among these are the various capacitance-voltage (C-V) methods [6] and secondary ion mass spectroscopy (SIMS) [7]. But SIMS is destructive and time consuming. Indirect techniques include inverse modeling where a doping profile is found in such a way that its electrical behaviour obtained through numerical simulations, matches with experimental data [8]-[10]. The use of C-V data to extract 2-D doping profiles has been reported [8],[9]. But due to the extremely small dimensions and capacitance of modern submicron devices, special test structures are needed. Noise and parasitic capacitance also become important issues. However, scanning capacitance microscopy (SCM) is a direct technique that can determine the 2-D doping profiles combined with atomic force microscopy (AFM). This is one of the most powerful methods for the characterization of semiconductor devices due to its non-destructive technique and high spatial resolution. Channel length of 0.15 micron MOSFETs were determined directly for the first time using SCM [11]. Present-day VLSI device technology demands accurate knowledge of the spatial extent in three dimensions (3-D) of active impurity dopants which have been incorporated into the discrete device elements. The active region of a MOSFET device is engineered by incorporating dopants, such as, As, B, or P, in a concentration range of 10^{15} to 10^{20} cm^{-3}. In the (2-D) junction regions of a submicron MOSFET device, it is necessary to quantify the variation (or "profile") of these impurity dopants to resolution of 100 nm or less over four orders of magnitude in concentration. Achieving such high precision in the characterization of dopant profiles is a nontrivial task in both the design and manufacturing phases.

Thus, it is desirable to have a method capable of measuring dopant profiles in 2-D (or even 3-D) in a straightforward, reliable, and repeatable (nondestructive) fashion. Lateral dopant profiles have been inferred from device capacitance measurements and simulation [12], or from junction-staining [13]. A "tomographic" technique based on a matrix of SlMS measurements has been explored [14]. In this paper, we have presented a technique using scanning capacitance microscopy (SCM) and its cousin, atomic force microscopy (AFM), which satisfies many of the desired criteria for 2-D and in some

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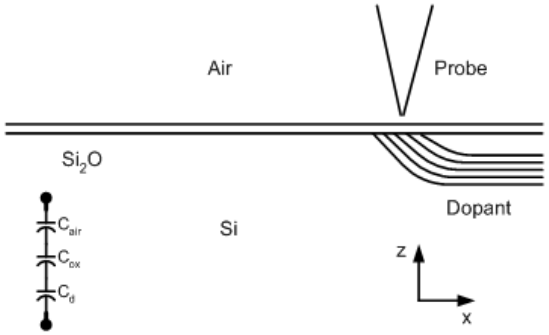

Fig. 1. Illustration of the basic concept of scanning capacitance microscopy

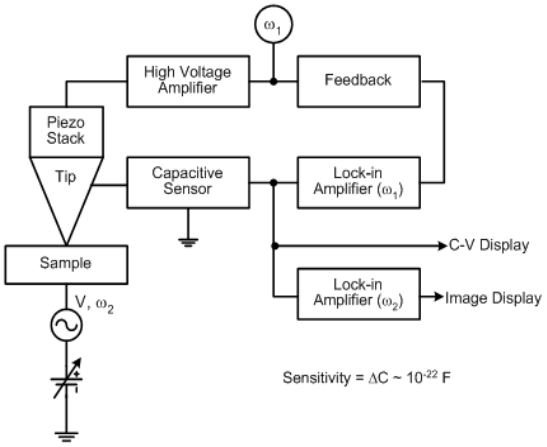

Fig. 2. Block diagram of the SCM apparatus with sample at bias voltage, V and with ac signal source having frequency, ω_2

sense 3-D dopant imaging [15], [16]. It is noted that other workers have used scanning tunnelling microscopy (STM) for potentiometry on p-n junctions [17], [18].

II. Scanning Capacitance Microscopy

Scanning capacitance microscopy (SCM) has been commonly used to image dopant gradients in silicon and other semiconductors. As a mobile, high-resolution (to 2 nm) metal-oxide-semiconductor (MOS) probe, SCM also is a non-destructive, contact less tool with which to examine local variations in dielectric thin film quality and local variations in semiconductor substrate properties. Virtually any measurement that can be made with fabricated metal electrodes can also be made with SCM. We describe here mainly the SCM; the AFM implementation is discussed briefly. As depicted in Fig. 1, a small metallic probe, with a radius of curvature at its tip of typically 50 nm, is scanned over a nonuniformly doped sample. A bias voltage (dc or ac) is placed on the tip, and the local capacitance, C, or its derivative, $\partial C/\partial V$, are then measured as a function of lateral position (x). The measured capacitance or capacitive gradient, as a function of bias voltage, provides a direct measurement of the activated dopant density with high spatial resolution. The inset to Fig. 1 represents the simplest equivalent circuit model for the SCM-semiconductor system. This is a series capacitance stack wherein the dopant affects the detected capacitance by virtue of dictating what the local depletion capacitance, C_d, is at lateral scan position, x. C_{air} and C_{ox}, are the capacitances due to the air gap and oxide film respectively.

Figure 2 is a high level block diagram of the SCM. The central feature of the detection system is the capacitance sensor [19]. This sensor is basically a microwave inductance strip in a resonant circuit. It can measure capacitance variations between the tip and the sample of the order of 10^{-22} F/Hz$^{1/2}$. The tip scan is controlled by a feedback loop which maintains the capacitive signal constant. The piezo-scanners have a 6 mm lateral and 3 mm vertical range. To avoid low-frequency drifts caused by stray capacitances, a vertical dither is placed on the tip/sample spacing typically at 30 KHz. This also provides a means to measure the capacitive gradient.

The ac signal is filtered and rectified by the lock-in amplifier with frequency, ω_1 as shown in Fig. 2. The lock-in amplifier's output is sent to an integrating feedback loop to maintain the constant ac signal by adjusting the average tip height above the sample. Such a system has achieved 25 nm resolution in topographic mode [20].

In the AFM implementation [16], a laser heterodyne detection system is used to measure excursions of a cantilever-style tip which is mechanically oscillated near its resonance. These deviations are directly proportional to tip-to-sample forces, including the Coulomb force due to mutual capacitance. A signal generator provides an ac and/or dc signal between tip and sample at the desired frequency, ω_2. Thus, a C-V curve can be taken at any given lateral position, or $\partial C/\partial V$ curves at constant dc bias can be acquired as the tip is scanned. Both the tip scan and data acquisition are controlled by a laboratory computer. In either SCM or AFM mode, a separate laser (633 nm) is used as an optical carrier pump to obtain transport data.

III. Experimental Procedure

A. Sample Preparation

Measurements have been made on a variety of VLSI structures: diffusion gratings, submicron MOSFET structures, and even DRAM devices. In this work, we describe data taken on uncleaved gratings and on cleaved MOSFETs. The gratings were prepared to emulate typical MOSFET source/drain diffusion pockets. P-type silicon substrates were thermally oxidized to grow 24 nm of SiO_2. The wafers were masked with 500-nm photoresist with an 8 μm period. A 50 KeV BF_2 implant at 10^{15} cm^{-3} dose was performed, producing a peak concentration of roughly 10^{20} cm^{-3} near the surface of the unmasked regions. The photoresist was stripped, leaving a topographically flat, nonuniformly implanted silicon surface. A 900^0C, 10 min anneal was performed to activate (and diffuse) the dopant. The 8 μm period was chosen in this case to minimize the effects of possibly large lateral depletion at some tip biases. Small area sections containing the gratings (typically a few square mm) were cut from the wafer and mounted on the SCM stage with the sectioned wafer surface up. The MOSFET samples were actual production devices from IBM's 1 Mb DRAM. A small section of the wafer was

cleaved to expose a MOSFET cross section. The section was mounted with the cleaved face up on the stage.

B. Measurement

For both the grating and the MOSFET samples, measurements were made in ambient air. An atomic force microscope is used to position a nanometer scale tip on the silicon surface, and the local capacitance change is measured as a function of the applied voltage V. We used a commercial SCM of Digital Instruments (Dimension 3100), which is a contact-mode atomic force microscope (AFM) with a 915 MHz tuned circuit to which it is coupled to the tip-sample capacitance to obtain the images [21]. SCM measurement is done in constant voltage change (constant dV) mode by applying a 100 KHz AC voltage of about 1 V to the sample. The system is configured to measure $\partial C/\partial V$, which depends on the variation of silicon capacitance (C_{Si}) due to dopant distribution. In general, when the probe of a conductive scanning probe microscope (SPM) contacts a silicon surface through an insulating layer, a flat-band offset occurs because of the movement of carriers from the insulating layer to the conductive SPM probe. Because of this flat-band offset, the magnitude of the SCM signal in the vicinity of the p-n junction does not reflect the carrier density [22]. The flat-band offset can be compensated for by applying a DC offset voltage to the sample. In principle, by applying a DC offset voltage, the change in capacitance due to the accumulation and depletion caused by the applied AC voltages can be maximized. However, the magnitude of the SCM signal varies in proportion to this change. Therefore, in this work, the level of the applied DC voltage is set according to the magnitude of the SCM signal. The SCM instrument can acquire SCM images in the amplitude mode and the phase mode, which reveals whether the carriers are n-type or p-type. The lock-in amplifier used to measure the SCM output operates at the same frequency as the frequency of the applied AC voltage. In the phase mode, the phase of the lock-in has to be designated. When the correct phase is selected, whenever, there is a change of carrier type, the lock-in amplifier output changes polarity. In the experiment, the phase is adjusted to around 900 to obtain the best contrast in the SCM images. SIMS measures the impurity distribution to a resolution of a few nm beneath the silicon surface. Our calibration of two-dimensional SCM data is based on the one-dimensional SIMS data. Therefore, to acquire the exact dopant profile in the ultra shallow region, SIMS measurement is carried out at energy below 1 KeV.

IV. Measured Capacitance Data

For the grating structure, Fig. 3 shows data vs. lateral scan position, x, for three typical tip-to-sample dc biases. The line traces clearly indicate the dopant variation in the sample on a scale less than 1 μm. The periodic variation is 8 μm. The signal varies strongly with bias voltage as expected from the simple model based on depletion capacitance in the semiconductor. The largest signal is apparent in the lightly-doped (p-type) region, due to the fact that depletion capacitance varies more rapidly with bias at lower dopant densities. Note

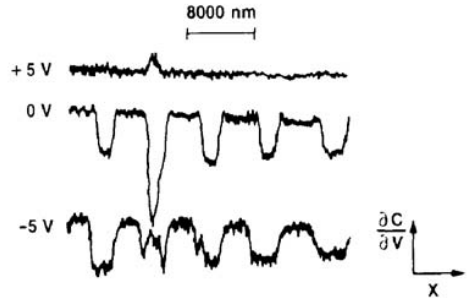

Fig. 3. Three line scans of the grating structure showing the $\partial C/\partial V$ signal at different bias voltages

that there is some defect or nonuniformity in the fourth period of the data which has apparently shifted the depletion voltage. Since the sample surface was measured in topographic mode to be nearly atomically flat, this defect is evidently some fixed charge, perhaps in the oxide.

Figure 4 shows a set of C-V curves taken with the SCM tip held fixed while positioned over several points along the grating structure. When the tip is centered over the relatively low-doped region (position D), the C-V curve looks like a typical high-frequency C-V curve. As the tip is moved closer to the junction near the more highly doped n-type region, the C-V curves are altered from the usual 1-D form. A gradual transition is evident as the junction is approached, due to the mixing of lateral depletion effects in this region of highly inhomogeneous doping. At positions A, B and C, the signature of both p- and n-type dopant are evident (positive and negative C-V slope, respectively). When the tip is well inside the highly-doped n-type region (i.e., to the left of position A), a signal is measured but cannot be displayed on the scale of Fig. 4.

A first-order deconvolution of the $\partial C/\partial V$ vs. x data to obtain crude contours of activated dopant density in 2-D is possible by a simple extension of the standard C-V analysis [23]. One integrates the $\partial C/\partial V$ vs. data (e.g. the data of Fig. 3) to obtain $C(V)$ at x within a constant. A less efficient procedure requires measuring both a $\partial C/\partial V$ vs. x and $C(V)$ vs. x, as in Fig. 4, to avoid the integration procedure. The modified standard model yields an expression for the local

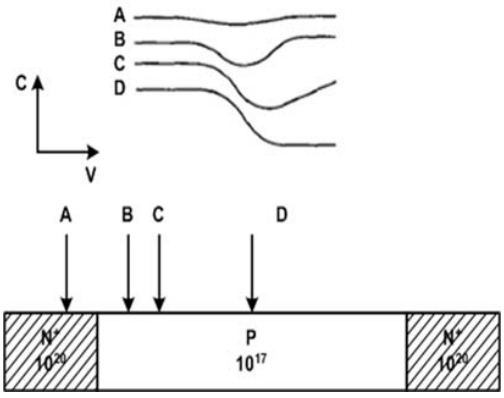

Fig. 4. Local C-V measurements acquired on grating structure with tip stationary at various points

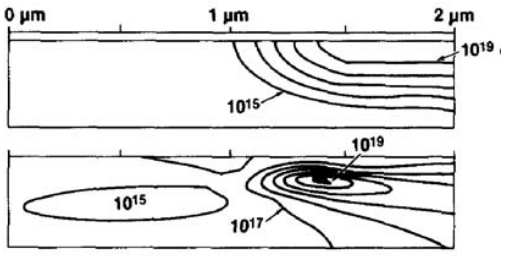

Fig. 5. 2-D dopant profile of grating structure. Upper profile is process simulation and lower profile is deconvolved from SCM data

activated dopant density, $N_{sub}(x,z)$, where z is the vertical dimension (in the bulk).

$$N_{sub}\Big(x,z(x)\Big) = -\frac{q\varepsilon_{Si}}{C^{-3}(a;V)/\partial C/\partial V} \tag{1}$$

,where q is the electronic charge, ε_{Si} is the dielectric coefficient for silicon. It is important to note that z is interpreted as the local depletion depth given by equation 2.

$$z(x) = \varepsilon_{Si}\left(\frac{1}{C(a;V)} - \frac{1}{C_{ox}} - \frac{1}{C_{air}}\right) \tag{2}$$

The parameter a, which appears in $C(a;V)$, is necessary to scale the integrated, measured signal. a is unit less and of the order of unity (0.3 in this case); it is interpreted as dependent on the effective spot size which the tip presents to the sample.

Figure 5 shows the results of such a deconvolution for data taken on the grating structure near one of the junction regions. The contours of dopant density in the upper plot are the result of a process simulation of the steps required to create the sample structure. The contours in the lower plot are the deconvolution of data such as shown in Fig. 3. The agreement is admittedly gross, but is encouraging since it indicates that the data have some quantitative value. Much of the error in the deconvolution is attributed to the neglect of junction capacitance and to the assumption of a homogeneous depletion front near the tip.

V. Pocket Doping Profile

The pocket implanted n-MOSFET structure shown in Fig. 6 is considered in this work and assumed co-ordinate system is shown at the right side of the structure. Localized extra dopings are shown by circles near the source and drain side regions. All the device dimensions are measured from the oxide-silicon interface. In the structure, the junction depth (r_j) is 25 nm. The oxide thickness (t_{ox}) is 2.5 nm, and it is SiO_2 with fixed oxide charge density of 10^{11} cm^{-2}. Uniformly doped p-type Si substrate is used with doping concentration (N_{sub}) of 4.2×10^{17} cm^{-3} with pocket implantation both at the source and drain side with peak pocket doping concentration of 1.75×10^{18} cm^{-3} and pocket lengths from 20 to 30 nm, and source or drain doping concentration of 9.0×10^{20} cm^{-3}.

The pocket implantation, which causes the Reverse Short Channel Effect (RSCE), is done by adding impurity atoms

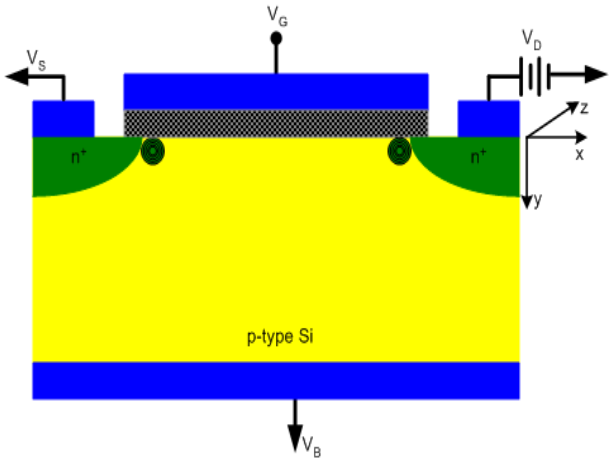

Fig. 6. Pocket implanted n-MOSFET structure

both from the source and drain edges. It is assumed that the peak pocket doping concentration (N_{pm}) gradually decreases linearly towards the substrate level concentration (N_{sub}) with a pocket length (L_p) from both the source and drain edges.

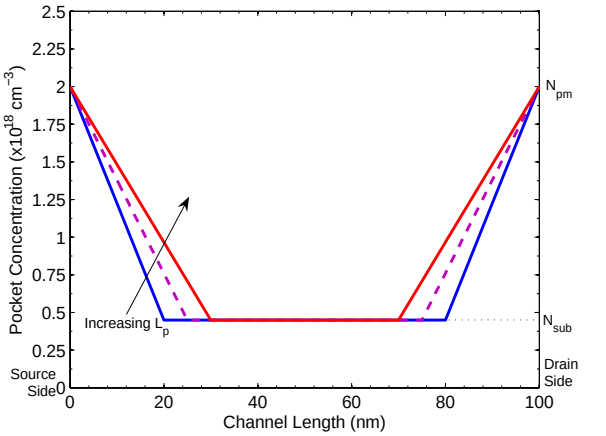

Fig. 7. Simulated pocket profiles at the surface for different pocket lengths, L_p = 20, 25 and 30 nm; peak pocket concentration, N_{pm} = 2.0×10^{18} cm^{-3}

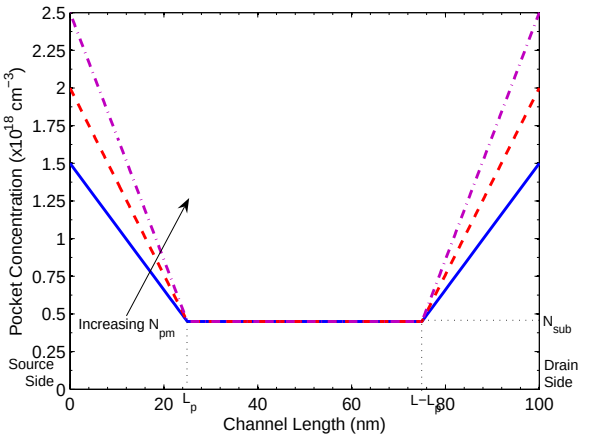

Fig. 8. Simulated pocket profiles at the surface for various peak pocket concentrations, N_{pm} = 1.5×10^{18}, 2.0×10^{18}, 2.5×10^{18} cm^{-3}; pocket length, L_p = 25 nm

The basis of the model of the pocket is to assume two laterally linear doping profiles from both the source and drain edges across the channel as shown in Figs. 7-8 for substrate concentration of 4.2×10^{17} cm^{-3} and channel length of 100 nm. The pocket parameters, N_{pm} and L_p, play important role in determining the RSCE. At the source side, the pocket profile is given as

$$N_s(x) = -\frac{N_{pm} - N_{sub}}{L_p}x + N_{pm}$$

$$N_s(x) = N_{sub}\frac{x}{L_p} + N_{pm}\left(1 - \frac{1}{L_p}x\right) \quad (3)$$

At the drain side, the pocket profile is given as

$$N_d(x) = \frac{N_{pm} - N_{sub}}{L_p}\left[x - (L - L_p)\right] + N_{sub}$$

$$N_d(x) = N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p}\right) + N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p}x\right) \quad (4)$$

,where x represents the distance across the channel. Since these pile-up profiles are due to the direct pocket implantation at the source and drain sides, the pocket profiles are assumed symmetric at both sides.

With these two conceptual pocket profiles of equations (3) and (4), the profiles are integrated mathematically along the channel length from the source side to the drain side and then the integration result is divided by the channel length (L) to derive an average effective doping concentration (N_{eff}) as shown in equation (5).

$$N_{eff} = \frac{1}{L}\int_0^L \Big[N_s(x) + N_d(x) + N_{sub}\Big]\mathrm{d}x \quad (5)$$

Putting the expressions of $N_s(x)$ and $N_d(x)$ from equations (3) and (4) in equation (5) the effective doping concentration is obtained in equation (6).

$$N_{eff} = N_{sub}\left(1 - \frac{L_p}{L}\right) + \frac{N_{pm}L_p}{L} \quad (6)$$

This effective doping concentration expression is then used in deriving the surface potential model by applying Gauss's law [25]. This surface potential model is used to find the inversion layer charges and other parameters for determining the effective inversion layer mobility. When $L_p \ll L$ for long channel device then the pocket profile has very little effect on uniform substrate concentration at the surface, but when L_p is comparable with L then the pocket profile parameters affects the substrate doping concentration at the surface of the n-MOSFET. This causes the surface potential, threshold voltage and hence effective mobility and subthreshold drain current along with other parameters of pocket implanted n-MOFET to change due to RSCE.

Because of the pocket implantation, effective doping concentration increases with decreasing channel lengths as observed in Fig. 9. This becomes stronger when both peak pocket concentration and/or pocket length increases.

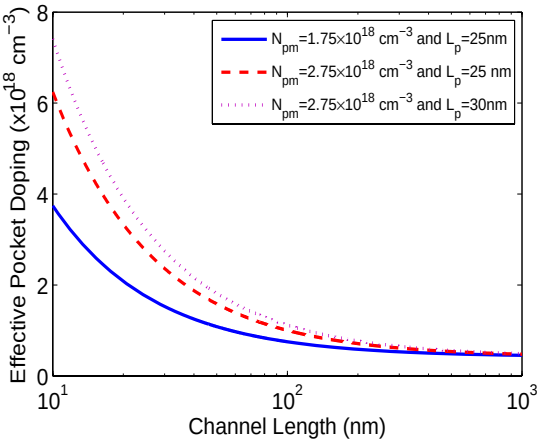

Fig. 9. Simulated effective pocket doping concentration vs. channel lengths at the surface for different peak pocket concentration and pocket lengths with substrate concentration, $N_{sub} = 4.5\times10^{17}$ cm^{-3}

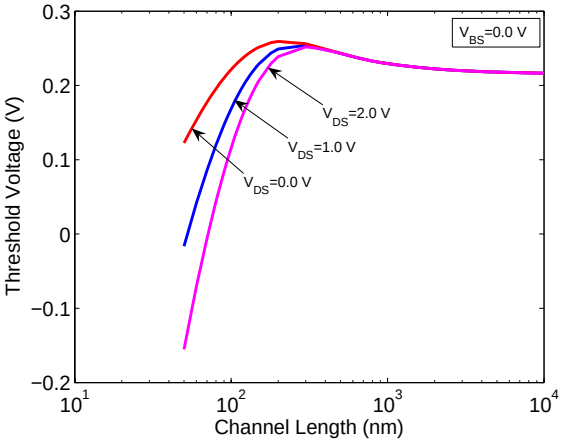

Fig. 10. Threshold voltage vs. channel length curves along the channel for various drain bias, $V_{DS} = 0.0$ V with $V_{BS} = 0.0$ V

VI. Simulated Results and Discussions

In order to verify the proposed linear pocket profile model, various operational parameters, such as, threshold voltage, surface potential, mobility, drain current etc. have been simulated using this pocket profile model. Few simulation results are shown in this section. Fig. 10 shows the threshold voltage variation as a function of channel length for different drain bias voltages. As the channel length goes down for particular drain bias, threshold voltage increases first and then with further decrement of channel length threshold voltage reduces, i.e. it shows both RSCE and SCE. But as the drain bias increases, both RSCE and SCE occur at longer channel length due to the drain induced barrier lowering (DIBL). As channel length becomes shorter DIBL effect is more pronounced, electric field is very high and it lowers the potential barrier that separates it from the adjacent diffused junction [24].

Figure 11 shows the variation of surface potential along the channel for different drain biases. It has been observed that as the drain bias increases surface potential increases at the drain

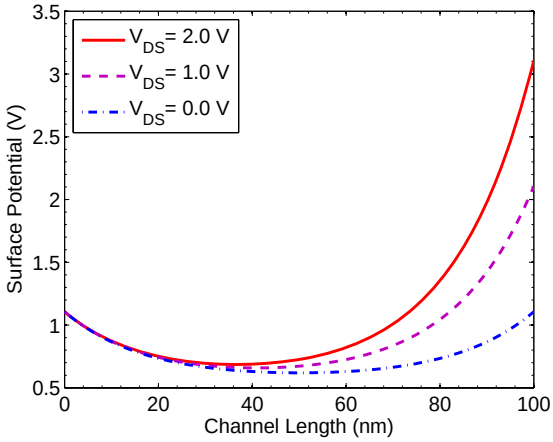

Fig. 11. Surface potential vs. channel length for various drain biases with channel length, L = 100 nm and substrate bias, $V_{BS} = 0.0 = 0.0$ V

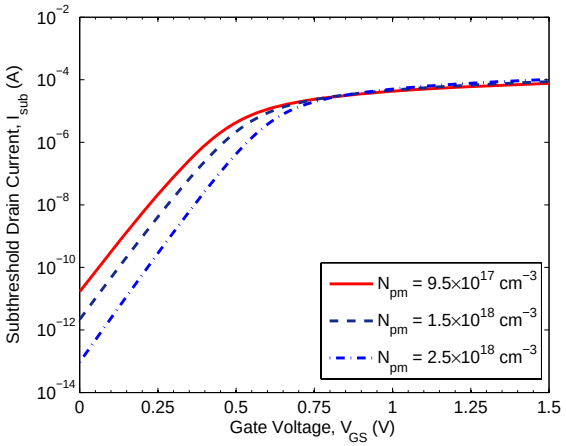

Fig. 13. Subthreshold drain current versus gate voltage for for different peak pocket implant concentrations with drain bias, $V_{DS} = 0.05$ V, substrate concentration, $N_{sub} = 4.5\times10^{17}$ cm^{-3}, pocket length, $L_p = 25$ nm and channel length, $L = 100$ nm

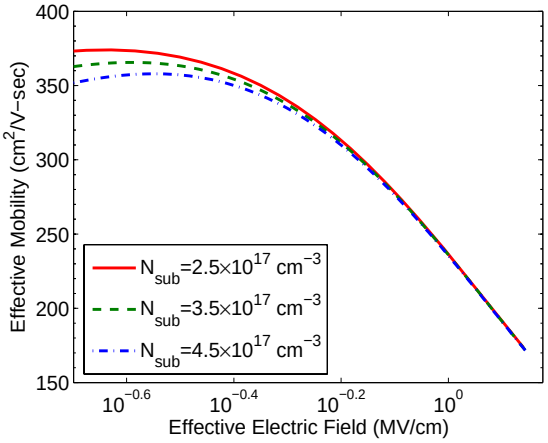

Fig. 12. Effective mobility vs. effective electric field for different substrate concentrations (N_{sub}) with L = 0.1 μm, $N_{pm} = 1.75\times10^{18}$ cm^{-3}, L_p = 25 nm, $V_{DS} = 0.05$ V, T = 300 K

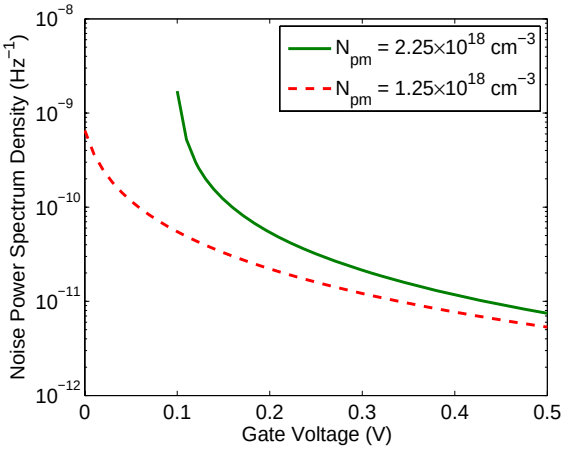

Fig. 14. Noise power spectrum density vs. gate voltage for two pocket doses with $L = 50$ nm, $L_p = 25$ nm, $V_{DS} = 0.2$ V, $f = 100$ Hz

side whereas it remains constant at the source side. Because, at the drain end carriers are then depleted [25].

Figure 12 shows the variation of effective mobility vs. effective normal electric field for different values of substrate concentration. It has been observed that there is no change in the curve with the change in substrate concentration. This proves the universality of mobility curve [26].

In order for the further verification of the proposed model, subthreshold drain current model is simulated incorporating the proposed effective mobility model. The model is simulated for three different pocket doses as shown in Fig. 13. It is observed that the subthreshold drain current behavior with the gate voltage variation is same as observed in [27]. As the pocket dose is increased the subthreshold drain current is decreased for a particular gate bias due to the This happens due to the additional doping atoms present near the source and drain edges and hence the increase of the Coulomb scattering rate and consequent mobility degradation. Also with the decrement of peak pocket implant concentration, subthreshold slope decreases since RSCE diminishes [27].

Fig. 14 shows the noise power spectrum density variations with the gate length for two different pocket doses at gate and drain bias of 0.5 V and 0.2 V respectively. Noise degradation is more significant in shorter channel length device as pocket implant region is comparable with the channel length of the device. For longer channel length, the noise is not changed with the increment of the pocket implantation dose [28].

VII. Conclusion

Lateral dopant profiling has been demonstrated on a 100-nm scale by a straightforward, basically non-destructive technique. With increased sensitivity, imaging on a 10-nm scale is believed feasible. Other important measurements can evidently be made, including trapped-charge, surface-defects, direct measurement of a variety of device-scale capacitances and, perhaps, carrier transport. It is anticipated that, with moderate enhancement, characterization of VLSI devices using SCM or AFM will have much value in future device development and manufacture. Based on the characterized dopant profile,

a linear pocket profile is assumed both at the source and drain sides. Then the simulated pocket profile is presented and simulated threshold voltage, surface potential and subthreshold drain current models developed using the effective pocket doping concentration are presented to show the usefulness of the assumed pocket profiles.

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