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130 nm CMOS Mixer and VCO for 2.4 GHz Low-power Wireless Personal Area Networks

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Abstract—This paper describes a 2.4 GHz passive switch mixer and a $5/2.5$ GHz voltage-controlled negative G_m oscillator (VCO) with an inversion-mode MOS varactor. Both circuits are implemented using a 1P8M 0.13 μm process. The switch mixer has an input referred 1 dB compression point of -3.89 dBm and a conversion gain of -0.96 dB when the local oscillator power is $+2.5$ dBm. The VCO consumes only 1.75 mW, while drawing 1.45 mA from a 1.2 V supply voltage. In order to reduce the passives size, the VCO natural oscillation frequency is 5 GHz. A clocked CMOS divide-by-two circuit is used for frequency division and quadrature phase generation. The VCO has a -109 dBc/Hz phase noise at 1 MHz frequency offset and a 2.35-2.5 GHz tuning range (after the frequency division), thus complying with ZigBee requirements.

Keywords—Switch Mixers, Varactors, IEEE 802.15.4 (ZigBee), Direct Conversion Receiver, Wireless Sensor Networks.

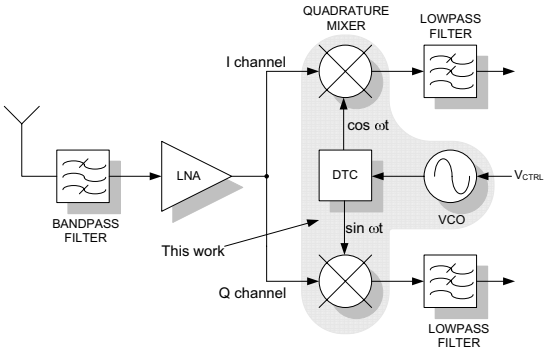

Fig. 1. Direct Down-conversion Front-End.

I. Introduction

THE increasing demand for low-power wireless transceivers operating in the 2.4 GHz ISM (Industry, Scientific, Medical) band, has prompted an extensive research in this area. In such scenario CMOS technology is very appealing for low-cost, low-power solutions targeted to low-rate wireless personal area networks (WPANs) such as ZigBee. Among all the reported receiver architectures, a direct conversion architecture, is particularly appealing for monolithic implementation due to its simplicity [7]. Regardless its simplicity, a direct conversion receiver requires a careful design to counterbalance the effects of DC offsets and flicker noise at low frequencies [3]. In a direct conversion receiver, the incoming signal is shifted to baseband with no intermediate conversion steps like in heterodyne receivers; furthermore, IEEE 802.14.5 standard relies on complex modulation schemes in which data is modulated by a pair of orthogonal signals. This modulation scheme complicates the transceiver since quadrature mixer and VCO are necessary to demodulate both the in-phase and the quadrature component of the incoming signal. Using a passive switch mixer helps reducing implementation complexity; in addition, a passive mixer has a better linearity than its active counterpart and, virtually, no power consumption which makes it very appealing for low-power designs. On the other hand, a quadrature VCO may not be the best solution for a low-cost design such as ZigBee, due to the high area overhead introduced by its passive elements. A more suitable technique consist in generating the target frequency using a VCO that oscillates at the double the target frequency and a frequency divide-by-two circuit (DTC) to generate all the phases necessary for O-QPSK signal demodulation [1]. This approach has two great advantages: (1) the increased frequency allows reducing the value of the inductors of the LC resonator, and, in turn to save area, and (2) the divide-by-two circuit improves by 6 dB the oscillator phase noise [8]. Fig. 1 sketches a simplified block diagram of a typical direct conversion receiver. This work deals with the down-conversion section of the receiver, i.e. mixer and VCO design. The rest of the paper is structured as follows. Section II describes the proposed switch mixer. In a direct conversion receiver flicker noise is a major concern since it is inversely proportional to signal frequency. For this reason, the effect of such kind of noise on the down-converted signal is examined as well. Section III deals with the ZigBee-compliant voltage controlled oscillator, frequency division and phases generations. Finally, in Section IV, the proposed designs are evaluated and discussed and conclusions are given.

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II. Switch Mixer

A mixer translates the incoming RF signal to low intermediate or zero frequency. Passive mixers are very attractive due to their very low power consumption and high linearity [4]. Fig. 2 depicts the proposed passive switch mixer. It consists of a input matching network formed by inductors L_{im}, a bias network formed by resistors R_b, and the switching core formed by transistors M1 to M4. Since both input and output impedances of the NMOS switch are capacitive, the series inductors L_{im} performs the cancellation of the imaginary part, thus improving input matching. The balanced RF signal is applied through inputs $RFinP$ and $RFinN$ to the sources of the NMOS switches, whereas the local oscillator (LO) signals are applied to the gates of the switching devices. All the

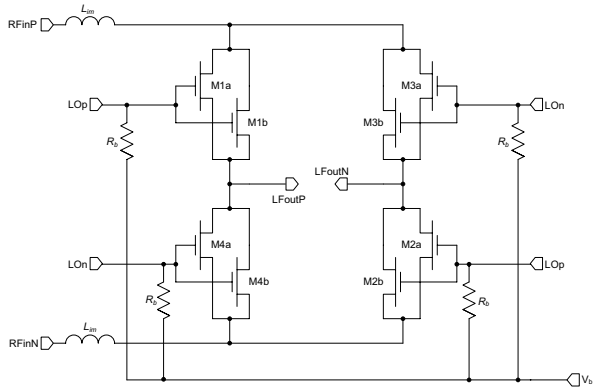

Fig. 2. The Passive Switch Mixer.

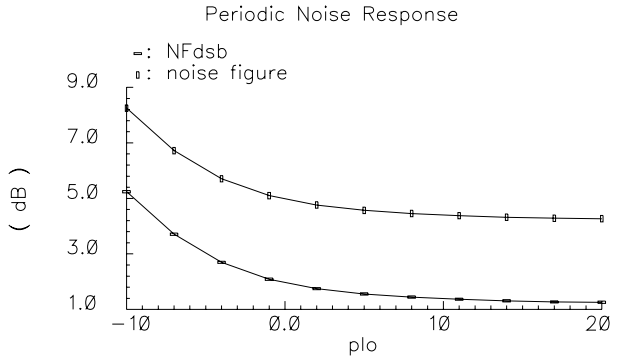

Fig. 3. Simulated Mixer Noise Figure at 10 MHz.

transistors are minimum length and 90 μm wide, matching inductors are $L_{im} = 2.3$ nH, bias resistors are $R_b = 10$ KΩ, whereas bias voltage is $V_b = 0.3$ V. In a NMOS convectional switch, the transistor conducts when its gate-to-source voltage exceeds the threshold voltage V_T, thus the output signal could be decreased by V_T in the case of large RF inputs. The V_T drop problem leads to output signal compression and non-linearities when the RF input is large compared to the LO signal. In the proposed design, switching transistors gates are biased closed to threshold voltage to tackle the V_T drop problem and to improve mixer linearity.

A. Mixer Performance

To evaluate mixer performance four figures of merit are considered: single and double sideband noise figure, voltage conversion gain, port-to-port isolation, and linearity (input referred 1-dB compression point $P1dB$ and third order intermodulation product $IIP3$). Flicker noise might be a major concern in a direct conversion receiver, hence noise performance is evaluated at different frequencies to study en evaluate the effect of flicker noise on the proposed design. Fig. 3 shows the single and double sideband noise figure calculated at a frequency of 10 MHz. At such frequency flicker noise is not present since it is proportional to $\frac{1}{f}$. The single sideband noise figure for a LO power of -1 dBm is approximately 5.3 dB. Furthermore, observe that as expected, there is a 3 dB difference between single and double sideband noise.

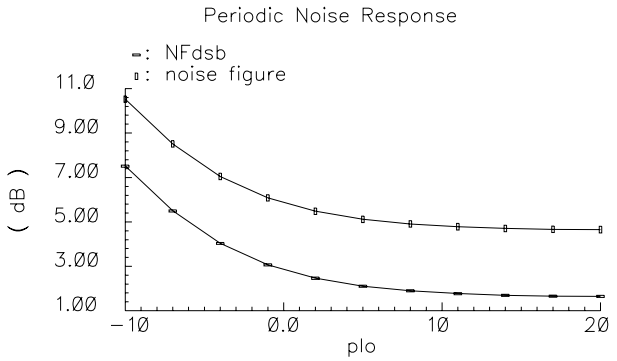

Fig. 4. Simulated Mixer Noise Figure at 1 KHz.

TABLE I
MIXER PORT TO PORT ISOLATION.

Port	Feedthrough Contribution
LO-RF	-72.40 dB
LO-IF	-77.80 dB
RF-LO	-113.84 dB
RF-IF	-72.40 dB

To evaluate the effects of flicker noise, simulation is repeated at a frequency of 1 KHz and the results are shown in Fig. 4 In this case, the single sideband noise figure for a LO power of -1 dBm is approximately 6.2 dB. Consequently, flicker noise contributes to the overall noise figure at low frequencies with 0.9 dB increasing it by approximately 17%. Conversion gain is simulated for different LO powers. Estimations are performed by means of periodic AC and XF analysis in a down-converted band of 10 MHz, and assuming the mixer is loaded by a high-impedance filter with a 1 KΩ input impedance. Fig. 5(a) shows mixer conversion gain in the down-converted band with a LO power of -1 dBm. The estimated conversion gain in this case is -1.23 dB. Fig. 5(b) depicts voltage conversion in the case the local oscillator power is $+2.5$ dBm. Increasing the LO power improves the conversion gain up to -0.96 dBm. Table I summarizes the simulated port-to-port isolation. LO feedthrough to mixer input (RF) and output (IF) ports is considered as well as the feedthrough from input port to LO and IF ports. The LO-RF isolation is of paramount importance since reciprocal mixing at the RF port may produce a large DC-offset. Finally, Fig. 6 shows the simulated 1-dB input-referred compression point when the power of local oscillator is 2.5 dBm. Table II compares the proposed implementation with other similar works. The proposed switch mixer has the best noise figure, conversion gain, port isolation and area overhead. The linearity is also excellent; however, the price to pay for these performances is a high LO power requirement. Decreasing the LO power to -1 dB does not affect significantly the conversion gain that drops to -1.23 dB (as depicted in Fig. 5(a)); the noise figure drop is also of little importance since it worsens by 1 dB. However, the impact on linearity is important since the input-referred 1-dB compression point is below -7 dBm with a LO power of 1 dB. Observe that these comparisons are qualitative and their main goal is only giving the reader a general view of

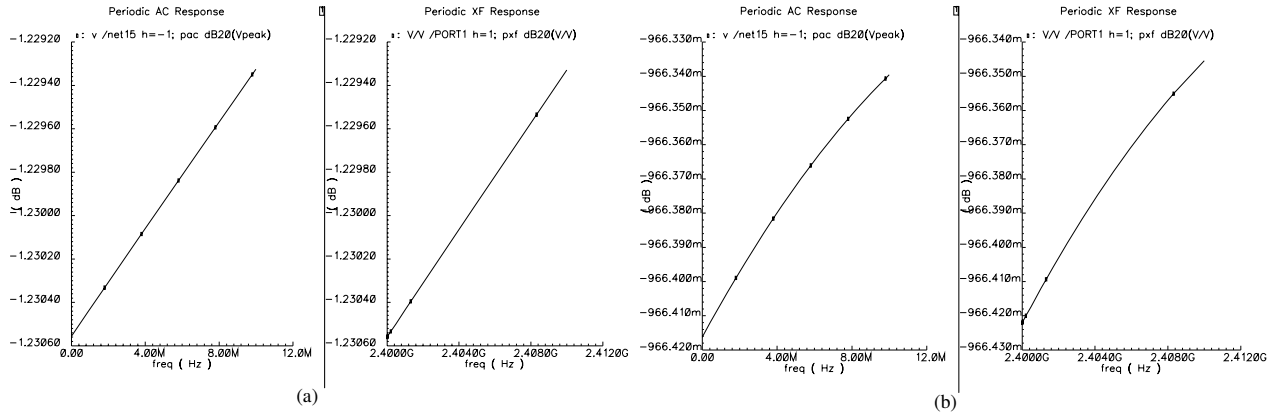

Fig. 5. Conversion Gain Estimation. Periodic AC and XF analysis with: (a) LO Power of -1 dBm, and (b) LO Power of $+2.5$ dBm.

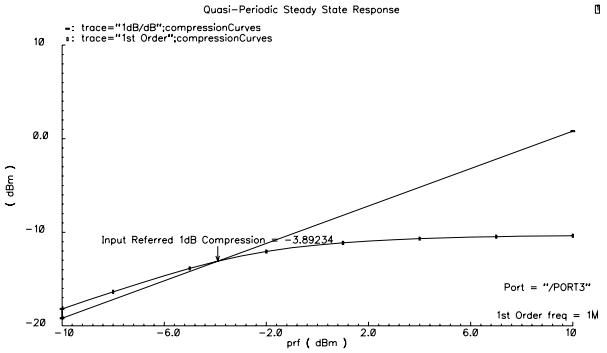

Fig. 6. Switch Mixer 1-dB Compression Point with LO Power of 2.5 dBm.

the strength and weakness of the proposed design. In fact, the implementation described in this paper has only been laid out and simulated; nevertheless the comparisons are carried out with implemented designs with measured data.

III. VCO

In modern RF applications such as zero or low-IF transceivers, the local oscillator must provide precise quadrature phases for either modulation or demodulation of the data streams in I and Q channels. This goal may be easily accomplished by using two crosscoupled VCOs. However, using a quadrature VCO leads to a huge area penalty and may also lead to an excessive power consumption that is not desirable in mobile applications. To tackle area and power overheads, oscillation frequency is doubled in order to decrease the size of passive elements. A divide-by-two circuit (DTC) is used to generate an oscillation frequency in the 2.4 GHz band. This, in turn, also improves by 6 dB the oscillator phase noise. The proposed VCO is shown in Fig. 7. The negative transconductance is implemented by the crosscoupled NMOS transistors, oscillation frequency is tuned by a NMOS inversion-mode varactor. All transistors are minimum length; transistors M1 and M2 are 40 μm wide whereas transistor Mb is 80 μm wide and is used to draw from the supply a bias current of $I_b = 1.45$ mA. Supply voltage is 1.2 V, hence VCO power consumption is 1.75 mW. Crosscoupled transistors M1 and M2 implement a negative resistance $R_i = -\frac{1}{g_m}$, where g_m is the transconductance of M1 and M2. The negative resistance

TABLE II
COMPARISON SUMMARY WITH PREVIOUSLY REPORTED IMPLEMENTATIONS.

Figure of Merit	This Work	[4]	[12]
LO Frequency	2.4 GHz	1.4 GHz	2.3 GHz
LO Voltage	420 mV	300 mV	280 mV
LO Power	$+2.5$ dBm	-0.4 dBm	-1 dBm
Noise Figure (SSB)	5.8 dB	10 dB	N/A
Conversion Gain	-0.96 dB	-3.6 dB	-2.9 dB
Input-Referred P1dB	-3.89 dB	-5 dBm	-1 dBm
LO-RF Isolation	72.40 dB	N/A	38 dB
Current Consumption	0 mA	N/A	< 0.1 mA
Die Area	0.18 mm^2	0.35 mm^2	0.21 mm^2
Technology	0.13 μm	0.35 μm	0.25 μm

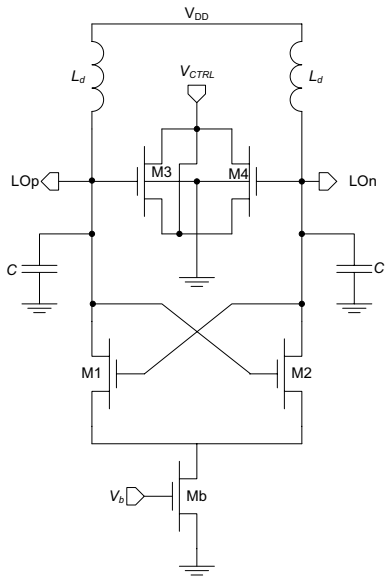

Fig. 7. Negative G_m Voltage Controlled Oscillator (Output Buffers and Bias Network not Shown).

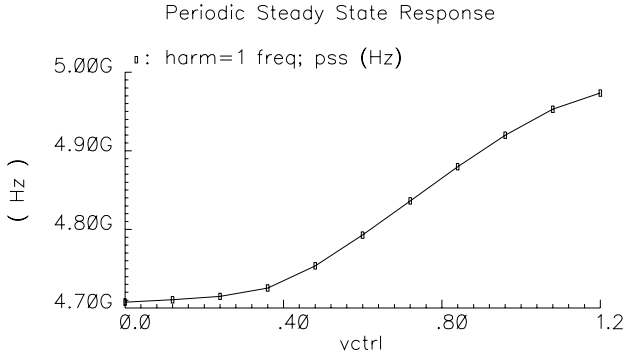

Fig. 8. VCO Oscillation Frequency vs. V_{CTRL}.

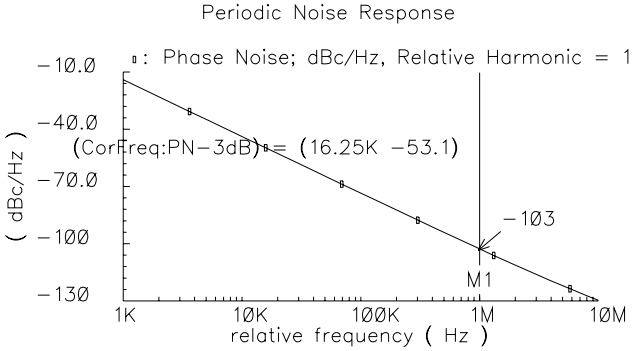

Fig. 9. VCO Phase Noise.

value is designed to cancel the inductor parasitic resistance, namely, $R_i = -2R_s(1+Q^2)$. R_s being the parasitic series resistance and Q the quality factor of the inductor. In this way power is transmitted from the inductor to the capacitance of the LC tank and vice versa, and the circuit oscillates. In order to start the oscillation transistor transconductance must be at least $g_m \geq \frac{R_s C_{tank}}{L_{tank}}$, where L_{tank} and C_{tank} are, respectively, the inductance and the capacitance of the LC tank of the oscillator. Bias, parasitics and inductor quality factor also affect the oscillator output swing ΔV, since $\Delta V = R_s I_b(1+Q^2)$ [6]. Bias current must be kept low to minimise power consumption, hence, due to the square dependence on Q, inductors quality has a great impact on the output swing. High quality inductors are necessary if a high output swing is a major design concern.

The LC tank is formed by two inductors $L_d = 2$ nH, two capacitors $C = 323$ fF, and a MOS inversion-mode varactor formed by transistors M3 and M4. Transistors M3 and M4 are minimum length and 90 μm wide and must be carefully laid out in order to minimise gate resistance. In the practice they are implemented by folding the channel width into 90 fingers of 1 μm length. An inversion-mode varactor is better other implementations due to the smoothness of its gate capacitance versus v_{gs} characteristics. Fig. 8 shows the oscillation frequency as a function of the varactor control voltage V_{CTRL}. The designed VCO may oscillate between 4.711 (when $V_{CTRL} = 0$ V) and 4.997 GHz (when $V_{CTRL} = 1.2$ V) with a tuning range from 2.35 to 2.5 GHz (after the frequency division). In ZigBee a high tuning range is not a major concern since the useful band goes from 2.4 to 2.48 GHz; in addition, doubling the oscillation frequency drastically reduces inductors and capacitors size an values. The oscillation frequency may be tuned adjusting suitably the values of the inductors and capacitors forming the LC tank. In order to obtain a wider tuning range it is desirable to decrease inductance and increase capacitance. However, in this particular case a wide tuning range is not strictly necessary and, since inductors are small, further decreasing inductance value does not lead to a significant improvement in area occupation. Observe from Fig. 8 that the required frequencies are obtained by applying control voltages ranging from 0.6 to 1.2 V, thus the VCO gain is approximately 333 MHz/V. The ZigBee standard requires an oscillator phase noise at 1 MHz frequency offset from the carrier of at least -88 dBc/Hz [2]. The simulated phase noise is depicted in Fig. 8 and is -103 dBc/Hz at the required frequency offset. In addition, the subsequent frequency division improves the phase noise of other 6 dB [8]. As a consequence, the proposed VCO is suitable for ZigBee applications. Simulation results are summarized in Table III, whereas Table IV shows performance comparisons with other implementations. The figure of merit used in the comparisons is [9]:

$$FoM = PN(f_{off}) - 20\log_{10}\left(\frac{f_o}{f_{off}}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\text{ mW}}\right)$$

where, f_o is the oscillation frequency, f_{off} the frequency offset, $PN(f_{off})$ the phase noise computed at the frequency offset, and P_{DC} is the DC power consumption. The figure of merit takes into account three factors: noise figure of the oscillator, frequency of oscillation, and DC power consumption. The smaller is the figure of merit, the better the oscillator because this means that the oscillator is able to work at high frequencies with very low noise figure and power consumption. Observe that the proposed implementation has a figure of merit comparable to the best ones and the best power consumption. This is of paramount importance in portable systems applications. The phase noise is not the best, however it is improved by 6 dB by the subsequent DTC circuit and it is sufficient to comply with ZigBee specifications that require at least a -88 dBc/Hz phase noise at a frequency offset of 1 MHz from the carrier. In this case as well, the same remark previously made for the mixer applies. Hence also the comparisons of Table IV are qualitative since the comparison is carried out between a laid-out and fabricated designs.

TABLE III
SUMMARY OF VCO PERFORMANCE.

Parameter	value
Frequency Tuning	6.5%
Phase Noise @ 1 MHz	-103 dB
VCO gain	333 MHz/V
Current Consumption	1.45 mA
Supply Voltage	1.2 V
Die Area	0.11 mm^2
Technology	0.13 μm CMOS

TABLE IV
COMPARISONS SUMMARY WITH PREVIOUSLY REPORTED IMPLEMENTATIONS.

Implementation	Power Consumption	Phase noise (@ 1 MHz)	Operating frequency	Technology	FoM (dB)
[10]	5.40 mW	−120 dBc/Hz	1 GHz	0.18 μm	−172.67
[11]	2.70 mW	−107 dBc/Hz	5.15 GHz	0.18 μm	−176.91
[12]	2.78 mW	−114.6 dBc/Hz	2.4 GHz	0.25 μm	−177.70
This work	1.75 mW	−103 dBc/Hz	2.5/5 GHz	0.13 μm	−174.01

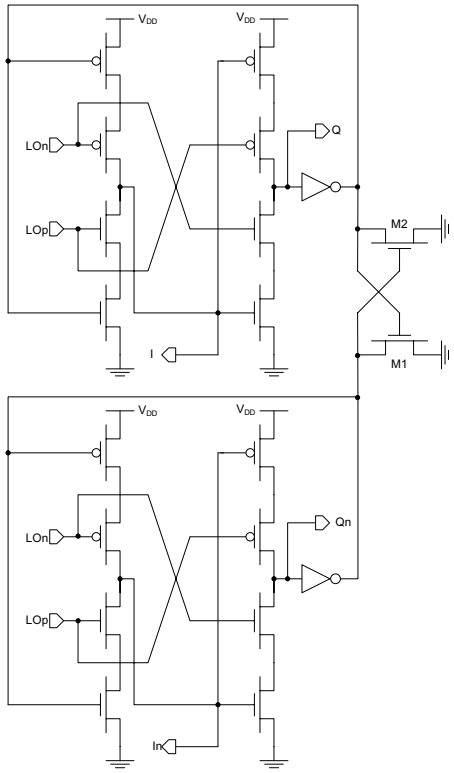

Fig. 10. Divide by Two Circuit Based on Clocked CMOS Latches.

A. Frequency Divider

Several DTCs have been reported [7]. The proposed topology is shown in Fig. 10 and is based on clocked CMOS latches [5]. A circuit branch generates quadrature and in phase components, whereas the other one generates de inverted waveforms. The output NMOS latch is used to force the feedback paths at opposite values (i.e., one at 0 V and the other at V_{DD}). The latch must be carefully sized: transistor must be big enough to make the outputs switch fast, but small enough in order not to overpower the strength of the output inverters and not to load excessively the feedback path. In the implementation of Fig. 10 all the PMOS transistors are 30 μm wide and all the NMOS transistors are 10 μm wide. The feedback crosscoupled NMOS latch M1 and M2 are asymmetric in order to speed-up the commutation to a stable state (either 0 V or V_{DD}) at power-up. Transistor M1 is 20 μm, whereas transistor M2 is 10 μm wide.

IV. CONCLUSION

In this paper, a passive switch mixer and a VCO suitable for low power operation have been proposed. The mixer switching core is a typical double-balanced architecture; however, each switching element is implemented by the parallel connection of two NMOS transistors to reduce the overall on resistance. To tackle the nonlinearity problems that may arise for large RF inputs, transistors gates are biased very close to threshold voltage. Matching is straightforward and is implemented by two inductors that cancel the imaginary parts of the source impedances. The simplicity of the matching network helps to reduce both the area occupation and the noise figure of the mixer.

The VCO is a typical negative G_m architecture tuned by an inversion-mode NMOS varactor. In order to decrease the size of passive elements, the LC tank has been designed to resonate at 5 GHz. A divide-by-two circuit is used to divide the VCO output frequency, shifting the operating frequency into the 2.4 GHz band, and to improve its phase noise. The oscillator tuning range is sufficiently wide to cover the frequency range from 2.4 to 2.48 GHz, making this design suitable for ZigBee applications. Both designs have a small area overhead compared with other similar implementations. The reduced number of passive elements, the good overall performances, and the extremely low power consumption makes the proposed design very appealing for low-cost and low-power applications.

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