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A 3rd order 3bit Sigma-Delta Modulator with Reduced Delay Time of Data Weighted Averaging

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***Abstract*—**This paper presents a method of reducing the feedback delay time of DWA(Data Weighted Averaging) used in sigma-delta modulators. The delay time reduction results from the elimination of the latch at the quantizer output and also from the falling edge operation. The designed sigma-delta modulator improves the timing margin about 16%. The sub-circuits of sigma-delta modulator such as SC(Switched Capacitor) integrator, 9-level quantizer, comparator, and DWA are designed with the non-ideal characteristics taken into account. The sigma-delta modulator has a maximum SNR (Signal to Noise Ratio) of 84 dB or 13 bit resolution.

***Keywords*—**Sigma-delta modulator, multibit, DWA

I. Introduction

Oversampling analog to digital and digital to analog converters employing sigma-delta modulators have been popular in high resolution applications, such as digital audio, where a large dynamic range is required for low bandwidth signal of less than 22 KHz[1]. Recently, due to rapid development of VLSI process, sigma-delta modulators are now being applied to wideband communication systems. Therefore, a sigma-delta modulator should be able to handle a signal with over several MHz bandwidth and maintain a high SNR at a lower oversampling ratio

Two methods have been used to increase the SNR of a modulator. One is to use a high order loop structure which can be realized either by using a single loop configuration or by using the MASH(Multi Stage Noise Shaping) structure. The other is to increase the number of quantizer bits[2-4]. When the number of quantizer bits is increased, the SNR of the sigma-delta modulator decreases because of capacitance mismatch. To overcome the capacitance mismatch problem, DEM(Dynamic Element Matching) techniques can be used. In implementing the DEM techniques, a DWA is commonly used to reduce the hardware complexity[5].

In this work, a new structure of DWA for high speed sigma-delta modulator is proposed. The proposed DWA decreases the feedback delay time by eliminating the latch and the second clock. So the timing margin is increased, leading to a more stable operation. A gain boosting scheme is used to implement the amplifier used in the integrator. The designed sigma-delta modulator has 84 dB SNR or 13 bit resolution.

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II. Circuit Implementation

A. Sigma-Delta Modulator Structure and Coefficients Determination

The sigma-delta modulator using a high order loop structure has a disadvantage in stability. Although the stability of MASH structure is guaranteed, the quantization noise of each stage is not perfectly cancelled in the digital filter. A 3rd order single loop structure is chosen in consideration of stability and the noise shaping property. In addition, a 3bit quantizer is adopted considering the signal to noise and the required hardware complexity. The block diagram of the resulting 3rd order 3 bit sigma-delta modulator is shown in Fig. 1.

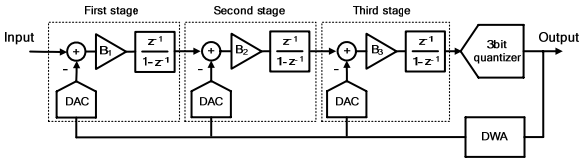


Fig. 1 Structure of 3rd order 3bit sigma-delta modulator

The coefficients are obtained through the behavior simulation. The maximum SNR of sigma-delta modulator is 87 dB. When B_2 is 0.8 and B_3 is 2, as can be seen in Fig. 2.

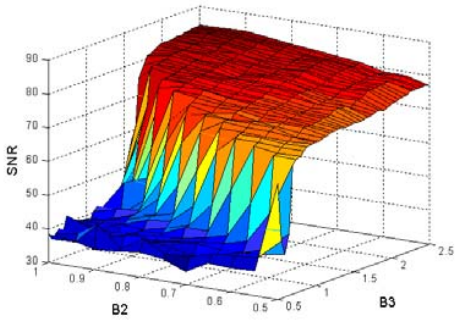


Fig. 2 The SNR characteristic of the modulator as a function of the integrator gain coefficients(B_1=0.33)

B. SC Integrator and DAC

The circuit of the SC integrator with feedback DAC (Digital to Analog Converter) is shown in Fig. 3. The SC integrator needs a two-phase non-overlapping clocks(with delay) such as ph1, ph1d, ph2, and ph2d. When the ph1 is high, the input signal is sampled by the unit capacitor block. When the ph2 is high, the SC integrator performs the integration and digital to analog conversion. The SC serves both as sampling capacitors and DAC capacitors. So, the area of capacitors is reduced by 1/2.

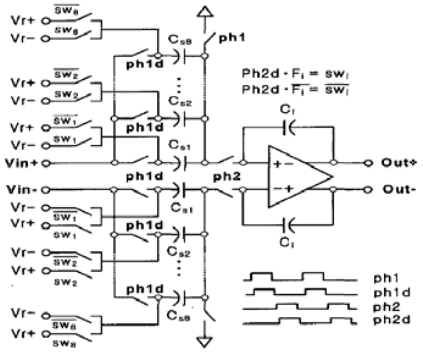


Fig. 3 SC integrator and feedback DAC

To reduce power consumption, the total capacitance used in SC integrator needs to be decreased. However, the noise floor in the signal band must be considered. The needed capacitance can be expressed in (1)[6]. In this work, the sigma-delta modulator needs at least 1.4 pF of the total capacitance. If each unit capacitor has 200 fF, the total capacitance is 1.6 pF. The feedback capacitance in the integrator must be 4.8 pF to make the coefficient 0.33.

$$C_{s,total} = \frac{8KT \cdot DR}{OSR \cdot V_{FS}} \quad (1)$$

Fig. 4 shows the amplifier of the first stage. A gain boosting technique and rail-to-rail structure are used in the amplifier of first stage because of required high gain. Table I shows the performances of amplifiers in each stage.

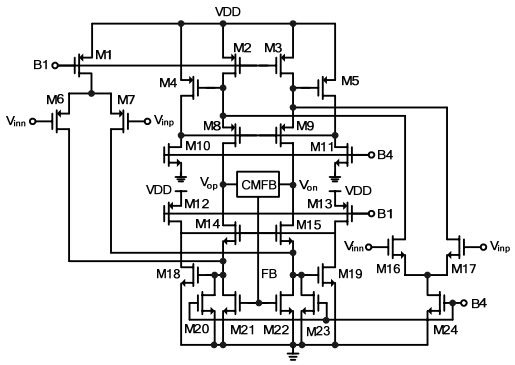


Fig. 4 Amplifier of the first stage

TABLE I
PERFORMANCES OF AMPLIFIER

	Amp1	Amp2, 3
Gain[dB]	93	64
Bandwidth[MHz]	405	160
Phase Margin[°]	70	60
Output Swing[V]	±0.85	±1
Slew Rate[V/μs]	200	150

C. DWA

Due to the mismatch of DAC capacitances, the SNR of sigma-delta modulator decreases. If a thermometer code selects the same combination of unit capacitors, the error due to capacitance mismatch continues to occur for the same input word. In the DEM method, the combinations of unit capacitors are dynamically chosen to reduce the average mismatch error. If the clock frequency of sigma-delta modulator is to be increased, the feedback delay time of thermometer code must decrease. In this work, the quantizer and DWA must operate within 8ns because the sigma delta modulator has a clock frequency of 52.8 MHz and an oversampling ratio of 24. Fig. 5 shows the block diagram of the conventional DWA.

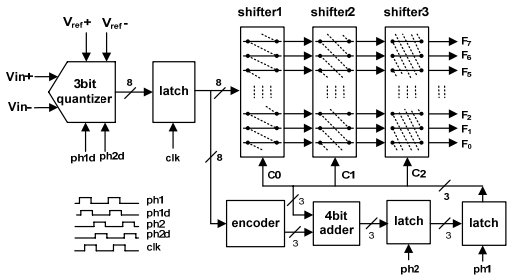
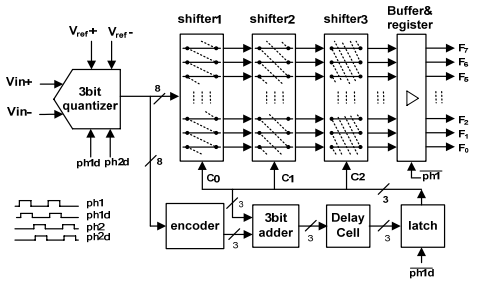
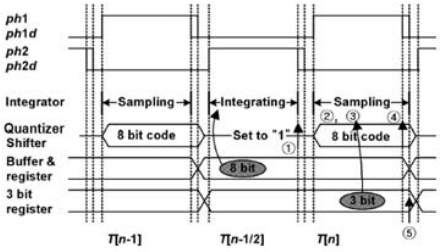


Fig. 5 The block diagram of conventional DWA

The ph1, ph2 and another cock are used in the conventional DWA. These clocks increase the feedback delay time. The proposed DWA eliminates three latches and thus reduces the feedback delay time. Fig. 6 shows the block diagram and the timing diagram of the proposed DWA. The principle of operation can be explained as follows, based on the timing diagram in Fig. 6 (b).



(a)



(b)

Fig. 6 Proposed DWA (a) block diagram, (b) timing diagram

- When the ph2d changes from ' 1' to ' 0' , the 9-level quantizer samples the output of integrator.
- The output of integrator is converted to 8 bit code by the quantizer.
- Thermometer code is passed to shifter1, shifter2, and shifter3 following control signals(C0, C1, and C2).
- Thermometer code is saved in 8 bit buffer by signal.
- Shift control signal that generates 3 bit register is encoded by signal.

The proposed DWA latches the quantizer output on the falling edge of ph1. The sigma-delta modulator with the proposed DWA increases the timing margin. The timing margin can be expressed in (2) and (3). The conventional DWA structure needs 31.25 % of 8 ns which is the maximum allowable time, but the proposed DWA structure has a delay time of 15 %.

$$\frac{Delay\,time\ of\ conventional\ DWA}{Periode\ of\ Ph1} = \frac{D_Q + 3\times D_S + CLK_M}{8n} = \frac{0.7n+1.5n+0.3n}{8n} \Rightarrow 31.25\% \quad (2)$$

$$\frac{Delay\,time\ of\ proposed\ DWA}{Periode\ of\ Ph1} = \frac{D_Q + D_S}{8n} = \frac{0.7n+0.5n}{8n} \Rightarrow 15\% \quad (3)$$

III. Simulation

Fig. 7 shows the output of DWA. The operation of the proposed DWA is verified by checking the thermometer codes. For example, the code 1000 0000 is followed by the code 0100 0000. The input signal has a magnitude of 1.2 Vp-p and the frequency of 825 KHz. The sampling frequency of sigma-delta modulator is 52.8 MHz. Fig. 8 shows the output of the sigma-delta modulator. The waveform shows the quantization levels of the input signal.

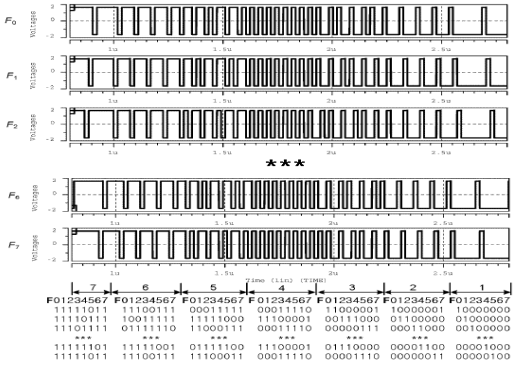


Fig. 7 Output of the thermometer code

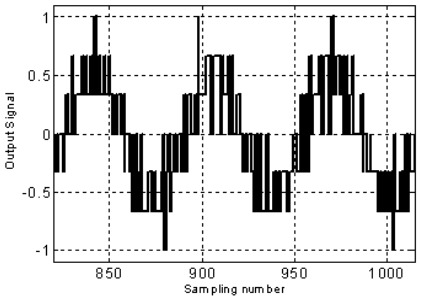


Fig. 8 Output waveform of sigma-delta modulator

The output spectrum of sigma-delta modulator is shown in Fig. 9. The SNR of the sigma-delta modulator is 84 dB. Table II shows the performances of 3rd order sigma-delta modulator with the proposed DWA.

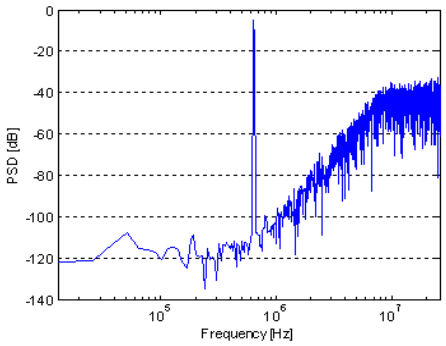


Fig. 9 Output spectrum of sigma-delta modulator

TABLE II
Performances Summary

	Sigma-Delta Modulator
Signal Band	1.1 MHz
Sampling Frequency	52.8 MHz
Peak SNR	84 dB
OSR	24
Power Supply	3.3 V

IV. Conclusion

This paper presents a method of reducing the feedback delay time in DWA. The proposed DWA only needs a delay time of only 1.2 ns. The timing margin is increased, leading to a more stable operation. The 3rd order 3bit sigma delta modulator with the proposed DWA has 13bit resolution or maximum SNR of

84 dB. The sigma delta modulator is designed using a 0.35 ㎛ CMOS process and can be applied to wideband applications.

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