

# Development of State Model Theory for External Exclusive NOR Type LFSR Structures

Afaq Ahmad

**Abstract**—Using state space technique and GF(2) theory, a simulation model for external exclusive NOR type LFSR structures is developed. Through this tool a systematic procedure is devised for computing pseudo-random binary sequences from such structures.

**Keywords**—LFSR, external exclusive NOR type, recursive binary sequence, initial state - next state, state transition matrix.

## I. INTRODUCTION

BINARY sequences whose terms depend in a simple manner on their predecessors are of great importance for a variety of applications. Such sequences are easily generated by recursive procedures and popularly known as with many names like Recursive Binary Sequences (RBS), Pseudo Random Binary Sequences (PRBSs), Maximal length sequences (m-sequences), and Pseudo Noise (PN) sequences [1 - 9]. Such kinds of sequences have an advantageous feature from the computational viewpoint, and they tend to have useful structural properties [10 - 19]. Due to only these structural properties, PRBSs have enormous applications for example: Direct Sequence Spread Spectrum (DSSS) [9, 20], Pseudo-random Number (PN) [1 - 20] generation, Built-in Self-Test (BIST) [21 - 40], Encryption - Decryption [41, 42] and Error Detection [3 - 5], [9] and many more.

The PRBSs can be easily generated by the use of simply extended circuits of shift registers, which is popularly known as Linear Feedback Shift Registers (LFSRs). Different types of LFSR structures are being used in various applications. These structures are broadly classified as:

- o External Exclusive OR (EEO),
- o External Exclusive NOR (EENOR),
- o Internal Exclusive OR (IEOR), and
- o External Exclusive OR (EEO) types.

Mathematical models of IEO and EEO structures are generously discussed in research literatures [1 - 9], [16], [18], [21], [23], [43]. But the theory and model of EENOR type of structure are not available right now although it is highly

applicable in VLSI test technology. This paper presents a state model theory for EENOR type LFSR structure. An algorithmic simulation procedure is also described through this paper.

## II. LFSR THEORY

An LFSR is made up of two parts: a shift register and a feedback function as shown in Fig. 1. The n-bit shift register is a chain sequence of n-bits of D – flip-flops. Each time a new bit is needed to load the first bit of the chains of D type flip-flops (see Fig. 2a, for D type flip-flop). The all others of the bits in the shift register are shifted one bit to the right. The feedback function is simply the Exclusive-NOR (Fig. 2b refers to Exclusive-NOR function) of certain bits of the register. The list of these bits is called feedback tapplings. The new left most bit's state (first bit of D – flip-flops) is computed as a function of the existing feedback tapplings of feedback function of the shift register. Since the exclusive NOR operation is carried out externally, therefore, such structure is called EENOR type of LFSR structures.

CLOCK

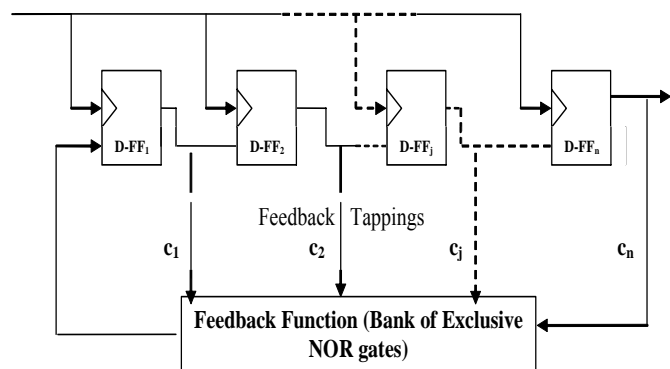


Fig. 1 A General Model of an n-bit LFSR

The output of the feedback shift register is one bit at each clock, often the most significant bit a clock before. The period of a shift register is the length of the output sequence before it starts repeating. An example of such generated sequence is as:

$a = [01110100101011010111010010101101]$ , having period  $p = 16$  time unit, is represented in signal form in Fig. 3. Shown in Table I is one such of the patterns produced by the LFSR of 5-bit in size having structure of Fig. 4, with the assumption

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that the bit pattern of 00001 was used as an initial state and feedback tappings are taken from 3<sup>rd</sup> and 5<sup>th</sup> bits of flip-flops.

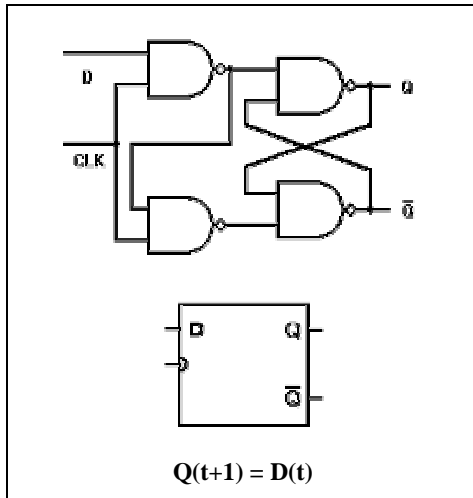


Fig. 2a Theory and model of D type flip-flop

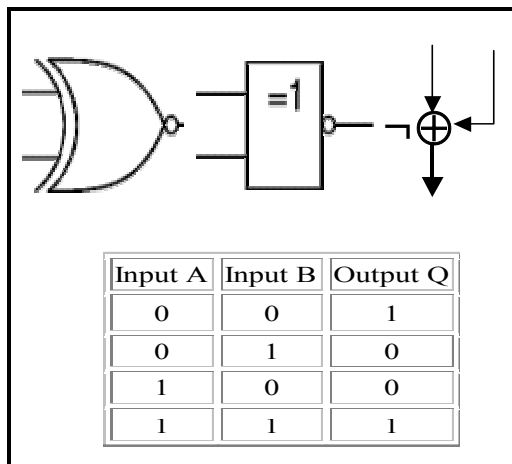


Fig. 2b Theory and model of exclusive or function

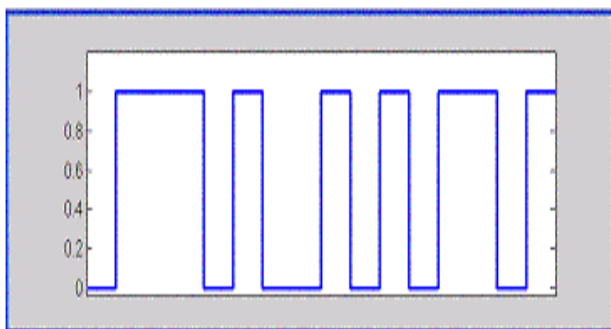


Fig. 3 waveform of the PRBS

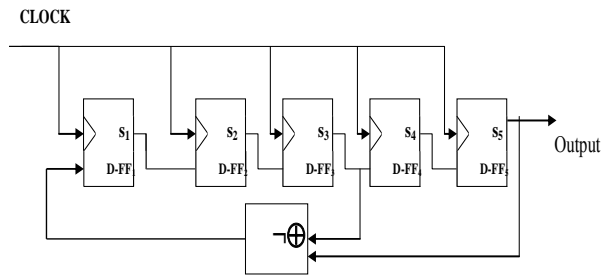


Fig. 4 a 5-bit LFSR

TABLE I  
PRBS GENERATED BY LFSR STRUCTURE OF FIG. 4

Clock	D-FF1	D-FF2	D-FF3	D-FF4	D-FF5	Comment
0	0	0	0	0	1	Seed
1	0	0	0	0	0	
2	1	0	0	0	0	
3	1	1	0	0	0	
4	1	1	1	0	0	
5	0	1	1	1	0	
6	0	0	1	1	1	
7	1	0	0	1	1	
8	0	1	0	0	1	
9	0	0	1	0	0	
10	0	0	0	1	0	
11	1	0	0	0	1	
12	0	1	0	0	0	
13	1	0	1	0	0	
14	0	1	0	1	0	
15	1	0	1	0	1	
16	1	1	0	1	0	
17	1	1	1	0	1	
18	1	1	1	1	0	
19	0	1	1	1	1	
20	1	0	1	1	1	
21	1	1	0	1	1	
22	0	1	1	0	1	
23	1	0	1	1	0	
24	0	1	0	1	1	
25	0	0	1	0	1	
26	1	0	0	1	0	
27	1	1	0	0	1	
28	0	1	1	0	0	
29	0	0	1	1	0	
30	0	0	0	1	1	
31	0	0	0	0	1	Starts repeating

Period of Pseudorandom PRBS is 31 (which is  $2^5-1$ ). The generated sequence is of maximal length.  
Pseudorandom PRBS (1 0 0 0 0 1 1 1 0 0 1 0 0 0 1 0 1 0 1 1 1 1 0 1 1 0 1 0 0 1)

### III. LFSR STATE MODEL

Let, for an n-stage LFSR shown in Fig. 1, [A] represents the state transition matrix of an  $n \times n$  order. Let the state at any time 't' be represented by vector  $[S(t)] = [s_1(t), s_2(t), \dots, s_n(t)]$  (which is effectively the contents of the LFSR) where each  $s_j$  represents the state of the  $j^{\text{th}}$  stage of the LFSR. Further, let the LFSR stage is numbered from 1 to n, proceeding in the same direction as the shifting occurs. Let the present state of the LFSR be represented by  $[S(t)]$  and, one clock later, the next state by  $[S(t+1)]$ ; then the relationship between the two states is given by:

$$\begin{bmatrix} s_1(t+1) \\ s_2(t+1) \\ \vdots \\ s_j(t+1) \\ \vdots \\ s_{n-1}(t+1) \\ s_n(t+1) \end{bmatrix} = \begin{bmatrix} c_1 \neg & c_2 \neg & c_3 \neg & \vdots & c_{n-2} \neg & c_{n-1} \neg & 1 \\ 1 & 0 & 0 & \vdots & 0 & 0 & 0 \\ 0 & 1 & 0 & \vdots & 0 & 0 & 0 \\ 0 & 0 & 1 & \vdots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \vdots & 1 & 0 & 0 \\ 0 & 0 & 0 & \vdots & 0 & 1 & 0 \end{bmatrix} * \begin{bmatrix} s_1(t) \\ s_2(t) \\ \vdots \\ s_j(t) \\ \vdots \\ s_{n-1}(t) \\ s_n(t) \end{bmatrix} \quad (1)$$

Where  $c_j \neg = 0$  or  $1$ , for  $1 \leq j \leq n-1$ , depends upon the existence or absence of the tap connections to the EENOR bank from the respective output of the flip-flops. And, since the last bit of the LFSR is always connected, therefore,  $c_n \neg = 1$ . The connection vector (CON) can be represented as,  $\text{CON} = [c_1 \neg \ c_2 \neg \ \dots \ c_{n-1} \neg \ c_n \neg]$ .

Equation (1) can be written as

$$[S(t+1)] = [A][S(t)] \quad (2)$$

If  $[S] = [S(0)]$  represents a particular initial loading of the LFSR, then the sequence of states through which the LFSR will pass during successive times is given by  $[S(t)], [A][S(t)], [A]^2[S(t)], [A]^3[S(t)], \dots$

Let the matrix 'period' be the smallest integer  $p$  for which  $[A]^p = I$ , where  $I$  is an identity matrix. Then  $[A]^p[S(t)] = [S(t)]$  for any non zero initial vector  $[S(0)]$ , indicating the 'cycle length (or period)' of the LFSR is  $p$ .

Thus, on the basis of this property of periodicity of LFSR and Equation (3), it follows that

$$[S(t)] = [S(t+p)] = [A]^p[S(t)] \quad (3)$$

#### IV. GF(2) FOR EENOR AND COMPUTATION METHOD

GF(2) multiplication and addition operations are described in Table II. The Table III contains developed models for EENOR multiplication and addition operations for the purpose of simulating Equation 1. Finally, the whole process for computing the next state sequences through state space model is summarized below in the form of an algorithm.

TABLE II  
GF(2) ADDITION AND MULTIPLICATION OPERATIONS

	+		X	
	0	1	0	1
0	0	1	0	0
1	1	0	0	1

TABLE III  
¬GF(2) ADDITION AND MULTIPLICATION OPERATIONS

	+		X		
	0	1	$c_i$	0	1
0	1	0	0	0	0
1	0	1	1	1	0

#### Algorithm

(For an n-bit LFSR)

#### STEP 1:

Check if CON has total number of  $c_j$ 's as odd number, then, Go To STEP 3, else Go To STEP 2.

#### STEP 2:

Compute the value of  $s_1(t+1)$  by using the Equation 4 described below. The computation is carried out using GF(2)

table for multiplication and  $\neg$  GF(2) for addition as described in Table 2 and 3 respectively. For computing  $s_1(t+1)$ , for  $j = 2, 3, 4, \dots, n$ ; Go To STEP 4.

$$s_{1(t+1)} = \sum_{j=1}^n c_j * s_{j(t)} \quad (4)$$

#### STEP 3:

Compute the value of  $s_1(t+1)$  as using the Equation 4 given above. The computation is carried out using tables GF(2) for

addition and  $\neg$  GF(2) for multiplication as described in Table 2 and 3 respectively. For computing  $s_{i(t+1)}$ , for  $j = 2, 3, 4, \dots, n$ ; Go To STEP 4.

#### STEP 4:

For other values of  $s_i(t+1)$ , for  $j = 2, 3, 4, \dots, n$ ; can be computed using Equation 5 as given below where the operations of addition and multiplications are carried out using GF(2) as given in Table II.

for  $j = 2, 3, 4, \dots, n$ ;

$$s_j(t+1) = s_{j-1}(t) \quad (5)$$

#### STEP 5:

STOP

#### V. COMPUTATION – AN EXAMPLE

To demonstrate the procedure of algorithm below is an example to make the steps more elaborative.

Let  $n = 4$ ,  $\text{CON} = [0 \ 1 \ 1 \ 1]$  which has 3 (odd) total entries.

Assume  $S = [1 \ 0 \ 1 \ 1] = (D)_{\text{Hex}}$

$$s_1(\text{next state}) = 0*1 + 1*0 + 1*1 + 1*1$$

$$s_1(\text{next state}) = 0 + 1 + 0 + 0 = 1$$

$$s_2(\text{next state}) = s_1(\text{previous state}) = 1$$

$$s_3(\text{next state}) = s_2(\text{previous state}) = 0$$

$$s_4(\text{next state}) = s_3(\text{previous state}) = 1$$

Thus,  $S(\text{next state}) = [1 \ 1 \ 0 \ 1] = (B)_{\text{Hex}}$  which can be verified from the Table IV (check upon  $s_0$  and  $s_1$  in column II of the table).

Let us consider another  $\text{CON} = [0 \ 0 \ 1 \ 1]$  which has 2 (even) total entries. Assume  $S = [1 \ 1 \ 0 \ 0] = (03)_{\text{Hex}}$

$$s_1(\text{next state}) = 0*1 + 0*1 + 1*0 + 1*0$$

$$s_1(\text{next state}) = 0 + 0 + 0 + 0 = 0$$

$$s_2(\text{next state}) = s_1(\text{previous state}) = 1$$

$$s_3(\text{next state}) = s_2(\text{previous state}) = 1$$

$$s_4(\text{next state}) = s_3(\text{previous state}) = 0$$

Thus,  $S(\text{next state}) = [1 \ 1 \ 1 \ 0] = (7)_{\text{Hex}}$  which can be verified from the Table IV (check upon  $s_0$  and  $s_1$  in column III of the table).

For  $n = 2$  to 32 EENOR LFSR structures are tested and results are verified. It is difficult to present the results, however, in Table V, the simulation results for  $n = 3$ , with all possible initial states ( $2^n$ ), and all possible CONs ( $2^{n-1}$ ) are given to put confidence in the readers.

TABLE IV  
AN EXAMPLE OF COMPUTATION FOR A 4-BIT LFSR

States	CON = [0 1 1 1] $s_0 = [1 \ 0 \ 1 \ 1] = (D)_{\text{Hex}}$	CON = [0 0 1 1] $s_0 = [1 \ 1 \ 0 \ 0] = (3)_{\text{Hex}}$
$s_0$	D	3
$s_1$	B	7
$s_2$	7	E
$s_3$	F	D
$s_4$	E	B
$s_5$	C	6
$s_6$	9	C
$s_7$	2	9
$s_8$	4	2
$s_9$	8	5
$s_{10}$	0	A
$s_{11}$	1	4
$s_{12}$	3	8
$s_{13}$	6	0
$s_{14}$	D	1

TABLE V  
AN EXAMPLE OF COMPUTATION FOR A 3-BIT LFSR

States (in Hex)	CON = [1 0 1]	CON = [1 1 1]
$s_0$	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
$s_1$	1 3 5 7 0 2 4 6	1 3 4 6 0 2 5
$s_2$	3 7 6 1 0 4	3 6 0 5 1 4 2
$s_3$	7 6 4 3 1 0	6 5 1 2 3 0 4
$s_4$	6 4 0 7 3 1	5 2 3 4 6 1 0
$s_5$	4 0 1 6 7 3	2 4 6 0 5 3 1

## VI. CONCLUSION

A state model theory for an external exclusive NOR based LFSR structure is developed. Based upon which an algorithm

is developed to compute the PRBSs. Since a unified approach is not adapted in modeling the LFSRs therefore, this is an orientation to that direction. In future it is highly desired to observe a standard approach for modeling any kind of LFSR i.e. internal or external structures with exclusive OR or NOR based feedbacks. Currently, a lot of scope of research is highly demanding due to outburst applications of LFSRs.

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