International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:2, No:2, 2008

A Reversible CMOS AD / DA Converter Implemented with Pseudo Floating-Gate

Omid Mirmotahari, Yngvar Berg, and Ahmad Habibizad Navin

Abstract**—**Reversible logic is becoming more and more prominent as the technology sets higher demands on heat, power, scaling and stability. Reversible gates are able at any time to ”undo” the current step or function. Multiple-valued logic has the advantage of transporting and evaluating higher bits each clock cycle than binary. Moreover, we demonstrate in this paper, combining these disciplines we can construct powerful multiple-valued reversible logic structures. In this paper a reversible block implemented by pseudo floating-gate can perform AD-function and a DA-function as its reverse application.

Keywords**—**Reversible logic, bi-directional, Pseudo floating-gate (PFG), multiple-valued logic (MVL).

I. Introduction and Background

REVERSIBLE logic is an emerging research area. Interest in this field is motivated by its applications in several technologies. Binary reversible circuits have been studied for their potential application in low-power CMOS design, quantum computation, optical and nanotechnology. Reversibility is essentially the possibility to choose whether to execute or to ”undo” the current step. The term ”reversible computing” refers to any computational process that is (at least to some close approximation) reversible. There are two major, closely related, types of reversibility that are of particular interest for this purpose: *physical reversibility* and *logical reversibility*. A process is said to be physically reversible if it results in no increase in physical entropy; it is isentropic. The first attempt to study reversibility in computing processes was described by Landauer in 1961 [1]. He was also the first to use the expression logically reversible to denote a computation where the outputs uniquely map the inputs. Furthermore, he states that in order for a computational process to be physically reversible, it must also be logically reversible. This statement is called Landauer’s principle. A discrete, deterministic computational process is said to be logically reversible if the transition function that maps old computational states to new ones is a one-to-one function (1-1 mapping). Probably the largest motivation for this study of hardware and software technologies aimed at actually implementing reversible computing is that they offer what is the only potential way to improve the energy efficiency of computers beyond the physical limits to computation given by the von Neumann-Landauer limit of kT ln 2 energy dissipated per bit operation, where k is Boltzmann’s constant of 1.38x10e-23 J/K and T is the temperature of the environment into which unwanted entropy will be expelled. The minimum energy requirements of a computation are proportional to the number of information bits destroyed during its course. In theory, by performing in a *reversible* manner, no information is lost or destroyed and thus potentially zero energy would be needed [2].

Omid Mirmotahari and Yngvar Berg are with the Nanoelectronic System Group at the Dept. of Informatics, University of Oslo in Norway (e-mail: omidmi@ifi.uio.no).

Ahmad Habibizad Navin is a member of Islamic Azad University Tabriz Branch, Tabriz, Iran.

In the last few decades multiple-valued logic has been proposed as a possible alternative to binary logic. Whereas binary logic is limited to only two states, ”true” and ”false”, multiple-valued logic (MVL) replaces these with finite or infinite number of values. An MVL system is defined as a system operating on a higher radix than two [3]. A radix-n set has *n* elements $\{0, 1, ..., n-1\}$. The feasibility of MVL depends on the availability of devices constructed for MVL operations [4]. The devices should be able to switch between the different logical levels, and preferably be less complex than their binary counterparts. Multiple-input floating-gate (FG) transistors can be used to simplify the design of multiple-valued logic [5]. Capacitively connecting the input signals to the transistor we achieve a floating-gate (FG). As the name implies, the gate is actually floating. The initial charge on the floating-gates may vary significantly and therefore substantial inaccuracy may occur unless some form of initialisation is applied. In order to control or assert a desired voltage level different techniques are available. There are two main different disciplines for programming or initialising the floating-gates that have arisen through the course of time. They are (1) *”once and for all”* (i.e. non-volatile) and (2) *frequent recharging* (i.e. volatile). Within each of the disciplines there are different techniques to obtain the desired voltage levels. For discipline (1) the well-known are Fowler-Nordheim tunnelling [6], hot-carrier injection [6] and UV-activated conductance [7]. It is worth emphasizing that discipline (1) has an disadvantage due to time-consuming initialisation of the floating-gates and leakage. For discipline (2) there are numerous different techniques. One of the most promising is the semi-floating-gate (SFG) [8], [9]. Recharge of the SFGs is accomplished by a local recharge transistor temporarily connecting the output to the floating-gate of a gate. Although the frequent recharging is subject to leakage (through the recharge transistor) it is better in terms of processing, designing/synthesis and the time consumption for initialising/programming of the floating-gate at start-up. One of the key advantages of the semi-floating-gate is the equilibrium state of $V_{dd}/2$ [8] achieved at input, output and the floating-gate during recharge. Although the design of the SFG is quite simple and the frequent recharging is made ”plug and play”, the design has led to more control overhead in terms of

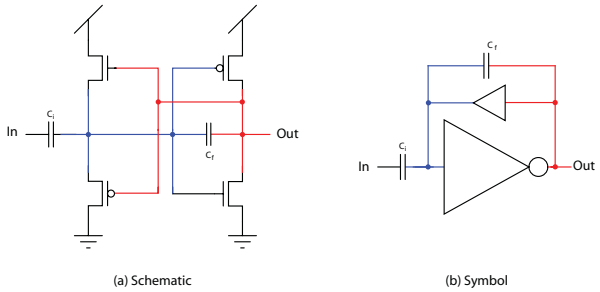

Fig. 1. The analog or multiple-valued pseudo floating-gate inverter is shown: the schematic (a) and the symbol (b). By removing the feedback capacitor, C_f, a binary pseudo floating-gate inverter is obtained. The transistors are matched and kept equal for both the inverter and the buffer. In our process the sizes are 2.95/0.35μm for pMOS and 0.4/0.35μm for nMOS, while the ratio for C_i/C_f is 1.2.

clocking strategies. It is also important to emphasise that the recharging of the floating-gate has not always made the design easier because the inputs have to include a recharge period. There are, nevertheless, gates that can solve this problem, but at a cost for larger designs. The SFG has had some glory days in the past few years, but as devices get smaller the recharge time seems to grow, thus limiting the operating frequency. A solution that might release the SFG from the recharge time is the pseudo floating-gate (PFG) [10]. Visually, the pseudo floating-gate is very similar to the semi-floating-gate (SFG). The difference lies in the use of a weak feedback buffer instead of the recharge switch. Furthermore, many of the SFG building blocks can be rebuilt using the PFG gate.

The outline of this paper is as follows: in section II the pseudo floating-gate (PFG) is presented. Simulation results verifying the design are included. Section III presents and elaborates on the bidirectional concept of the PFG. In section IV a reversible converter is presented. The converter implements an AD function and a DA as its reverse function. Finally, the paper concludes by emphasising the key aspects of this paper. The results demonstrated throughout this paper were obtained by simulations produced in an *AMS 0.35μm* process environment provided by Cadence.

II. The Pseudo Floating-Gate

The pseudo floating-gate (PFG), shown in Figure 1, was used in a frequency detecting application that suppresses low frequencies [11]. The design resembles the semi-floating-gates (SFG) and therefore many of the same applications (as for SFG) may apply to the PFG. The main difference is the use of a feedback buffer instead of a switch. The feedback buffer can be implemented, among others, as a voltage follower. Although this may not be the ideal feedback in terms of linearity, it adds simplicity and symmetry as far as synthesis and layout are concerned. In contrast to the past, one of the first noticeable characteristics after some test simulations was the increased operating frequency. The characteristics resemble a band pass filter. Moreover, it was found that the high cut-off frequency is determined by the inverter‘s response limit, while the low cut-off frequency is dependent on the response for the feedback buffer. The gain of the band pass filter can be made higher by increasing the input capacitances, thus transferring more of the input signal. Our hand calculations indicated a band pass of a maximum three decades. Given enough time and assuming ideal conditions the PFG would settle at an equilibrium state $V_{dd}/2$ (DC-point). Moreover, the design has been treated such that it operates on low-voltages, in fact as low as $2V_t$. The pseudo floating-gate used to implement multiple-valued logic (MVL) was first demonstrated in [10]. The author’s main goal was to release the traditional SFG MVL design from the recharge mode and thus emphasised the design’s ability to operate in continuous mode. In Figure 2 the multiple-valued voltage level transitions are shown. These results clearly demonstrate the speed and functionality of the PFGs and, moreover, their ability to operate on either binary, analog or multiple-valued logic and also their operational mode of either recharge or continuous.

III. Bidirectional Property

In order to obtain a bidirectional property, it is obvious that the design must be symmetrical in order to obtain the same conditional for each direction. The pseudo floating-gate consists of an inverter and a weak buffer feedback. One of the first solutions to the symmetrical approach is to use voltage follower as the weak feedback buffer. This fulfils the symmetrical property owing to the fact that the voltage follower can be constructed by an inverter. The only difference is to invert the references, i.e. swap the V_{dd} and Gnd. The pseudo floating-gate obtains a bidirectional property by introducing a control signal (**Ctrl**) as its reference. The key idea is to have the gate’s reference provided by a desired voltage level (primarily V_{dd} or Gnd). As Figure 3 illustrates, a control signal (**Ctrl**) has been included at the reference. With the ability to assert a voltage level at the reference signals the signal direction can be directly

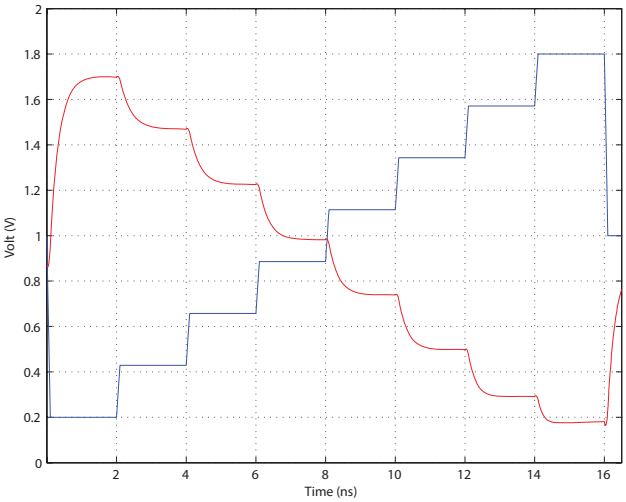

Fig. 2. The simulation result for the pseudo floating-gate inverter in the context of MVL. A single input PFG in continuous mode with input ranging from 0.2V to 1.8V with a frequency of 500MHz. The steps are a little smaller compared with the input, but are justifiable within the noise margin.

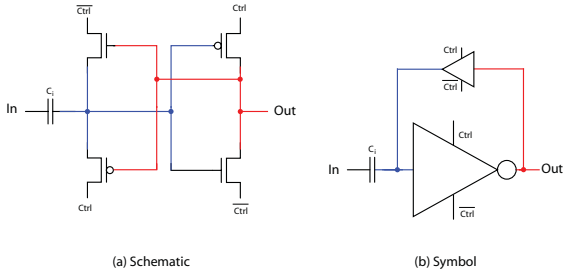

Fig. 3. The single-input binary PFG inverter is shown: the schematic (a) and the symbol (b). The inverter signal direction is operated by a control signal (**Ctrl**) at the reference. With Ctrl = V_{dd} the signal is processing from left to right, and vice versa when Ctrl = Gnd. The transistors are matched and are kept equal for both the inverter and the buffer.

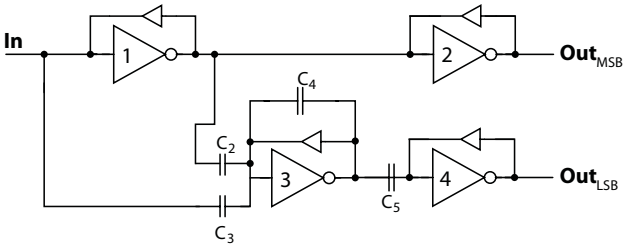

Fig. 4. A radix-4 to binary (AD) converter implemented with pseudo floating-gates is illustrated. The transistor sizes are kept at a minimum and matched, while the capacitors are C_2 = 5fF, C_3 = 7fF, C_4 = 6FF and C_5 = 10fF. We have intentionally not pictured the control signals (**ctrl**) here for the sake of clarity. All the PFG gates have the ctrl signal included within each block. This ctrl signal is used to enable the bidirectionality and hence the reverse function.

controlled through the gate. By changing the reference voltage it is possible to choose which of the two inverters in the PFG becomes an inverter or a feedback buffer. When changing the signal direction, one aspect obviously needs to be discussed and from that the question ”how to make an output to become a capacitively coupled input” arises. The answer is found by looking at the next block, because when inverting the signal direction, the floating-gate of the next PFG actually becomes the input. Hence, the output is the floating-gate. This ability to have a bidirectional property will motivate new and powerful designs. One of the major improvements will be to link the bidirectionality to reversible logic. Whereas some authors [12] have demonstrated designs which link multiple-valued logic to reversible logic, our structures can operate on multiple-valued logic and, in addition, have the bidirectional property.

IV. A Reversible Converter

The earlier PFGs were claimed to handle both binary as well as multiple-valued signals. In the following a multiple-valued to binary converter will be presented that has the ability to be reversible by changing the signal direction, i.e. an ”undo” step, without losing any information. First, the multiple-valued to binary converter (hereby referred to as AD) is shown in Figure 4. This converter operates at a multiple-value radix of 4, i.e. the signals can have up to 4 levels. Simulation results, shown in Figure 7, verify the operation of the design. In our approach time has been dedicated to evaluating the design’s logical behaviour. Therefore, many adjustments can be made to obtain much more stable and faster level transitions.

Using the possibility of altering the signal direction, as described earlier in this paper, a reversible function of the AD can be obtained, which is a DA (binary to multiple-valued) converter. This reversible function and how the reversed design in Figure 4 would look is shown in Figure 6. The verifying simulation results are shown in Figure 7. Some may point out that the AD and the DA are not perfectly alike, and that some more elements are added. The explanation is that by altering the signal direction the output becomes the input and vice versa. Owing to the design of the PFG, all inputs must be a floating-gate, therefore in the case of the DA a capacitor is added to the input (see Figure 6 grey area). In a larger design, the capacitor would actually be the next gate’s floating-gate which is included.

Although the pseudo floating-gate is a continuous mode design, we have included a control signal to enable the bidirectionality. This added feature therefore includes timing issues. To our knowledge and experience we have not had difficulties with the timing. We have found out that as long as the signal direction is reversed during a period where all the signals are $V_{dd}/2$.

V. Conclusion and Discussion

In this paper we have linked reversible logic with multiple-valued gates. We have chosen to use the pseudo floating-gate as a general gate, due to its capacitive coupled input-signals, ability to handle multiple-valued signals and, not least, its symmetrical design whoch enables bidirectionality. As

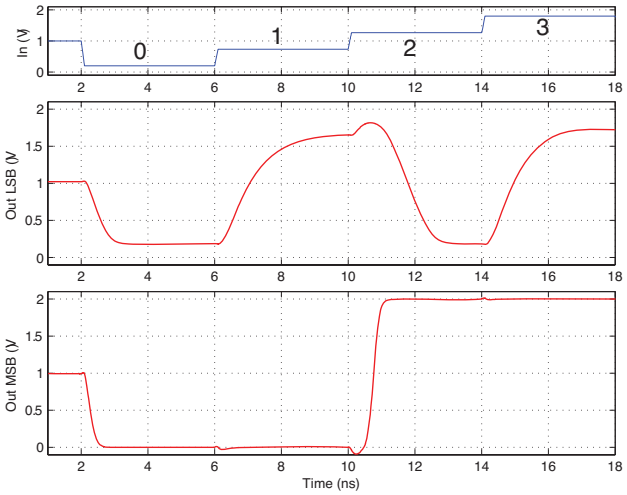

Fig. 5. The simulation results for the radix4 to binary converter shown in Figure 4 is presented. The AD’s logical behaviour is evident from these results. The only transition which has some latency is the logical level 2. The solution is to increase the width of the transistor in inverter no. 2 to obtain higher frequency response.

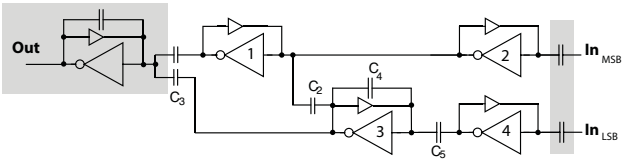

Fig. 6. The binary to radix4 (DA) converter is presented. This figure serves as a visual illustration of how the signal propagation through the block in Figure 4 appears, when the block is reversed. All the same capacitors and pseudo floating-gates are used. In order to reverse the signal direction some elements of the previous and next blocks are included. Those elements are illustrated by a grey area.

described in the paper, the size and ratio for the capacitances are the main keys to build up functions using these gates. A down-converting structure is chosen to serve as an example. Moreover, simulation results obtained by Cadence verifies the logical behaviour. Throughout the paper the underlying intention has been to link and unite the reversible logic to the MVL gates. We have not elaborated on the complete potential of the general PFGs, in gates, whereas using complex clocking schemes (controlling the bidirectionality) to construct new and powerful functions within the union of reversible logic and multiple-valued logic.

Our discussion has mainly focused on *logical reversibility* - the inputs and outputs of reversible logic gates that can be uniquely retrievable from each other (commonly know as 1-1 mapping). However, we have barely touched upon the *physical reversibility* which is the key issue as to whether we can build physical gates and circuits that can actually operate backwards and consume ”zero” energy.

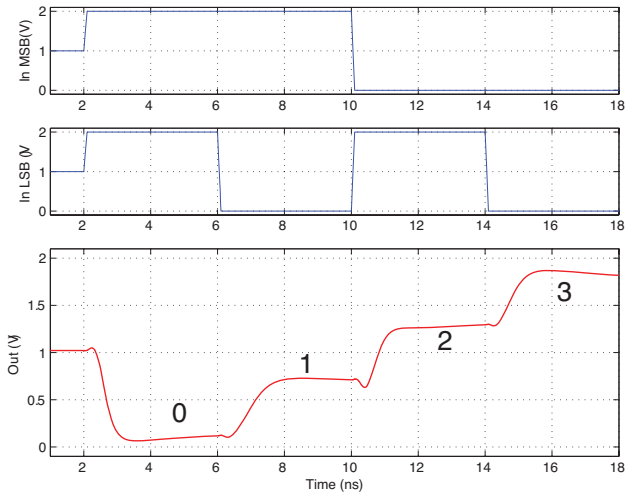

Fig. 7. The simulation results for the binary to radix-4 (DA) converter shown in Figure 6 is presented. All levels are within the noise margin. Focusing on a small detail it can be noticed that the output signal actually is the inverted as one would expect. This is due to the last inverter (i.e. inverter no. 0) added on the output. The actually correct output is the floating-gate of the inverter no. 0.

References

[1] R. Landauer. ”Irreversibility and Heat Generation in the Computing Process”. *IBM Journal of Research and Development*, 5(3):183–191, July 1961.
[2] C.H. Bennett and R. Landauer. ”The Fundamental Physical Limits of Computation”. *Scientific American*, 253(1):38–46, July 1985.
[3] K.C. Smith. ”Multiple-Valued logic: a tutorial and appreciation”. *IEEE Computers*, 21:17–27, April 1988.
[4] D. Etiemble. ”On the performance of the Multiple-Valued integrated Circuits: Past, Present and Future”. *Proceeding 22nd IEEE International Symposia on Multiple-Valued Logic (ISMVL)*, pages 154–164, May 1992.
[5] T. Shibata and T. Ohmi. ”A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations”. *IEEE Transactions on Electron Devices*, 39(6):1444–1455, June 1992.
[6] C. Diorio, S. Mahajan, P. Hasler, B. Minch and C. Mead. ”A High-Resolution Non-Volatile Analog Memory Cell”. *Proc. IEEE Intl. Symp. on Circuits and Systems*, 3:2233–2236, 1995.
[7] Y. Berg, T. S. Lande and Ø. Næss. ”Programming Floating-Gate Circuits with UV-Activated Condictances”. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 48(1):12–19, January 2001.
[8] Y. Berg, S. Aunet, O. Mirmotahari and M. Høvin. ”Novel Recharged Semi-Floating-Gate CMOS Logic for Multiple-Valued Systems”. *IEEE International Symposium on Circuits and Systems (ISCAS)*, 5:193–196, May 2003.
[9] K. Kotani, T. Shibata, M. Imai and T. Ohmi. ”Clocked-Neuron-MOS Logic Circuits Employing Auto-Threshold-Adjustment”. *IEEE International Solid-State Circuits Conference (ISSCC)*, 388:320–321, February 1995.
[10] O. Mirmotahari, J. Lomsdalen and Y. Berg. ”A Continuous Mode MVL Gate using Pseudo Floating-Gate”. *14th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, pages 185–189, June 2007.
[11] Y. Berg, O. Mirmotahari and S. Aunet. ”Pseudo Floating-Gate Inverter With Feedback Control”. *IFIP International Conference on Very Large Scale Integration (VLSI-SOC)*, 1:272–276, October 2006.
[12] O. Mirmotahari, Y. Berg, J. Lomsdalen and V. Øverås. ”Using Multiple-Valued Gates to Implement Reversible Logic”. *Ph.D. Research in Microelectronics and Electronics (PRIME)*, 1:361–364, June 2006.

Omid Mirmotahari Omid Mirmotahari received the M.Sc. degrees in micro-electronics from the Department of Informatics, University of Oslo, Norway, in 2003. He is currently working on a Ph.D. degree at the same department. His research activity is mainly focused on low-voltage/low-power digital and analog floating-gate design.

Yngvar Berg Yngvar Berg received the M.Sc. and Ph.D. degrees in micro-electronics from the Department of Informatics, University of Oslo, Norway, in 1987 and 1992, respectively.

He is currently a Professor with the same department. His research activity is mainly focused on low-voltage/low-power digital and analog floating-gate design. He is the author or coauthor of more than 110 papers.

Ahmad Habibizad Navin Ahmad Habibizad Navin id s member of Islamiz Azad University Tabriz Branch, Tabriz, Iran, Computer Department. He is also collaborated with computer Research laboratory, IAUT-CRL. He is also a part time member of Islamic Azad University Mamaghan branch mamagan, Iran.