

Efficient Electromagnetic Modeling of Dual-Gate Transistor with Iterative Method using Auxiliary Sources

Z. Harouni¹, L. Osman¹, M. Yeddes¹, A. Gharsallah¹ and H. Baudrand²

Abstract—In this paper, an efficient wave concept iterative process (WCIP) with auxiliary Sources is presented for full wave investigation of an active microwave structure on micro strip technology. Good agreement between the experimental and simulation results is observed.

Keywords—WCIP, Dual-Gate Transistor, Auxiliary source.

I. INTRODUCTION

VIEWED improving higher performance integrated circuits monolithic microwave MMIC which are becoming a density of active and passive devices on a single chip and given the increased frequency of work, having more accurate models that take into account the electromagnetic coupling in the model is needed. On the other hand, a simulation for reliable and have good performance for circuits must be accurate models for nonlinear devices. However, it is very difficult and slow to establish these models, as it requires the characterization of various device samples. The commercial electromagnetic tools take part largely in industrial designs [1], [2]. Indeed, the high cost of technology implemented and the time for the realization of a function of analogy electronics can not return the traditional approach consisting in testing several models of testing there to make the improvements necessary. The rules of scaling classical [3] and even with the geometric parameters that are limited by the available samples of the transistor can not provide reliable models.

The systematic modeling is time consuming and uneconomical. However, a theory of auxiliaries' sources is included [4], [5] and [6], they have an intermediary calculation role between the external domain and the active domain and they permit to calculate impedance of the circuit which can overcome the limitations of some analysis methods and are suitable for a general structure.

II. AUXILIARY SOURCE TECHNIQUE

The technique of the auxiliary source introduced in [5], [6] is used when the circuit includes elements with very different dimensions. We suppose that the thickness of the small circuit is very less. It is therefore equivalent to surface impedance. The small circuit can be a non-linear component; it is therefore equivalent to non-linear surface impedance.

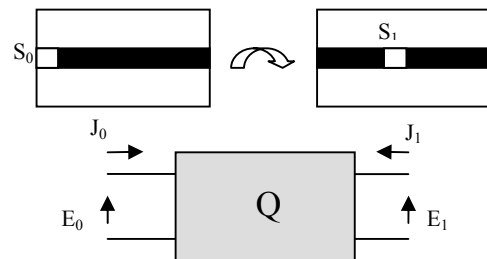


Fig. 1 A planar circuit including one principal source (S_0) and one auxiliary source (S_1).

For example, if a circuit is composed by a principal source S_0 , conductor and surface impedance S_1 , this technique consists of replacing S_1 by an auxiliary source and to calculate the coupling two-port network Q between S_1 and S_0 . The two-port network Q is closed by the impedance of S_1 . Finally we can deduce the relative impedance in the principal source S_0 . S_0 , (auxiliary source) is a passage tool between a large scale and a small scale. An electromagnetic calculus is used to obtain the characteristics of the large scale, whereas the small scale corresponds to a connection element where the characteristics are given elsewhere. The different interactions between principals and auxiliary sources are illustrated in Fig. 2.

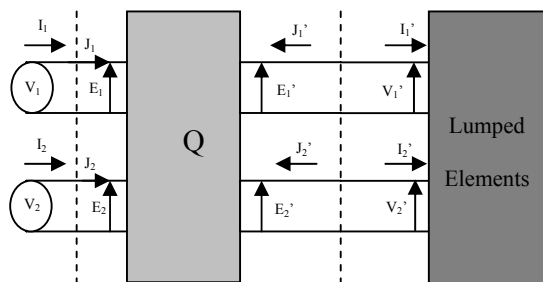


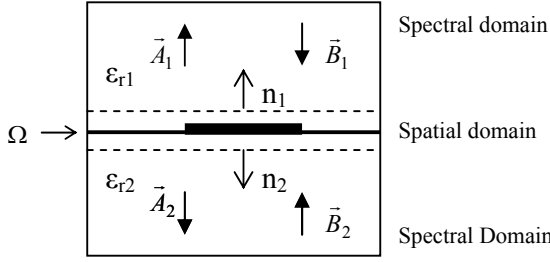
Fig. 2 Interaction between principals and auxiliaries sources

III. ITERATIVE METHOD

A brief overview of the iterative method [7] based on wave concept is presented here. It consists of generating a recursive relationship between a given incident and reflected waves generated from the discontinuity planes (equations 1). The analysis structure shown in figure 3 is composed of planar microstrip enclosed in the metal box; the interface Ω is divided into cells which form sub-domains corresponding to metal, dielectric, and sources.

¹ Laboratoire d'électronique, Faculté des Sciences de Tunis, 2092 El manar II, Tunisie, Email : zied.harouni@gmail.com

² E.N.S.E.E.H.T. Laboratoire d'électricité, groupement de recherche en électromagnétisme, 2 rue Charles Camichel B.P. 7122, 31071 Toulouse Cdx7, France.

Fig. 3 Illustration of waves on both sides of the interface Ω

$$\begin{aligned}\vec{A}_i^n &= \hat{\Gamma}_\Omega \cdot \vec{B}_i^n + \vec{A}_i^0 \\ \vec{B}_i^n &= \hat{\Gamma}_i \cdot \vec{A}_i^{n-1}\end{aligned}\quad (1)$$

The wave concept is introduced by writing the tangential electric field E , (on Ω) and surface tangential current density J , (on Ω) in terms of incident and reflected waves.

$$\begin{aligned}A_i &= \frac{1}{2\sqrt{z_{oi}}} (E_i + Z_{oi} J_i) \\ B_i &= \frac{1}{2\sqrt{z_{oi}}} (E_i - Z_{oi} J_i)\end{aligned}\quad (2)$$

Where J_i is the surface tangential current density which is defined as: $\vec{J}_i = \vec{H}_i \wedge \vec{n}_i$; n_i is a unit vector normal to Ω . A_i and B_i are two tangential vectors associated with the discontinuity interface Ω . Z_{oi} is the characteristic impedance of region i (equation 1):

$$Z_{oi} = \sqrt{\frac{\mu_i}{\epsilon_i}} \quad (3)$$

ϵ_i , μ_i are respectively the permittivity and permeability of region i . E_i , H_i are the tangential electric and magnetic field on Ω . The interface Ω is characterized by a scattering operation matrix [7] depending on boundary conditions defined for each point of Ω . The continuity conditions for fields in each point of Ω (spatial domain) are:

$$\begin{aligned}E_1 &= E_2 = 0 && \text{on the metal domain.} \\ E_1 &= E_2 \text{ and } J_1 + J_2 = 0 && \text{on the dielectric domain.} \\ E_1 &= E_2 = E_0 && \text{on the source domain}\end{aligned}$$

A. Electromagnetic model of the studied structure

The studied circuit will be placed in a cavity with metal walls for reasons of shielding and modelling.

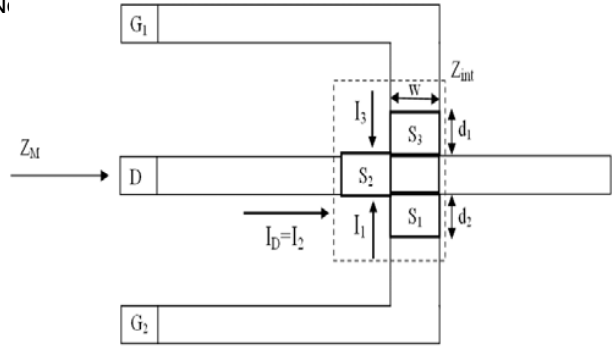


Fig. 4 The studied structure of the Dual gate MESFET transistor

B. Application of the iterative method with auxiliary source

In transistor case, we can admit that the dimensions are sufficiently small; we choose a simple design (figures 5) containing the electrodes drain and two gates as well as three auxiliary sources. For instance, the three auxiliary sources express the electromagnetic coupling between electrodes of transistor which corresponds to the intrinsic part;

$$\begin{pmatrix} J_1 \\ J_2 \\ J_3 \end{pmatrix} = \begin{pmatrix} Y_{11 \text{ int a}} & Y_{12 \text{ int a}} & Y_{13 \text{ int a}} \\ Y_{21 \text{ int a}} & Y_{22 \text{ int a}} & Y_{23 \text{ int a}} \\ Y_{31 \text{ int a}} & Y_{32 \text{ int a}} & Y_{33 \text{ int a}} \end{pmatrix} \begin{pmatrix} E_1 \\ E_2 \\ E_3 \end{pmatrix} \quad (4)$$

The intrinsic admittance of transistor is given by the following relation:

$$\begin{pmatrix} I_{G1S} \\ I_{G2S} \\ I_{DS} \end{pmatrix} = \begin{pmatrix} Y_{11 \text{ int}} & Y_{12 \text{ int}} & Y_{13 \text{ int}} \\ Y_{21 \text{ int}} & Y_{22 \text{ int}} & Y_{23 \text{ int}} \\ Y_{31 \text{ int}} & Y_{32 \text{ int}} & Y_{33 \text{ int}} \end{pmatrix} \begin{pmatrix} V_{G1S} \\ V_{G2S} \\ V_{DS} \end{pmatrix} \quad (5)$$

- I_{G1S} , I_{G2S} , I_{DS} : Current respectively on gate 1, gate 2 and drain.
- V_{G1S} , V_{G2S} , V_{DS} : Voltage respectively on gate 1, gate 2 and drain.

According to figures 5, the various current and voltage in the different electrodes of the transistor takes the following expressions:

$$\begin{cases} V_{G1S} = E_{G1S} d_3 = E_3 d_3 \\ V_{G2S} = E_{G2S} d = E_1 d_1 \end{cases} \quad (6)$$

$$\begin{cases} I_{G1S} = I_3 = J_3 w \\ I_{G2S} = I_1 = J_1 w \end{cases} \quad (7)$$

$$\begin{cases} V_{DS} = E_{DS} d_2 = E_2 d_2 \\ I_{DS} = I_2 = J_2 w \end{cases} \quad (8)$$

- J_1 , J_2 , and J_3 : Density of current on the three auxiliary sources respectively: S_1 , S_2 and S_3 .
- E_1 , E_2 , and E_3 : Electric field on the three auxiliary sources respectively: S_1 , S_2 and S_3 .

Using equations (5), (6), (7) and matrix (B), the matrix (A) becomes:

$$\begin{pmatrix} J_1 \\ J_2 \\ J_3 \end{pmatrix} = \begin{pmatrix} \frac{d_1}{w} Y_{22nt} & \frac{d_2}{w} Y_{23nt} & \frac{d_3}{w} Y_{21nt} \\ \frac{d_1}{w} Y_{32nt} & \frac{d_2}{w} Y_{33nt} & \frac{d_3}{w} Y_{31nt} \\ \frac{d_1}{w} Y_{12nt} & \frac{d_2}{w} Y_{13nt} & \frac{d_3}{w} Y_{11nt} \end{pmatrix} \begin{pmatrix} E_1 \\ E_2 \\ E_3 \end{pmatrix}$$

From matrix (A):

$$\begin{cases} J_1 = Y_{11int} E_1 + Y_{12int} E_2 + Y_{13int} E_3 \\ J_2 = Y_{21int} E_1 + Y_{22int} E_2 + Y_{23int} E_3 \\ J_3 = Y_{31int} E_1 + Y_{32int} E_2 + Y_{33int} E_3 \end{cases}$$

From equations (d), (e) and (f), we calculate E_1 , E_2 and E_3 as function of E_D , E_{G1} and E_{G2}

$$\begin{cases} E_1 = K_1 E_{G1} + K_2 E_{G2} + K_3 E_D \\ E_2 = K'_1 E_{G1} + K'_2 E_{G2} + K'_3 E_D \\ E_3 = K''_1 E_{G1} + K''_2 E_{G2} + K''_3 E_D \end{cases}$$

Are calculated and not mentioned in this paper. We replace the expressions of E_1 , E_2 and E_3 in equations (a), (b) and (c).

$K_i, K'_i, K''_i \quad i = 1, 2, 3 :$

$$\begin{cases} J_{G1} = (Y_{G1G1} + Y_{G1G2} + Y_{G1D} + Y_{G1G3} K'_1) E_{G1} + (Y_{G1G2} + Y_{G1G3} K'_2 + Y_{G1D} + Y_{G1G3} K'_3) E_{G2} + (Y_{G1D} + Y_{G1G3} K'_3) E_D \\ J_{G2} = (Y_{G2G1} + Y_{G2G2} + Y_{G2D} + Y_{G2G3} K'_1) E_{G1} + (Y_{G2G2} + Y_{G2G3} K'_2 + Y_{G2D} + Y_{G2G3} K'_3) E_{G2} + (Y_{G2D} + Y_{G2G3} K'_3) E_D \\ J_D = (Y_{DG1} + Y_{DG2} + Y_{DG3} K'_1) E_{G1} + (Y_{DG2} + Y_{DG3} K'_2 + Y_{DG3} K'_3) E_{G2} + (Y_{DG3} K'_3) E_D \end{cases}$$

Y_{tr} , are then:

$$\begin{bmatrix} J_{G1} \\ J_{G2} \\ J_D \end{bmatrix} = \begin{bmatrix} Y_{11tr} & Y_{12tr} & Y_{13tr} \\ Y_{21tr} & Y_{22tr} & Y_{23tr} \\ Y_{31tr} & Y_{32tr} & Y_{33tr} \end{bmatrix} \begin{bmatrix} E_{G1} \\ E_{G2} \\ E_D \end{bmatrix}$$

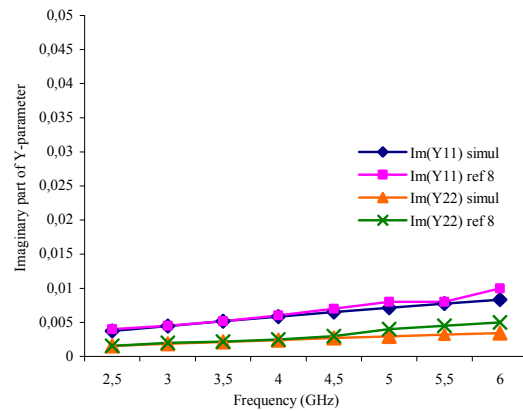
Where,

$$Y_{tr} = \begin{bmatrix} Y_{G1G1} + Y_{G1G2} + Y_{G1D} + Y_{G1G3} K'_1 & Y_{G1G2} + Y_{G1G3} K'_2 + Y_{G1D} + Y_{G1G3} K'_3 & Y_{G1D} + Y_{G1G3} K'_3 \\ Y_{G2G1} + Y_{G2G2} + Y_{G2D} + Y_{G2G3} K'_1 & Y_{G2G2} + Y_{G2G3} K'_2 + Y_{G2D} + Y_{G2G3} K'_3 & Y_{G2D} + Y_{G2G3} K'_3 \\ Y_{DG1} + Y_{DG2} + Y_{DG3} K'_1 & Y_{DG2} + Y_{DG3} K'_2 + Y_{DG3} K'_3 & Y_{DG3} K'_3 \end{bmatrix}$$

($Y_{DD}, Y_{G1G1}, Y_{G1G2}, Y_{G1D}, \dots$) are the admittances which express the coupling admittance between various sources of the structure, they are determined using the iterative method.

IV. VALIDATION OF THE ANALYSIS METHOD

We validated our method by comparing our results with those published in [8]; the figure 8 {a, b} shows that they are similar. The disposition of different electrodes of transistor layout given in figure 4 is based on the equivalent circuit. A FORTRAN program is elaborate to model the dual gate transistor introducing the auxiliary source technique and the iterative method.



(a)

C. Intrinsic Y parameters of DGMESFET

The equivalent circuit of a dual-gate MESFET is essential in the design of microwave circuits. The DGMESFET small-signal and large-signal models have been proposed by many authors [8]. In general, a DGMESFET is basically modelled as a cascade circuit of two single-gate MESFET's (SGMESFET). The typical small-signal equivalent circuit of a coplanar DGMESFET, as shown in figure 7, contains two intrinsic FET's and extrinsic elements with a total of about 27 elements and the intrinsic parameters of the two transistors are given in table 1.

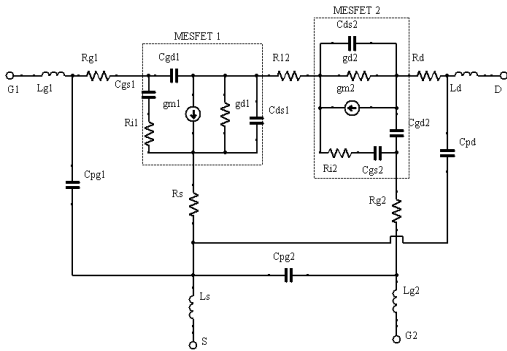


Fig. 5 A small-signal equivalent circuit of Dual gate MESFET

TABLE I VALUES OF INTRINSIC PARAMETERS OF THE TWO TRANSISTORS

MESFET 1		MESFET 2	
Parameters	Values	Parameters	Values
C_{gs1}	0.2 pF	C_{gs2}	0.29 pF
R_{i1}	7 Ω	R_{i2}	10 Ω
g_{m10}	0.058 AV^{-1}	g_{m20}	0.03 AV^{-1}
t_1	7.6 ps	t_2	8.04 ps
C_{gd1}	63 fF	C_{gd2}	68 fF
g_{d1}	10 mS	g_{d2}	5.88 mS
C_{ds1}	0.15 pF	C_{ds2}	0.034 pF

D. Transistor admittance

Using the iterative method we determine the expressions of the density of current according to electric field for each source:

$$J_{G1} = Y_{G1G1} E_{G1} + Y_{G1G2} E_{G2} + Y_{G1D} E_D + Y_{G1G3} E_1 + Y_{G1G2} E_2 + Y_{G1G3} E_3 \quad (a)$$

$$J_{G2} = Y_{G2G1} E_{G1} + Y_{G2G2} E_{G2} + Y_{G2D} E_D + Y_{G2G3} E_1 + Y_{G2G2} E_2 + Y_{G2G3} E_3 \quad (b)$$

$$J_D = Y_{DG1} E_{G1} + Y_{DG2} E_{G2} + Y_{DG3} E_D + Y_{DG1} E_1 + Y_{DG2} E_2 + Y_{DG3} E_3 \quad (c)$$

$$J_1 = Y_{1D} E_D + Y_{11} E_1 + Y_{12} E_2 + Y_{13} E_3 + Y_{1G1} E_{G1} + Y_{1G2} E_{G2} \quad (d)$$

$$J_2 = Y_{2D} E_D + Y_{21} E_1 + Y_{22} E_2 + Y_{23} E_3 + Y_{2G1} E_{G1} + Y_{2G2} E_{G2} \quad (e)$$

$$J_3 = Y_{3D} E_D + Y_{31} E_1 + Y_{32} E_2 + Y_{33} E_3 + Y_{3G1} E_{G1} + Y_{3G2} E_{G2} \quad (f)$$

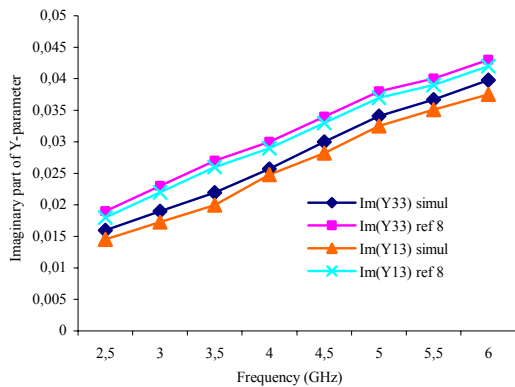


Fig. 6 (a), (b): Imaginary part of three-port Y-matrix

We note that our DGMESFET have $1\mu\text{m}$ gate length and, we can observe in figure 9, that DGMESFET's gain is higher than the simple MESFET. The difference between the two curves is about 4 dB.

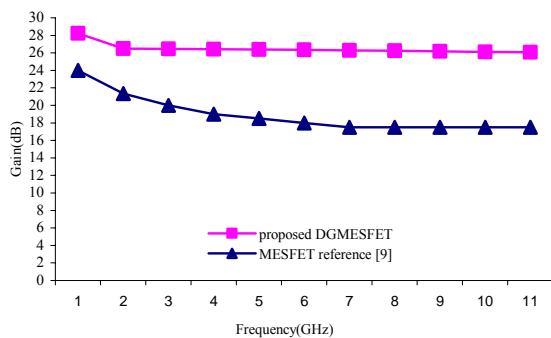


Fig. 7 Gain of DGMESFET and MESFET as function of frequency

V. CONCLUSIONS

An efficient method has been presented and used to simulate the insertion of any lumped passive or active, linear or nonlinear component into a distributed microwave structure. This calculation was made only once for a passive or active linear or no-linear component and it could be changed without any influence on the final result. In order to validate our work the gain and the imaginary part of three Y matrixes are determined. The comparison of the results shows a good agreement with those published.

Based on the use of an iterative method using localised auxiliary sources to model the intrinsic part of the transistor, in conjunction with the F.M.T (Fast Modal Transformation), our proposed technique is validated through the presentation of test case, in which Dual gate MESFET is included. The good agreement between simulation results and experimental data prove its adaptability for the analysis of microwave circuits including lumped elements.

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