International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:2, No:5, 2008

A Novel Zero Voltage Transition Synchronous Buck Converter for Portable Application

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***Abstract*—**This paper proposes a zero-voltage transition (ZVT) PWM synchronous buck converter, which is designed to operate at low output voltage and high efficiency typically required for portable systems. To make the DC-DC converter efficient at lower voltage, synchronous converter is an obvious choice because of lower conduction loss in the diode. The high-side MOSFET is dominated by the switching losses and it is eliminated by the soft switching technique. Additionally, the resonant auxiliary circuit designed is also devoid of the switching losses. The suggested procedure ensures an efficient converter. Theoretical analysis, computer simulation, and experimental results are presented to explain the proposed schemes.

***Keywords*—**DC-DC Converter, Switching loss, Synchronous Buck, Soft switching, ZVT.

I. INTRODUCTION

THE next generation of portable products, such as personal communicators and digital assistants, has demanded improvement in dc-dc converter topology in order to increase battery life time and enable smaller, cheaper systems. Since many portable devices operate in low-power standby modes for a majority of the time they are on, increasing light-load converter efficiency can significantly increase battery lifetime. A key element in this task, especially at low output voltages that future microprocessor and memory chips will need, is the synchronous rectifier. The synchronous rectifier buck converter is popular for low-voltage power conversion because of its high efficiency and reduced area consumption [3], [9], [12], [21], and [25]. A synchronous rectifier is an electronic switch that improves power-conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. MOSFETs usually serve this purpose.

However, higher input voltages and lower output voltages have brought about very low duty cycles, increasing switching losses and decreasing conversion efficiency. So in this paper, we have optimized the efficiency of the synchronous buck converter by eliminating switching losses using soft switching technique**.**

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The voltage-mode soft-switching method that has attracted most interest in recent years is the zero voltage transition [1], [2], [4]-[8], [10], [11], [13]-[20], [22]-[24], [26]-[27], [29]. This is because of its low additional conduction losses and because its operation is closest to the PWM converters. The auxiliary circuit of the ZVT converters is activated just before the main switch is turned on and ceases after it is accomplished. The auxiliary circuit components in this circuit have lower ratings than those in the main power circuit because the auxiliary circuit is active for only a fraction of the switching cycle; this allows a device that can turn on with fewer switching losses than the main switch to be used as the auxiliary switch. The improvement in efficiency caused by the auxiliary circuit is mainly due to the difference in switching losses between the auxiliary switch and the main power switch if it were to operate without the help of the auxiliary circuit. Previously proposed ZVT-PWM converters have at least one of the following key drawbacks.

1) The auxiliary switch is turned off while it is conducting current. This causes switching losses and EMI to appear that offsets the benefits of the using the auxiliary circuit. In converters such as the ones proposed in [2], [10], [14] and [15] the turn off is very hard.
2) The auxiliary circuit causes the main converter switch to operate with a higher peak current stress and with more circulating current. This results in the need for a higher current-rated device for the main switch, and an increase in conduction losses. The converters proposed in [3], [6], [8], [11], [12], and [16] the current stresses are very high on the main switch.
3) The auxiliary circuit components have high voltage and/or current stresses. Such as converters proposed in [1], [5], [6] and [13], [16]. The converter proposed in [23] and [28] reduces the current stress on the main switch, but circuit is very complex.

Reducing switching losses for low power circuit such as synchronous buck is not known to be present in the literatures [1]-[24] and [26]-[29]. The converter shown in Fig.1 is designed for a low voltage, high current circuit and found to be highly efficient. Hence, this paper presents a new class of ZVT synchronous buck converter. By using a resonant auxiliary network in parallel with the main switch, the proposed converters achieve zero-voltage switching for the main switch and synchronous switch and zero-current switching for the auxiliary switch without increasing their voltage and current stresses.

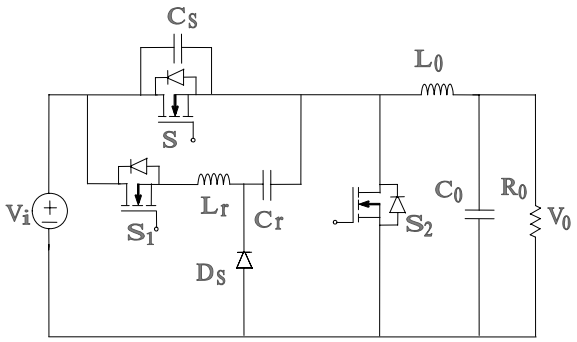

Fig. 1 The proposed converter

The paper is organized as follows: The next section gives a short description of the proposed circuit followed by review of the various modes of operation with their key waveforms and the representation of their equivalent operation modes. Section III presents the design considerations and section IV includes basic features of converter. Section V includes simulation and experimental results to illustrate the features of the proposed converter scheme. Section VI includes some conclusions.

II. OPERATION PRINCIPLES AND ANALYSIS

A. Definitions and Assumptions

The circuit scheme of the proposed new ZVT synchronous buck converter is shown in Fig.1. The auxiliary circuit consists of switch S_1, resonant capacitor Cr, Resonant inductor L_r. The auxiliary circuit operates only during a short switching-transition time to create ZVS condition for the main switch. The body diode of the main switch is also utilized in the converter. A high frequency schottky diode D_S is used for discharging the capacitor voltage to the output, which happens before the turn on of the synchronous switch. During one switching cycle, the following assumptions are made in order to simplify the steady-state analysis of the circuit shown in Fig.1.

1. Input Voltage V_i is constant.
2. Output Voltage V_0 is constant or output capacitor C_0 is large enough.
3. Output current I_0 is constant or output inductor L_0 is large enough.
4. Output Inductor L_0 is much larger than resonant circuit inductor L_r.
5. Resonant circuits are ideal.
6. Semiconductor devices are ideal.
7. Reverse recovery time of all diodes is ignored.

B. Modes of Operation

Eight stages take place in the steady-state operation during one switching cycle in the proposed converter. The key waveforms of these stages are given in Fig.2 and the equivalent circuit schemes of the operation stages are given in Fig.3. The detailed analysis of every stage is presented below:

Mode 1 (t_0, t_1): Prior to $t = t_0$, the body diode of S_2 was conducting; main switch S and auxiliary switch S_1 are turned-off. At t_0, the auxiliary switch S_1 is turned on which realizes zero-current turn-on as it is in series with the resonant inductor L_r. The current through resonant inductor L_r and resonant capacitor C_r rise at the same rate as falls of current through i_{S2}. Resonance occurs between L_r and C_r during this mode. The mode ends at $t = t_1$, when i_{Lr} reaches I_0 and i_{S2} falls to zero in result the body diode of S_2 stops conducting. The voltage and current expressions which govern this circuit mode are given by:

$$i_{S2} = I_0 - i_{Lr} \tag{1}$$

$$i_{Lr}(t - t_0) = \frac{V_i}{Z} Sin\omega(t - t_0) \tag{2}$$

$$\omega = \frac{1}{\sqrt{L_r C_r}} = \text{Resonant frequency}$$

$$Z = \sqrt{L_r / C_r} = \text{Characteristic impedance}$$

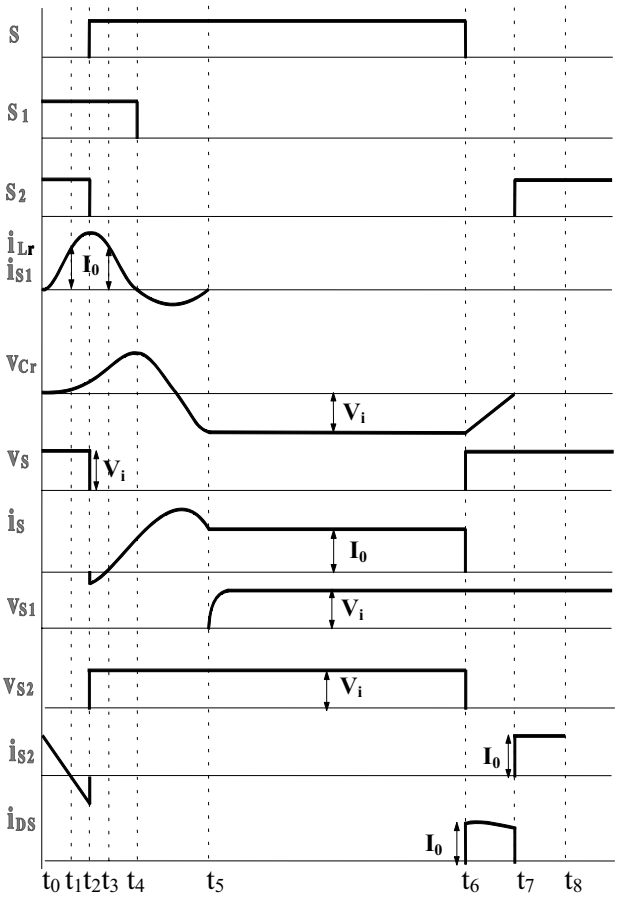

Fig. 2 Key theoretical waveforms concerning the operation stages in the proposed converter

At $t = t_1$

$$t_{01} = t_1 - t_0 = \frac{1}{\omega} Sin^{-1}\left(\frac{I_0 Z_i}{V_i}\right) \tag{3}$$

$$V_{Cr}(t_1 - t_0) = V_{Cr1} \tag{4}$$

$$i_{Lr}(t_1 - t_0) = I_0 \quad (5)$$

Mode 2 (t_1, t_2): L_r and C_r continue to resonate. At t_1, the synchronous switch S_2 is turned on under ZVS. This mode is made to end by turning off the switch S_2 under ZVS, when i_{Lr} current reaches to it maximum value i.e. i_{Lrmax}.

$$i_{S2} = i_{Lr} - I_0 \quad (6)$$

$$i_{Lr}(t - t_1) = \frac{V_i - V_{Cr1}}{Z} Sin\omega(t - t_1) + I_0 Cos\omega(t - t_1) \quad (7)$$

At $t = t_2$

$$i_{Lr}(t_2 - t_1) = I_{Lr\max} \quad (8)$$

$$t_{12} = \frac{1}{\omega}\tan^{-1}\left(\frac{V_i - V_{Cr1}}{I_0 Z}\right) \quad (9)$$

$$V_{Cr}(t_2 - t_1) = V_{Cr2} \quad (10)$$

Mode 3 (t_2, t_3): At t_2, i_{Lr} reaches its peak value i_{Lrmax}. Since i_{Lr} is more than load current I_0, the capacitor C_S will be charged and discharge through body diode of main switch S, which leads to conduction of body diode. This mode ends when resonant current i_{Lr} falls to load current I_0. So current through body diode of main switch S becomes zero which results turned off of body diode. At the same time the main switch S is turned on under ZVS. The voltage and current expressions for this mode are:

$$i_{Lr}(t - t_2) = -\frac{V_{Cr2}}{Z} Sin\omega(t - t_2) + I_{Lr\max} Cos\omega(t - t_2) \quad (11)$$

$$t_{23} = \frac{1}{\omega}\left[\tan^{-1}\left(\frac{I_{Lr\max} Z}{V_{Cr2}}\right) - Sin^{-1}(I_0)\right] \quad (12)$$

At $t = t_3$

$$i_{Lr}(t_{23}) = I_0 \quad (13)$$

$$V_{Cr}(t_{23}) = V_{Cr3} \quad (14)$$

Mode 4 (t_3 t_4): At t_3, the main switch is turned-on with ZVS. During this stage the growth rate of i_S, is determined by the resonance between L_r and C_r. The resonant process continues in this mode and the current i_{Lr} continue to decrease. This mode ends when i_{Lr} falls to zero and S_1 can be turned-off with ZCS. The voltage and current expressions for this mode are:

$$i_{Lr}(t - t_3) = -\frac{V_{Cr3}}{Z} Sin\omega(t - t_3) + I_0 Cos\omega(t - t_3) \quad (15)$$

At $t = t_4$

$$i_{Lr} = 0 \quad (16)$$

$$t_{34} = \tan^{-1}\left(\frac{I_0 Z}{V_{Cr3}}\right) \quad (17)$$

$$V_{Cr}(t_4) = V_{Cr\max} \quad (18)$$

Mode 5 (t_4 t_5): At t_4, the auxiliary switch S_1 is turned-off with ZCS. The body diode of S_1 begins to conduct due to resonant capacitor C_r which starts to discharge. The resonant current i_{Lr} rises in the reverse direction, reaches a maximum negative and increases to zero. At this moment the body diode of S_1 is turned off and the mode ends. The voltage and current equations for this mode are given by:

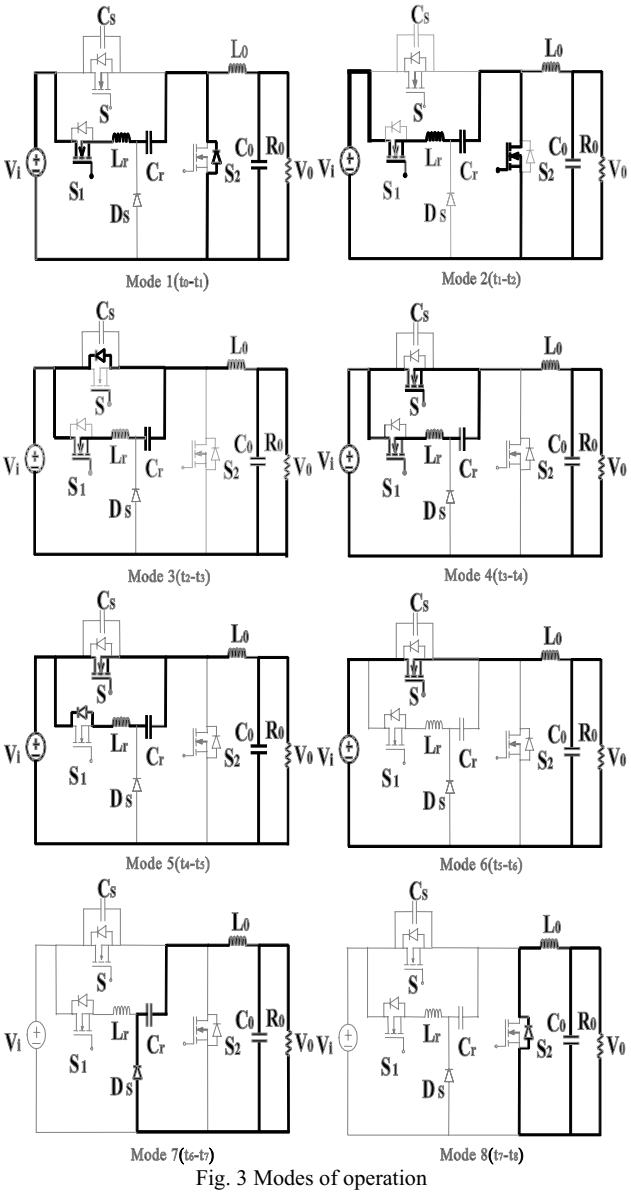

Fig. 3 Modes of operation

$$i_{Lr}(t - t_4) = \frac{V_{Cr\max}}{Z} Sin\omega(t - t_4) \quad (19)$$

At $t = t_5$

$$i_{Lr}(t_5) = 0 \quad (20)$$

$$t_{45} = \frac{\pi}{\omega} \quad (21)$$

$$V_{Cr}(t_5) = -V_{Cr4} \quad (22)$$

Mode 6 (t_5, t_6): Since the body diode of S_1 has turned off at t_5, now only the main switch S carries the load current. There is no resonance in this mode and the circuit operation is

identical to a conventional PWM buck converter. The voltage and current equations for this mode are given by:

$$i_S = I_0 \tag{23}$$

$$i_{Lr}(t_6) = 0 \tag{24}$$

$$V_{Cr}(t_6) = -V_{Cr4} \tag{25}$$

Mode 7 (t_6, t_7): At t_6, the main switch S is turned off with ZVS. The schottky diode D starts conducting. The resonant energy stored in the capacitor Cr starts discharging to the load through the high frequency schottky diode D_S for a very short period of time, hence body – diode conduction losses and drop in output voltage is too low. This mode finishes when Cr is fully discharged. The equations that define this mode are given by:

$$V_{Cr}(t - t_6) = -V_{Cr4} + \frac{I_0}{C_r}(t - t_6) \tag{26}$$

At $t = t_7$

$$V_{Cr}(t_7) = 0 \tag{27}$$

$$t_{67} = \frac{C_r V_{Cr4}}{I_0} \tag{28}$$

Mode 8 (t_7, t_8): At t_7, the body diode of switch S_2 is on as soon as Cr is fully discharged and schottky diode is turned off under ZVS. Dead time loss is negligibly small compared to the conventional synchronous buck converter. During this mode, the converter operates like a conventional PWM buck converter until the switch S_1 is turned on in the next switching cycle. The equation that defines this mode is given by:

$$i_{S2} = I_o \tag{29}$$

III. DESIGN PROCEDURE

Design of conventional PWM converters has been well presented in literatures. Thus it is more significant to focus on design procedures of the auxiliary circuit. The resonant inductor, resonant capacitor, and the delay time of the auxiliary switch are the most important components when designing the auxiliary circuit. The proposed auxiliary resonant circuit provides soft switching conditions for the main transistor. The following design procedure is developed considering procedures such as those presented previously [20].

A. Delay time

The on time of auxiliary switch (S_1) must be shorter than one tenth of the switching period.

$$T_D = \frac{1}{10} T_S \tag{30}$$

B. Current Stress Factor (a)

The current stress factor of the auxiliary switch is defined as

$$a = \frac{I_{Lrm}}{I_{in(\max)}} \tag{31}$$

It is greater than one $(1 \le a \le 1.5)$ and is desired to be as small as possible. This factor can be used for the selection of the auxiliary switch.

C. Resonant Capacitor (C_r)

The resonant capacitor can be expressed as

$$C_r = \frac{(a-1)^2 I_{in(\max)} T_D}{V_o\left[1 + \frac{\pi}{2}(a-1)\right]} \tag{32}$$

D. Resonant Inductor (L_r)

The resonant inductor is given by

$$L_r = \frac{V_o T_D}{I_{in(\max)}\left[1 + \frac{\pi}{2}(a-1)\right]} \tag{33}$$

E. MOSFET Selection

A method to choose the MOSFETs for the converter is to compare the power dissipation values for a number of different MOSFET types. Usually, a low on-state drain resistance MOSFET is chosen for the synchronous rectifier, and a MOSFET with a low gate charge is chosen for the switches.

IV. BASIC CONVERTER FEATURES

The features of the proposed soft switching converter are briefly summarized as follows.

1. All of the active and passive semiconductor devices are turned on and off under exact ZVS and/or ZCS.
2. The proposed converter has a simple structure, low cost, and ease of control.
3. The converter acts as a conventional PWM converter during most of the switching cycle.
4. The presented snubber cell can be easily applied to the other basic PWM dc-dc converters and to all switching converters.
5. The proposed converter has a larger total efficiency and a wider load range.
6. The main switch and the auxiliary switch are not subjected to additional voltage stresses. Current stress on the main switch is slightly higher, but current stress on the auxiliary switch is within safe limit.

V. SIMULATION AND EXPERIMENTAL RESULTS

A Prototype of the proposed converter, as shown in Fig.1 has been built in the laboratory. The newly proposed converter operates with an input voltage Vs = 12V, output voltage Vo = 3.3V, load current of 10A and a switching frequency of 200 kHz. The converter is simulated using simulation software PSIM version 6.0. The major parameters and components are given in Table I.

TABLEI COMPONENTS USED IN THE PROPOSED CONVERTER

Component	Value/Model	
	Simulation	Experiment
Main Switch, S	Ideal	IRF1312
Auxiliary Switch, S1	Ideal	IRF1010E
Synchronous Switch, S2	Ideal	IRF1010E
Schottky Diode, D	Ideal	MBR60L45CTG
Capacitance, CS	0.05nH	0.05nH
Resonant Inductor, Lr	200nH	200nH
Resonant Capacitor, Cr	0.2μF	0.2μF
Output Capacitor, Co	100μF	100μF
Output Inductor, Lo	2μH	2μH

Figs. 4 (a-d) show the simulation results of the proposed converter and Figs. 5 (a-d) present the experimental results. All the waveforms except the efficiency curve represents a time period of one switching cycle, which is 5μs in this case. The amplitudes are denoted below each of their waveforms respectively.

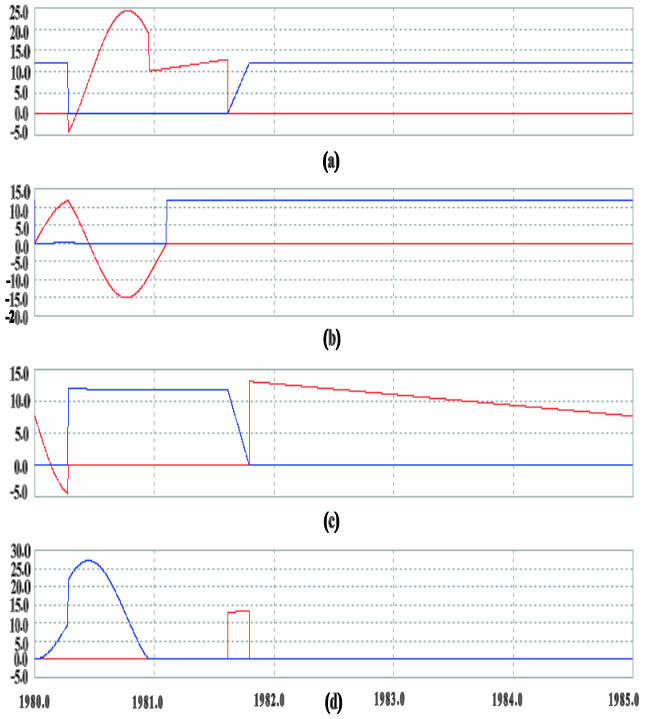

Fig. 4 Simulated voltage and current waveforms: (a) main switch S: VS; IS, (b) auxiliary switch S1: VS1; IS1, (c) synchronous switch S2: VS2; IS2, (d) schottky diode DS: VDS; IDS.

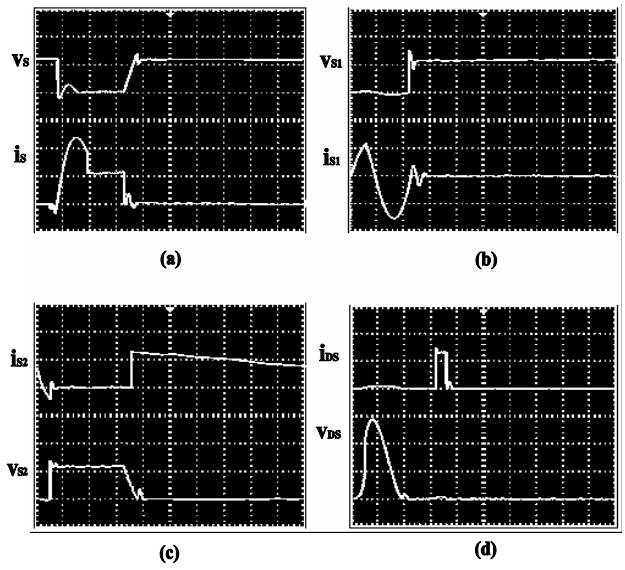

Fig. 5 Experimental voltage and current waveforms: (a) main switch S: V_S; I_S: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div), (b) auxiliary switch S_1: V_{S1}; I_{S1}: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div), (c) synchronous switch S_2: V_{S2}; I_{S2}: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div), (d) schottky diode D: V_D; I_D: (V: 10 V/div, I: 10 A/div, time: 0. 5 μs/div).

A. Main Switch S

It is noted from the Figs. (4a & 5a) that the main switch S is turned on under ZVS, when voltage across Cs is zero. The converter has not exceeded the voltage limits; however the current stress is slightly higher for a very short period of time. The main switch also switches off under ZVS. The current and voltage wave shape are identical to theoretical waveforms.

B. Auxiliary Switch S_1

It is noted from the Figs. (4b & 5b) that auxiliary switch S_1 also operates with the soft switching. The switch S_1 is turned on under ZCS because of the inductor L_r and turns off under ZCS when resonant current through L_r and C_r falls to zero. Its body diode also turns on as soon as S_1 is off at zero current and turns off when the resonant current is zero. The shapes of the figures are identified to confine much with the theoretical waveforms. The auxiliary switch is active only for a short period of time, which is verified by its conduction period and it is too small. Also the current and voltage stresses are well within the operating limits.

C. Synchronous switch S_2

The synchronous switch is turned on under ZVS when C_r has completely discharged and also turns off under ZVS, which can be observed from Figs. (4c & 5c). The synchronous switch also has characteristics similar to the switches S, S_1. They operate within the safe limits and it can be noted here, the conduction period of S_2 is more confining to the design values and it operates at a low power when compared to the other switches.

D. Schottky Diode D

The schottky diode works for a very short period to discharge the resonant capacitor Cr as can be observed from Figs. (4d & 5d). The schottky diode also turned-on and turned-off under ZVS. A high-frequency schottky diode which is available at high-current, low voltages can be used. The conduction of schottky diodes may cause a considerable drop in output voltage for low power circuits but due to the advancement in semiconductor techniques, schottky diodes are also now available with a low forward voltage drop for high frequency circuits.

E. Efficiency curve

From Fig.6 it can be observed that the efficiency values of the soft switching converter are relatively high with respect to those of the hard switching converter. The efficiency values towards the minimum output power decrease naturally because the converter is designed for the maximum output current. At 70% output power, the overall efficiency of the proposed converter increases to about 97% from the value of 92% in its counterpart hard switching converter. The high efficiency concludes the correctness of the design values.

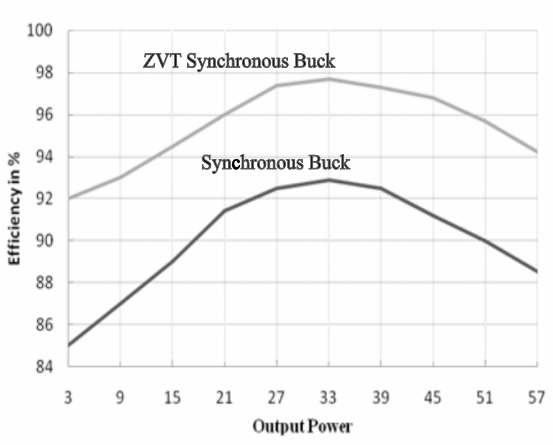

Fig. 6 Converter efficiency versus output power

VI. Conclusion

The concepts of ZVT used in high power were implemented in synchronous buck converter and it was shown that the switching losses in synchronous buck were eliminated. Besides the main switch ZVS turned-on and turned-off, the auxiliary switch ZCS turned-on and turned-off, the synchronous switch also turned-on and turned-off under ZVS. Hence switching losses are reduced and the newly proposed ZVT synchronous buck is highly efficient than the conventional converter. The additional voltage and current stresses on the main devices do not take place, and the auxiliary devices are subjected to allowable voltage and current values. Moreover, the converter has a simple structure, low cost and ease of control. A prototype of a 3.3V, 10A, 200 kHz system was implemented to experimentally verify the improved performance.

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