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Efficient Hardware Realization of Truncated Multipliers using FPGA

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***Abstract*—**Truncated multiplier is a good candidate for digital signal processing (DSP) applications including finite impulse response (FIR) and discrete cosine transform (DCT). Through truncated multiplier a significant reduction in Field Programmable Gate Array (FPGA) resources can be achieved. This paper presents for the first time a comparison of resource utilization of Spartan-3AN and Virtex-5 implementation of standard and truncated multipliers using Very High Speed Integrated Circuit Hardware Description Language (VHDL). The Virtex-5 FPGA shows significant improvement as compared to Spartan-3AN FPGA device. The Virtex-5 FPGA device shows better performance with a percentage ratio of number of occupied slices for standard to truncated multipliers is increased from 40% to 73.86% as compared to Spartan-3AN is decreased from 68.75% to 58.78%. Results show that the anomaly in Spartan-3AN FPGA device average connection and maximum pin delay have been efficiently reduced in Virtex-5 FPGA device.

***Keywords*—**Digital Signal Processing (DSP), Field Programmable Gate Array (FPGA), Spartan-3AN, Truncated Multiplier, Virtex-5, VHDL.

I. Introduction

MULTIPLICATION is a computation intensive and the core operation in many algorithms used in scientific computations. The computational complexity of algorithms used in digital signal processing (DSP) has gradually increased. As a result fast and efficient parallel multipliers are required for general purpose digital signal processors (DSPs) as well as application specific architectures for DSP.

In particular, if the processing has to be performed under real time conditions, such algorithms have to deal with high throughput rates. In many cases implementation of DSP algorithm demands using application specific integrated circuits (ASICs). This is especially required for image processing applications. Since development costs for ASICs are high, algorithms should be verified and optimized before implementation.

However, with recent advancements in very large scale integration (VLSI) technology, hardware implementation has become a desirable alternative. Significant speedup in computation time can be achieved by assigning computation intensive tasks to hardware and by exploiting the parallelism in algorithms. Recently, field programmable gate arrays (FPGAs) have emerged as a platform of choice for efficient hardware implementation of computation intensive algorithms. [1]. FPGAs enable a high degree of parallelism and can achieve orders of magnitude speedup over general purpose processors (GPPs). This is a result of increasing embedded resources available on FPGA. FPGA have the benefit of hardware speed and the flexibility of software. The three main factors that play an important role in FPGA based design are the targeted FPGA architecture, electronic design automation (EDA) tools and design techniques employed at the algorithmic level using hardware description languages. In FPGAs, the choice of the optimum multiplier involves three key factors: area, propagation delay and reconfiguration time. Therefore, FPGA has become viable technology and an attractive alternative to ASICs [1]-[2].

Multiplication and squaring functions are used extensively in applications such as DSP, image processing and multimedia [3]-[4]. A full width digital $n \times n$ multiplier computes the $2n$ output as a weighted sum of partial products [5]. If the product is truncated to n-bits, the least-significant columns of the product matrix contribute little to the final result. To take advantage of this, truncated multipliers and squarers do not form all of the least-significant columns in the partial-product matrix [6]-[7]. As more columns are eliminated, the area and power consumption of the arithmetic unit are significantly reduced, and in many cases the delay also decreases. The trade-off is that truncating the multiplier matrix introduces additional error into the computation.

Other applications, which require not only a significant number of multiplication and squaring functions but also large integers, are found in the cryptography domain [8]. Achieving efficient realization of the multiplication may have a significant impact on the specific applications in terms of speed, power dissipation and area. Many research efforts have been presented in literature to achieve hardware efficient implementation of a truncated multiplier. The basic idea of these techniques is to discard some of the less significant partial products and to introduce a compensation circuit that partly compensates for the dropped terms, thereby reducing approximation error [9]-[16]. Garofalo et al [17] presented a truncated multiplier with minimum square error for every inputs' bit width. Truncated multiplication provides an efficient method for reducing the power dissipation and area of rounded parallel multiplier. Rais et al [18] reported a design and implementation of standard and truncated 6×6-bit

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multipliers with FPGA resource utilization of 24 slices as compared to 36 slices of standard multiplier of a Spartan-3AN FPGA device. High speed multiplication is desired in DSP which is normally achieved by parallel processing and pipelining, but by truncation that can be multi fold to get rid of the undesired part of information. The objective of this paper is to present for the first time a comparison between device utilization of Sapartan-3AN and Virtex-5 FPGA devices.

The remainder of this paper is organized as follows. In section 2, the mathematical basis of truncated multiplication is briefly discussed. Section 3 discusses the architectural platform used in this study. FPGA design and implementation results are presented in section 4. Finally, conclusion is presented in section 5.

II. Truncated Multiplier Mathematical Basis

Considering the multiplication of two n-bit inputs X and Y, a standard multiplier performs the following operations to obtain the 2n bit product P

$$P = XY = \sum_{i=0}^{2n-1} P_i 2^i = (\sum_{i=0}^{n-1} x_i 2^i)(\sum_{i=0}^{n-1} y_i 2^i) \quad (1)$$

where x_i, y_i and P_i represent the i^{th} bit of X, Y and P, respectively.

Fig. 1 shows the standard architecture of 6×6-bit parallel multiplier, where HA and FA are the half and full adders respectively. Equation (1) can be expressed by the sum of two segments: the most-significant part *MP* and the least-significant part *LP*

$$P = MP + LP = \sum_{i=0}^{2n-1} P_i 2^i + \sum_{i=0}^{n-1} P_i 2^i \quad (2)$$

The standard 6×6-bit parallel multiplier can also be divided into three subsets: the most-significant part *MP*, input correction *IC* and the least-significant part *LP*. Equation (2) can be rewritten as follows:

$$P = MP + IC + LP \quad (3)$$

The fixed width multiplier can be obtained directly by removing the *LP* region and introducing the *IC* region to obtain MP' region, which is truncated multiplier as shown in Fig. 2 and given by equation (4).

$$P = MP' + IC \quad (4)$$

III. Target FPGAs Platform

Due to the parallel nature, high frequency, and high density of modern FPGAs, they make an ideal platform for the implementation of computationally intensive and massively parallel architecture. In this section a brief introduction about Spartan-3AN and Virtex-5 devices from Xilinx is presented.

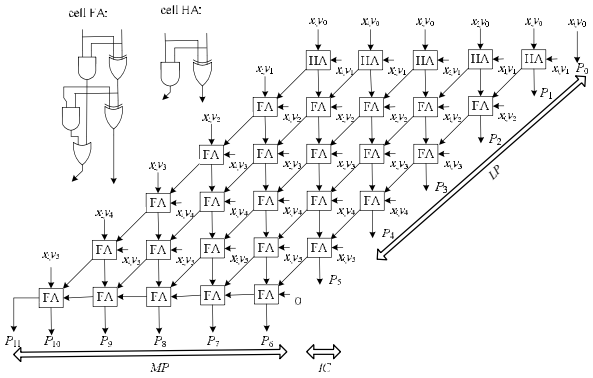

Fig. 1 The architecture of a standard 6×6-bit parallel multiplier

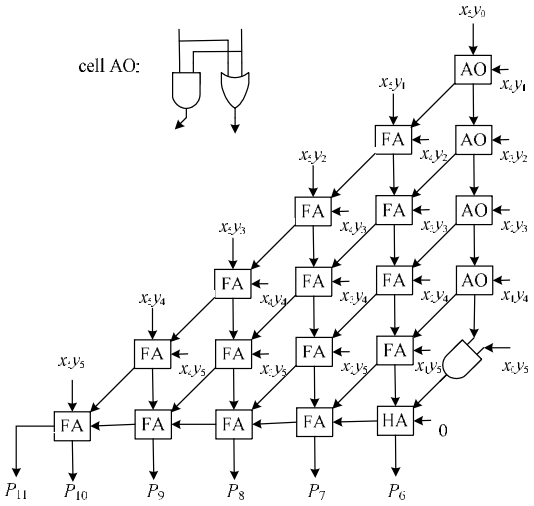

Fig. 2 The architecture of a truncated 6×6-bit parallel multiplier

A. Spartan-3 FPGAs

The Spartan-3 FPGA belongs to the fifth generation Xilinx family. It is specifically designed to meet the needs of high volume, low unit cost electronic systems. The family consists of eight member offering densities ranging from 50,000 to five million system gates [19]. The Spartan-3 FPGA consists of five fundamental programmable functional elements: CLBs, IOBs, Block RAMs, dedicated multipliers (18×18) and digital clock managers (DCMs), Spartan-3 family includes Spartan-3L, Spartan-3E, Spartan-3A, Spartan-3A DSP, Spartan-3AN and the extended Spartan-3A FPGAs. Particularly, the Spartan-3AN is used as a target technology in this paper. Spartan-3AN combines all the feature of Spartan-3A FPGA family plus leading technology in-system flash memory for configuration and nonvolatile data storage.

TABLE I

FPGA RESOURCE UTILIZATION FOR STANDARD AND TRUNCATED MULTIPLIER FOR SPARTAN-3AN

Bit Width	Multipliers	Four Input LUTs (11776)	Occupied Slices (5888)	Bonded IOBs (372)	Total Equivalent Gate Count	Average Connection delay (ns)	Maximum Pin delay (ns)
n = 4	Standard	30	16	16	180	1.421	3.598
	Truncated	18	11	12	111	1.272	2.705
n = 6	Standard	67	36	24	402	1.238	4.873
	Truncated	43	24	18	261	1.096	2.722
n = 8	Standard	121	62	32	726	1.085	3.968
	Truncated	76	40	24	456	1.072	3.641
n = 12	Standard	289	148	48	1734	1.079	3.766
	Truncated	164	87	36	984	1.307	3.971

TABLE II
FPGA RESOURCE UTILIZATION FOR STANDARD AND TRUNCATED MULTIPLIER FOR VIRTEX-5

Bit Width	Multipliers	Four Input LUTs (28800)	Occupied Slices (7200)	Bonded IOBs (440)	Total Equivalent Gate Count	Average Connection delay (ns)	Maximum Pin delay (ns)
4×4	Standard	22	15	16	154	0.927	1.990
	Truncated	11	6	12	77	0.773	1.140
6×6	Standard	46	28	24	322	0.955	1.757
	Truncated	27	14	18	182	0.854	1.730
8×8	Standard	83	30	32	581	0.826	1.697
	Truncated	50	19	24	350	0.765	1.500
12×12	Standard	190	88	48	1330	1.107	2.845
	Truncated	117	65	36	819	1.027	2.611

B. Virtex-5 FPGAs

The Virtex-5 devices built on a 65nm state-of-the-art copper process technology are a programmable alternative to custom ASIC technology. The Virtex-5 LX platform also contains many hard-IP system-level blocks, including Block RAM/first in first out (FIFO), second generation 25×18 DSP slices, SelectIO technology with built-in digitally-controlled impedance, ChipSync source-synchronous interface blocks, enhanced clock management tiles with integrated DCM and phase locked loop (PLL) clock generators, and advanced configuration options.

In addition to the regular programmable functional elements, Virtex-5 family provides power-optimized high speed serial transceiver blocks for enhanced serial connectivity, tri-mode Ethernet MACs and high-performance PPC 440 microprocessor embedded blocks. Virtex-5 devices also use triple-oxide technology for reducing the static power consumption. Their 1.0V core voltage and 65nm implementation process leads also to dynamic power consumption reduction as compared to Virtex-4 devices.

Advanced DSP48E slices are available in Virtex-5 FPGAs that helps in accelerating computation intensive DSP and image processing algorithms. These slices can operate at a maximum frequency of 550MHz, drawing only 1.38mW of power at 100MHz frequency [20].

IV. FPGA DESIGN AND IMPLEMENTATION RESULTS

The design of standard and truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers are done using VHDL and implemented in Xilinx Spartan-3AN XC3S700AN (package: fgg484, speed grade: -5) and Virtex-5 XC5VLX50 (package: ff676, speed grade: -3) FPGAs using the Xilinx ISE 9.2i design tool.

The results of FPGA devices resources utilization for standard and truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers are summarized in Table I and Table II. The comparison of number of occupied slices for both the devices for standard and truncated multipliers are shown in Fig. 3, which clearly shows that the Viretx-5 FPGA device utilizes fewer resources than the Spartn-3AN device. The Virtex-5 FPGA device shows better performance with a percentage ratio of number of occupied slices for standard to truncated multipliers is increased from 40% to 73.86% as compared to Spartan-3AN is decreased from 68.75% to 58.78%. The Standard multiplier in Virtex-5 device almost uses same resources as the truncated multiplier for the Spartan-3AN FPGA device as shown in Fig. 3.

Fig.4 shows four input look-up-tables (LUTs) for standard and truncated multipliers for both the FPGAs devices. The same phenomenon is observed here as compared to number of occupied slices for both the devices. The total equivalent gate count obtained for standard and truncated multipliers for both the FPGAs devices are shown in Fig. 5.

Figs. 6 and 7 illustrate the average connection delay and maximum pin delay for both the FPGAs devices for standard and truncated multipliers respectively. The anomaly in average connection delay and maximum pin delay for Spartan-3AN device (12×12-bit multiplier for standard and truncated multiplier) has been significantly reduced in Virtex-5 device as

shown in Figs. 6 and 7 respectively.

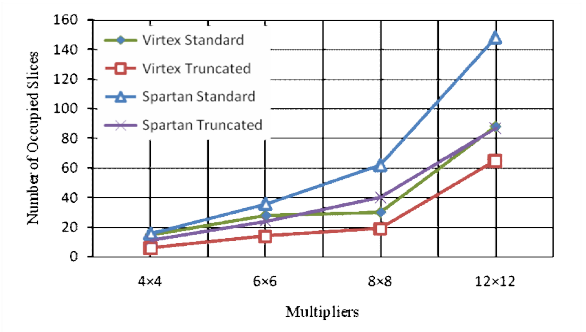

Fig. 3 The number of occupied slices for Spartan-3AN and Virtex-5 for standard and truncated multipliers

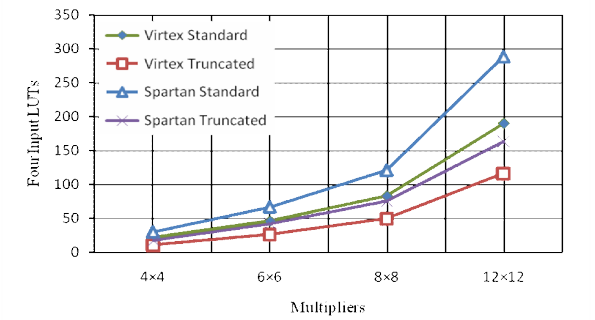

Fig. 4 The four input LUTs for Spartan-3AN and Virtex-5 for standard and truncated multipliers

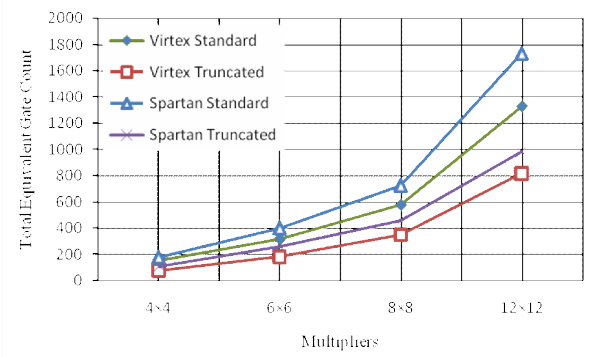

Fig. 5 The total equivalent gate count for Spartan-3AN and Virtex-5 for standard and truncated multipliers

The reduction in average connection delay and maximum pin delay and the number of occupied slices used in truncated multiplier also show that it is one of the viable solutions for image processing applications, where most of the redundant information can be removed.

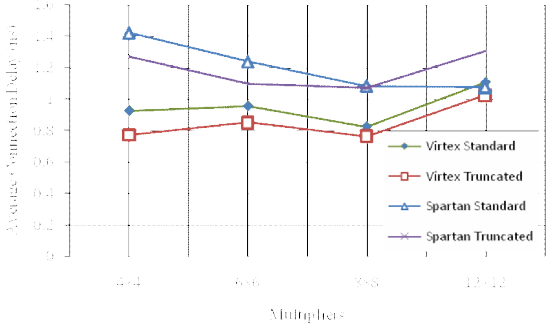

Fig. 6 The average connection delay for Spartan-3AN and Virtex-5 for standard and truncated multipliers

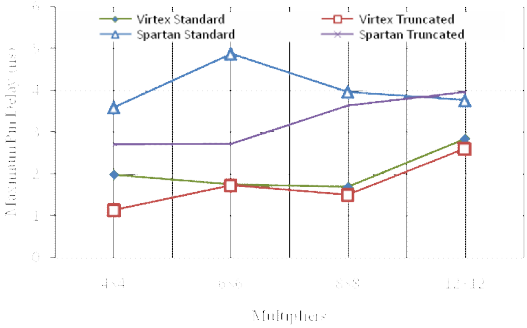

Fig. 7 The maximum pin delay for Spartan-3AN and Virtex-5 for standard and truncated multipliers

V. Conclusions

This paper presented a hardware design and implementation of FPGA based parallel architecture for standard and truncated multipliers utilizing VHDL. The design was implemented on Xilinx Spartan-3AN XC3S700AN and Virtex-5 XC5VLX50 FPGAs devices using the ISE 9.2i design tool. The truncated multiplier shows much more reduction in device utilization as compared to standard multiplier. Furthermore, the standard and truncated multipliers show that the number of occupied slices, four input LUTs, total equivalent gate count, average connection delay and maximum pin delay have been significantly reduced in Virtx-5 FPGA device. The Virtex-5 FPGA device shows better performance than Spartan-3AN FPGA device with a percentage ratio of number of occupied slices for standard to truncated multipliers is increased from 40% to 73.86% as compared to Spartan-3AN is decreased from 68.75% to 58.78%. The anomaly in Spartan 3AN device for 12×12-bit multiplier for standard and truncated multiplier has been significantly reduced in Virtex-5 FPGA device.

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