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Delay and Energy Consumption Analysis of Conventional SRAM

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***Abstract*—**The energy consumption and delay in read/write operation of conventional SRAM is investigated analytically as well as by simulation. Explicit analytical expressions for the energy consumption and delay in read and write operation as a function of device parameters and supply voltage are derived. The expressions are useful in predicting the effect of parameter changes on the energy consumption and speed as well as in optimizing the design of conventional SRAM. HSPICE simulation in standard 0.25µm CMOS technology confirms precision of analytical expressions derived from this paper.

***Keywords*—**Read energy consumption, write energy consumption, read delay, write delay.

I. Introduction

STATIC Random Access Memory (SRAM) has found its way into almost every IC as an embedded component. Traditionally, an SRAM macro is mainly formed by an array of cells consisting of four or six transistors and a number of periphery circuits such as row decoder, column decoder, sense amplifier, write buffer, etc. Information access from/to this macro consumes energy in both dynamic and static ways. The dynamic energy consumption involving the switching of signals is consumed in operations such as word-line decoding, bit-line charging/discharging, sense amplification, etc. The static energy consumption is consumed when there is a direct path from V_{DD} to ground during memory access [1]. Furthermore information access from/to this macro involve delay, due to RC networks exists in SRAM structure.

Two aspects are important for SRAM design: the dynamic energy consumption and delay of read and write operation. Dynamic energy consumption consumed energy of power supply during read and write operation and determines time battery operation in mobile application. The delay during read and write operation determine speed of SRAM, and this is important in height speed application. Much of the published work has been concerned with the power modeling in especial structure such as hierarchical bit-line SRAM [2][3]. And analytic work has not yet been reported include delay or energy consumption modeling for conventional SRAM.

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This paper is concerned with the delay and energy consumption in read and write operation of conventional SRAM both from an analytic as well as a simulation point of view in standard 0.25µm CMOS technology.

In Section II the structure, read and write operation of conventional SRAM discussed. Capacitance in conventional SRAM discussed in section III. Analytical expressions for the energy consumption and delay in read and write operation of conventional SRAM are derived in Section IV and V respectively. Simulation results are given in Section VI. And finally, we conclude with a brief summary in Section VII.

II. Conventional SRAM

The structure of conventional SRAM with 6T cell is shown in Fig. 1. In the following we describe the read and write operation in conventional SRAM.

A. Write Operation

When a write operation is issued the memory array will go through the following steps:

- Row and column decoding : The row and column address decoded and select one cell from memory array
- Bit-line driving: for a write, this bit-line driving conducts simultaneously with the row and column decoding by turning on proper write buffer. After this step, the bit-line pair will forced into full-swing logic level.
- Cell flipping: If the value of the stored bit in the target cell is opposite to the value being written, then cell flipping process will take place.
- Pre-charging: At the end of write operation all bit-lines pre-charged to the V_{DD} and get ready for next read or write operation [1].

B. Read Operation

When a read operation is issued the memory array will go through the following steps:

- Row and column decoding: The row and column address decoded and select the target cell.
- Bit-line deriving: after the word-line go to height voltage, the target cell connected to bit-line and bit-line-bar. The so-called cell current through a driver of target cell will discharge the voltage of either bit-line or bit-line-bar progressively and this resulted a difference voltage between the bit-line and bit-line-bar.
- Sensing: The sense amplifier is turned on to amplify the small difference voltage at bit-line pair into full-swing logic signals.
- Pre-charging: At the end of read operation all bit-line pre-charged to the V_{DD} [1].

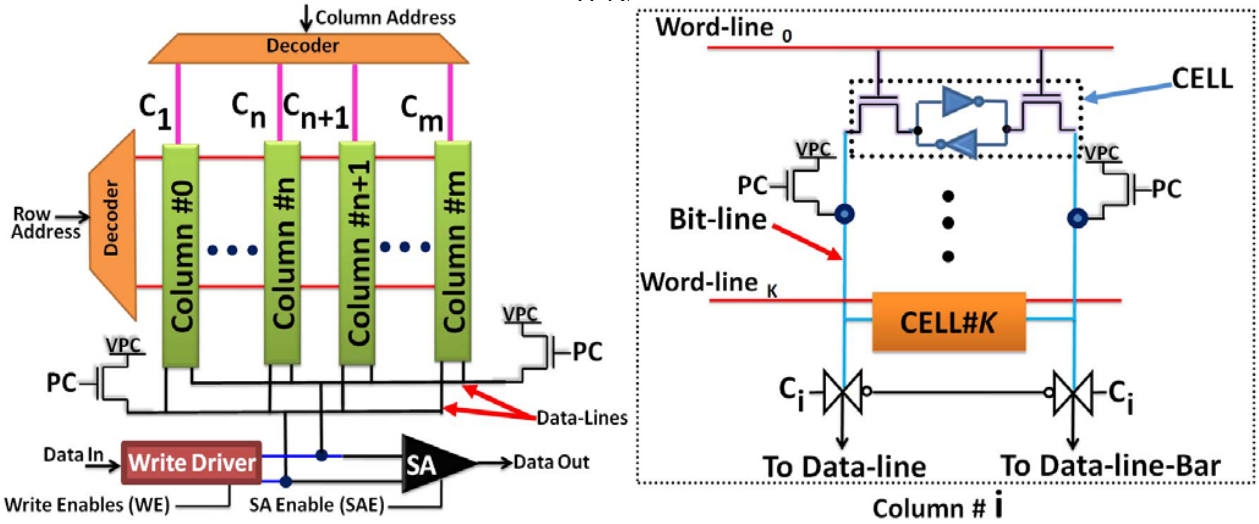

Fig. 1 Structure of conventional SRAM

III. Capacitance in Conventional SRAM

There are three premier capacitance in conventional SRAM that include bit-line capacitance, word-line capacitance, data-line capacitance. The bit-line capacitance is mainly composed of the drain junction capacitance of access transistor of memory cell and metal capacitance of bit-line. We can obtain this capacitance by following expression:

$$C_{BL} = C_{Junction\_AccessTransistor} \times 2^{Row} + C_M \quad (1)$$

Where, $C_{Junction\_AccessTransistor}$ is drain junction capacitance of access transistor of memory cell, Row is number of address line in row decoder and C_M is metal capacitance of bit-line and is assumed to be 10% of the total drain junction capacitance [2]. Thus the metal capacitance of bit-line obtained from following expression:

$$C_M = C_{Junction\_AccessTransistor} \times 2^{Row} \times 0.1 \quad (2)$$

The next large capacitance in conventional SRAM is word-line capacitance and is mainly composed of gate capacitance of the access transistor of memory cell and obtained by following expression:

$$C_{WL} = 2 \times C_{gate\_AccessTransistor} \times 2^{Column} \quad (3)$$

Where, $C_{gate\_AccessTransistor}$ is gate capacitance of access transistor of memory cell and Column is number of address line in column decoder. And finally the next large capacitance in conventional SRAM is data-line capacitance and this capacitance is mainly composed of junction capacitance of column access transistor and obtained by following expression:

$$C_{DL} = 2 \times C_{Junction\_ColumnAccessTransistor} \times 2^{Column} \quad (4)$$

Where, $C_{Jumction\_ColumnAccessTransistor}$ is drain junction capacitance of column access transistor (these transistor shown in Fig. 1) and Column is number of address line in column decoder.

IV. Dynamic Energy Consumption in Conventional SRAM

The energy consumption in the SRAM includes two components: dynamic energy consumption and static energy consumption. Static energy consumption, consumed due to leakage current in SRAM, and dynamic energy consumption consumed due to the charging and de-charging of capacitance during read and write operation. In following, we introduce explicit analytic expressions for estimation of dynamic energy consumption in read and write operation.

A. Dynamic Energy Consumption During Read Operation

There are four premier energy dissipation source during read operation include 1-energy dissipation during charging and discharging data-line capacitance 2- energy dissipation during charging and discharging word-line capacitance 3- energy dissipation during charging and discharging word-line capacitance 4- when row address decoded and one word-line asserted in row of memory array all cell in that row connected to bit-line and this caused unselected bit-line discharged thus energy dissipated on this lines.

Based on four premier energy dissipation sources during read operation that listed above dynamic energy consumption in SRAM for normal read operation, is given by:

$$E_{Read} = C_{W\,l} V_{DD}^{\,2} + C_{DL} V_{DD}^{\,2} + C_{BL} V_{DD}^{\,2} - \frac{1}{2} V_{BL}^{\,2} (C_{BL} + C_{DL}) + (2^{Column} - 1) \times \left[C_{BL} V_{DD}^{\,2} - \frac{1}{2} \frac{(C_{BL} V_{DD} - I_{PT} \Delta T)^2}{C_{BL}} \right] \quad (1)$$

Where, V_{BL} is voltage of bit-line at the end of read operation, V_{DD} is external supply voltage, ΔT is interval time that access transistor of cell is turn on and I_{PT} is current of access transistor of cell in saturation region, and obtained by following expression:

$$I_{PT} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 \quad (2)$$

Where, μ_n is the mobility of electron, C_{OX} is the gate capacitance per unit area, , W is the width of access transistor of cell, L is the length of access transistor of cell, V_{GS} is the gate-source voltage of access transistor of cell and V_{tn} is the threshold voltage of access transistor of cell. As described in section II during read operation voltage changed on bit-line, word-line, data-line and equation (1) is based on this fact.

B. Dynamic Energy Consumption During Write Operation

Dynamic energy consumption in conventional SRAM for normal write operation is given by:

$$E_{write} = C_{W\,l}V_{DD}^{\ 2} + C_{DL}V_{DD}^{\ 2} + C_{BL}V_{DD}^{\ 2} + (2^{Column} - 1)\left[C_{BL}V_{DD}^{\ 2} - \frac{1}{2}\frac{(C_{BL}V_{DD} - I_{PT}\Delta T)^2}{C_{BL}}\right] \quad (3)$$

Equation (3) is based on fact that, during write operation voltage changed on bit-line, word-line and data-line and this caused energy consumed like read operation.

V. Delay in Conventional SRAM

During transitions occur in read and write operation, transistors in SRAM structure can be modeled as a liner resistor [4], and RC networks shown in Fig. 2 can be considered for read and write operation. Based on these RC networks we can estimate the read and write delay by following expression:

$$T_{Read} = \tau_{PC} \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{PC}}\right) + \tau_{change\_read} \times \ln\left(\frac{V_{DD}}{V_{BL}}\right) + T_{SA} \quad (4)$$

$$T_{Write} = \tau_{PC} \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{PC}}\right) + \tau_{change\_write} \times \ln\left(\frac{V_{DD}}{V_{write}}\right) + T_{Filiping} \quad (5)$$

Where, V_{PC} is maximum voltage of bit-line and data-line at the end of pre-charging, V_{BL} is voltage of bit-line at the end of read operation, T_{SA} is delay of sense amplifier, V_{write} is voltage of bit-line that flipping process starts, $T_{Filiping}$ is delay of flipping process and depended on transistor size of SRAM cell ,and τ_{PC} , τ_{change_write} , τ_{change_read} obtained by following expression:

$$\tau_{PC} = R_{PC} \times Max\left\{C_{DL}, C_{BL}\right\} \quad (6)$$

$$\tau_{change\_read} = (R_{eq\_Driver\_Cell} + R_{eq\_access\_cell}) \times C_{BL} + (R_{eq\_Driver\_Cell} + R_{eq\_access\_cell} + R_{eq\_column\_access}) \times C_{DL} \quad (7)$$

$$\tau_{change\_write} = R_{eq\_Driver\_DL} \times C_{DL} + (R_{eq\_Driver\_DL} + R_{eq\_column\_access}) \times C_{BL} \quad (8)$$

Where, R_{eq_PC} is equivalent resistance of pre-charging

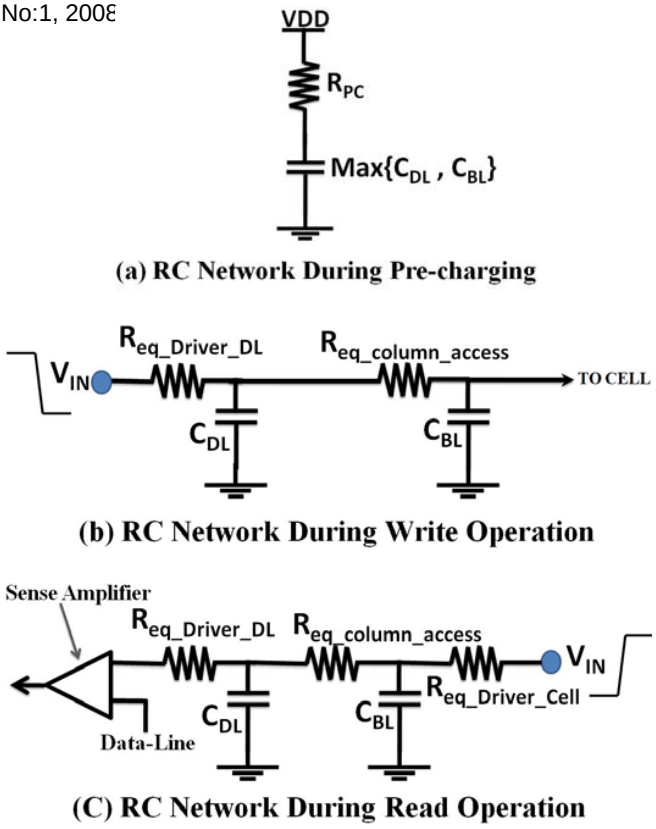

Fig. 2 RC Networks during read and write operation

transistor, $R_{eq\_Driver\_Cell}$ is equivalent resistance of deriver transistor of cell, $R_{eq\_access\_cell}$ is equivalent resistance of access transistor of cell, $R_{eq\_column\_access}$ is equivalent resistance of transmission gate, this transmission gate connect bit-line to data-line and $R_{eq\_Driver\_DL}$ is equivalent resistance of data-line driver transistors. The equivalent resistance for each transistor during a transition obtained by following equation [4]:

$$R_{eq\_each\_transistor} = \frac{2.5}{\mu_{n,p}\frac{W}{L}C_{OX}(V_{DD} - |V_t|)} \quad (9)$$

Where $\mu_{n,p}$ is mobility of electron or hole, W is the width of transistor , L is the length of transistor , V_t is threshold voltage of transistor. Since bit-line connected to data-line with transmission gate, $R_{eq\_column\_access}$ obtained by following expression:

$$R_{eq\_column\_access} = \frac{R_{eq\_n} \times R_{eq\_p}}{R_{eq\_n} + R_{eq\_p}} \quad (10)$$

Where R_{eq_n} and R_{eq_p} are equivalent resistance of NMOS and

PMOS of transmission gate and obtained by expression (9).

VI. Simulation Result

To evaluate the precision of obtained analytic expression in this paper, we simulate read and write operation of conventional SRAM in standard 0.25µm CMOS technology for different memory array size. In these simulations we use 2.5V for supply voltage and 0.5V and -0.5V for threshold voltage of NMOS transistor and PMOS transistor respectively. Fig. 3 shows layout of conventional 6 transistors SRAM cell in standard 0.25µm CMOS technology with traditional topology. Based on layout shown in Fig. 3, all parasitic capacitances and resistances of bit-lines, data-line and word-lines are included in the circuit simulation. In our simulation all transistors in SRAM structure have fixed size for different memory array size and following results obtained:

1-The read dynamic energy consumption predicted by analytic expression (1) is very close to values that obtained from simulation as shown in Fig. 4 and this indicates expression (1) has good precision.

2-The write dynamic energy consumption predicted by analytic expression (3) is very close to values that obtained from simulation as shown in Fig. 5 and this indicates expression (3) has good precision.

3-Read delay predicted by analytic expression (4) is very close to values that obtained from simulation as shown in Fig. 6 and this indicate expression (4) has good precision.

4-Write delay predicted by analytic expression (5) is very close to values that obtained from simulation as shown in Fig. 7 and this indicate expression (5) has good precision.

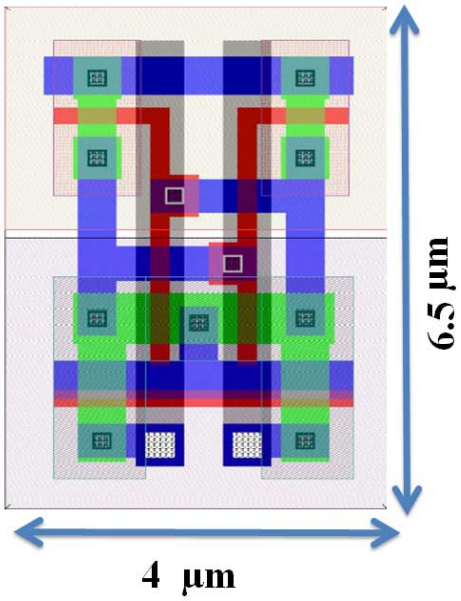

Fig. 3 Conventional layout of 6 transistor SRAM cell

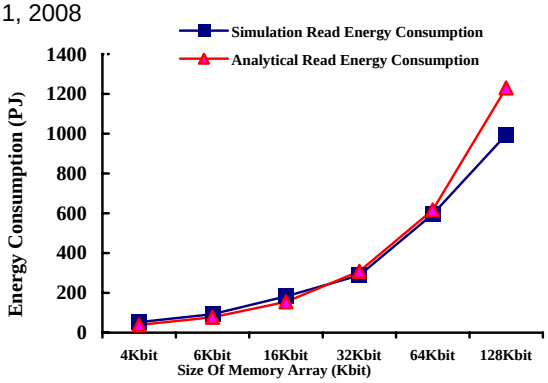

Fig. 4 Simulation and analytical read energy consumption

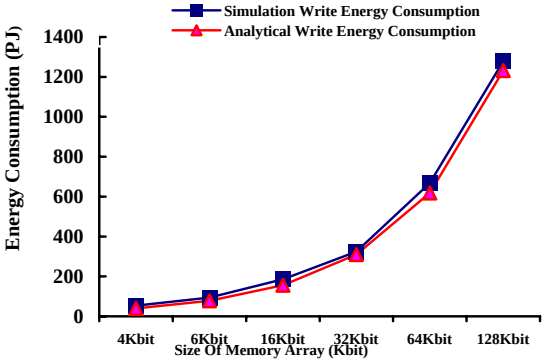

Fig. 5 Simulation and analytical write energy consumption

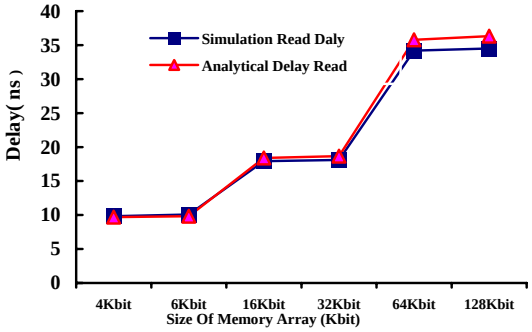

Fig. 6 Simulation and analytical read delay

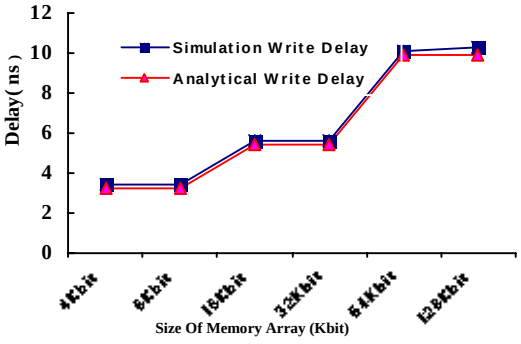

Fig. 7 Simulation and analytical write delay

VII. Conclusion

Capacitance in Conventional SRAM investigated analytically. Analytical expressions for the energy consumption and delay in read and write operation of conventional SRAM have been derived. The expressions are useful in predicting the effect of parameters as well as in optimizing the design of conventional SRAM. In addition, the simulation results in standard 0.25µm CMOS technology are in good agreement with the analytic expressions prediction.

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