International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:5, No:5, 2011

An Innovative Wireless Sensor Network Protocol Implementation using a Hybrid FPGA Technology

Danielle Reichel, Antoine Druilhe and Tuan Dang

***Abstract*—**Traditional development of wireless sensor network mote is generally based on SoC[1] platform. Such method of development faces three main drawbacks: lack of flexibility in terms of development due to low resource and rigid architecture of SoC; low capability of evolution and portability versus performance if specific micro-controller architecture features are used; and the rapid obsolescence of micro-controller comparing to the long lifetime of power plants or any industrial installations. To overcome these drawbacks, we have explored a new approach of development of wireless sensor network mote using a hybrid FPGA technology. The application of such approach is illustrated through the implementation of an innovative wireless sensor network protocol called OCARI.

***Keywords*—**Hybrid FPGA, Embedded system, Mote, flexibility, durability, OCARI protocol, SoC, Wireless Sensor Network

I. Introduction

Wireless Sensor Network (WSN) protocol implementation is a challenging issue when one has to deal with several objectives such as durability, portability, and evolutivity. These are difficult to satisfy while rapid development of prototype is an overall requirement. Implementing advanced and sophisticated OCARI [1] WSN protocol in a flexible, durable hardware platform using hybrid FPGA[2], allows time-saving in terms of qualification and long-term exploitation of WSN in nuclear plant.

Our approach of development is to use the combined advantages of ASICs and FPGA. To illustrate such advantages we chose to implement OCARI on a hybrid platform which has both ASIC and FPGA components. We consider that ASICs are COTS circuits, which are in terms of development similar to black box, contrary to FPGA-based hardware that is fully programmable and perfectly understandable by the design team who develops it.

In this paper, we describe different development approaches that use the specificities of hybrid development platform. Our idea is to develop the system from ASICs and FPGA simultaneously to rapidly test its performances, then to replace hardware ASICs portion by their equivalent IP in order to have a durable and flexible system. IPs are pre-existing VHDL blocks provided by a components library, that can be buy by the designer. In the end, specific VHDL codes can be developed by the user on the basis of the IP source code, so that total control of the design can be achieved. This approach of development is called “principle of migration” and is illustrated by the following figure (figure 1):

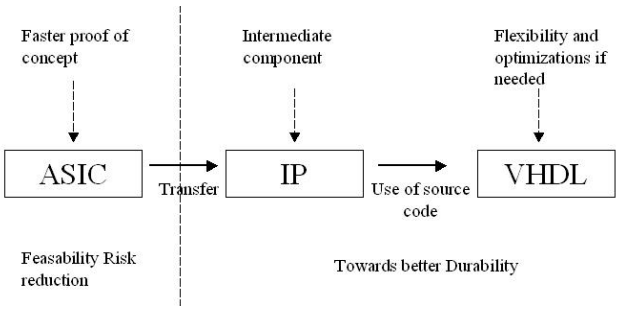


Fig. 1 Development principle based on migration approach

ASICs provide facilities for the implementation of software but are not durable. In case of obsolescence of these circuits, they can be “transferred” to IPs and then IPs can be reused or adapted for specific need using VHDL.

Usually, the development is faster with pre-existing ASICs; the software can be written and tested right at the beginning of the development process. These early tests give precious indications on the overall probability of success of the projet. On the contrary, FGPA-based embedded systems need a longer development time for the implemented hardware. Such approach also increases the risks without any warranty of success before a long time.

The novelty we introduce here is to build embedded system in two steps: a development on ASIC (COTS-based system) that gives confidence of success and a FPGA version that is more durable. All these steps are realized in a same "development flow" according to the same specifications using the same test vectors, and keeping exactly the same software throughout the project.

Our paper is organized as follow: chapter II gives a brief introduction of OCARI WSN communication protocol; chapter III describes the hybrid FPGA platform on which we implement OCARI and chapter IV presents the new approach of development to have a flexible and durable system.

II. OCARI PROTOCOL DESCRIPTION

OCARI is a communication protocol for Industrial Wireless

Tuan DANG and Antoine DRUILHE are with the STEP Department of EDF Research & Development, 6 quai Watier, 78401 Chatou Cedex FRANCE (e-mail: tuan.dang@edf.fr, antoine.druilhe@edf.fr) .

Danielle REICHEL is with the LME Department of EDF Research & Development, Avenue de Renardières, Ecuelles, 77818 Moret-sur-Loing cedex, FRANCE (e-mail: danielle.reichel@edf.fr).

[1] SoC: System on Chip

[2] FPGA is a programmable matrix of combinatorial interconnected and configurable cells. It is typically configured with a CAD tool that transforms the functions described in VHDL language into an electronic configuration.

Sensor Network. It was developed by different partners - EDF, DCNS, INRIA, LATTIS, LIMOS, LRI and Telit RF Technologies - during the OCARI project that was partially funded by the French National Research Agency. It is a wireless technology based on IEEE 802.15.4 standard and it offers the following functionalities:

- A deterministic access method to the RF medium supporting time-constrained packets relay, called MaCARI [2] [3].
- A proactive energy efficient routing strategy supporting micro-mobility, called EOLSR (Energy efficient OLSR) [4].
- An activity scheduling mechanism based on a three-hop coloring algorithm helps to reduce interference and thus optimizes node's energy consumption, called SERENA [5].

The following figure (figure 2) illustrates the OCARI stack:

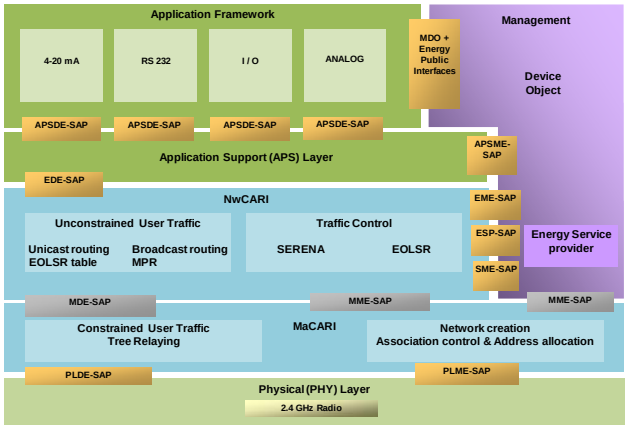


Fig. 2 OCARI stack

MaCARI is the layer that manages access to RF medium, initialize the network (address assignment, topology control) and control time-constrained traffic. NwCARI is responsible for ad hoc energy efficient routing and activity scheduling. “Energy service provider” is an advanced software component that estimates the residual energy of the battery.

OCARI is actually implemented on a SoC platform that has an integrated system which is composed of an 8-bits microcontroller, an IEEE-802.15.4 based RF transceiver, and a dedicated 16-bits microcontroller for the management of the application layer. Such SoC has limited resource and flexibility if one would like to extend OCARI functionality. Moreover, in case of obsolescence of the SoC, we need to adapt the software portion to a new platform and to realize all the required qualification procedures for constrained environment in nuclear power plant.

In this paper, we present our work of trying to implement OCARI on a hybrid FPGA platform with following requirements in terms of ASIC:

- A 32-bits low power microprocessor;
- 196 Kbytes of flash memory;
- 64 Kbytes of RAM memory for supporting large scale deployment of WSN. The memory is typically used for storing routing tables;
- A RF interface for an IEEE 802.15.4 RF transceiver.

The OCARI stack is stored in flash memory and is executed by the microcontroller to process dataflow to and from the RF transceiver via some standardized bus and interface (cf. figure 3).

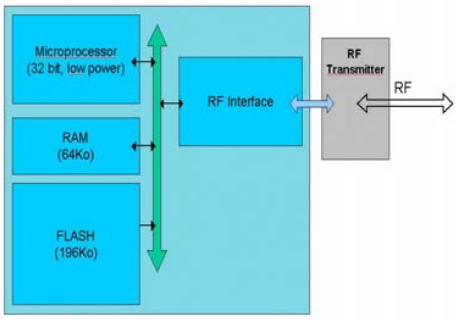


Fig. 3 Hybrid FPGA platform requirements

Our review of different FPGA platform manufacturers (Xilink, Altera, Actel…) shows that SmartFusion platform from Actel is the one which has the characteristics close to our requirements. Before describing our work on the implementation of OCARI on such platform, let’s introduce the main features of SmartFusion in the following chapter.

III. Hybrid FPGA Platform and Development Strategy

A. Platform description

The SmartFusion [6] platform has the following characteristics:

- A 32-bits ARM Cortex M3 microprocessor @100Mhz;
- 512 Kbytes of embedded flash memory;
- 64 Kbytes of embedded SRAM memory;

The development kit consists of a programmable matrix (FPGA), connected to a number of pre-existing ASIC circuits (microprocessor, interfaces, memories, internal bus, etc). ASICs can be activated or inhibited and are interconnected to design a particular architecture. The COTS ASIC-based portion and the FPGA portion can be easily interconnected through a dedicated interface which is called “Fabric” interface (cf. figure 4).

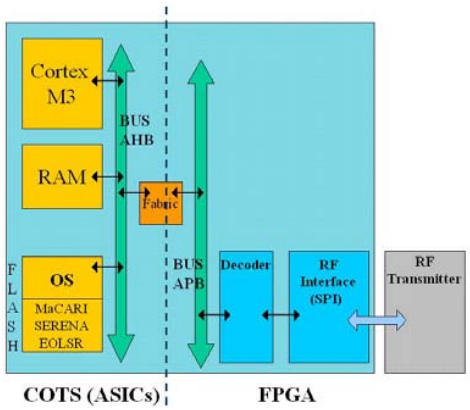


Fig. 4 Global architecture of SmartFusion hybrid platform

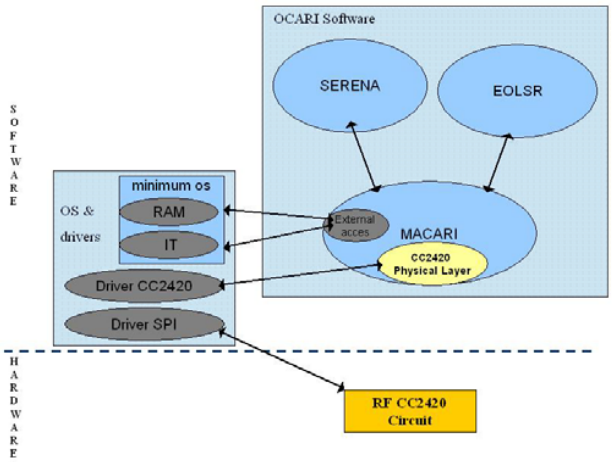
B. Development strategy

Hybrid platform has advantages in terms of ease of development. ASIC circuits in the SmartFusion platform are partially configurable. ASICs interfaces can be configured using VHDL and are programmable with the APIs[3] that are provided in the development software tools.

Using such platform, the component circuits can be configured and be adapted to the functionality needed and not the opposite. Moreover, the IP components can be designed to easily interface with ASICs circuits of hybrid platform. Actel also provides VHDL portion of the IP corresponding to most of ASICs that are available in the SmartFusion platform when they become obsolete. A rapid porting could be possible on another Actel platform using the provided VHDL.

IV. New Development Approach for a Flexible and Durable System

We propose to explore a new system development approach using the above hybrid platform through the implementation of OCARI. The overall architecture of our implementation is depicted by the following figure (figure 5):



[3] API : Application Programming Interface

Fig. 5 Overall architecture of OCARI implementation

We first begin with the development of minimal Operating System (OS) functionalities such as RAM access and Interruptions (IT) management. Furthermore, a task execution scheduler will be implemented to manage concurrent access to share resources such as RF transceiver. The current implementation of MaCARI is based on the CC2420 RF circuit from Texas Instruments; in order to minimize the effort of porting MaCARI to our hybrid platform, we use the same RF chipset for this work. Moreover, we also need to develop some drivers to provide transparent access to the CC2420 functionalities from higher layers such as MaCARI, SERENA and EOLSR. These specific drivers are related to our VHDL implementation of the interconnection between the ASIC portion (Cortex M3) and the FPGA portion that provides interface to the CC2420 RF transceiver (cf. figure 4).

Our approach requires a new paradigm of system development in which hardware and software designs must be concurrently done [7] as their interactions are very strong.

In our case, Actel supplies two mixed development tools which help to evolve the hardware and the software simultaneously altogether:

- Libero: a software chain that provides tools to develop the hardware platform based on FPGA;
- SoftConsole: a C language software development framework that is particularly useful for the debugging and the implementation of high level functions.

This development approach presents several strengths and benefits (see figures 6 and 7); however, contrary to the traditional [8] development approach in which we develop the software on the pre-existing SoC platform; this development approach implies more efforts in debugging. In particular, we need to identify and decorrelate hardware issues from software issues.

To resolve such issues, we have developed a test protocol which consists to test separately the hardware and the software. First, the hardware is tested using a simulation file which replaces the software (i.e. code executed by the microprocessor) and contains writing and reading commands in assembly language. Then, the software and the hardware are pooled together and the overall test of the system is realized; and if necessary the debugging of the software can be simultaneously done using the SoftConsole. In the case of OCARI system implementation, we start by testing if the bidirectional communications between the hybrid platform and the RF daughter board work correctly. Then, we made test bench on the IP and ASIC before doing their migration to VHDL. In our case study, it concerns the GPIO (IP) to GPIO Decoder (in VHDL) and SPI-ASIC to SPI-VHDL. Of course, if the optimization is required, the same migration process (ASIC to FPGA/VHDL) can be applied to “CC2420 driver” and “SPI driver”.

As shown in figure 6, on the one side, with the ASIC (COTS), we can rapidly develop a compliant/qualified system, and on the other side, when one uses the FPGA, the process of

development is much longer. This is the cost for obtaining a compliant, durable and optimized system.

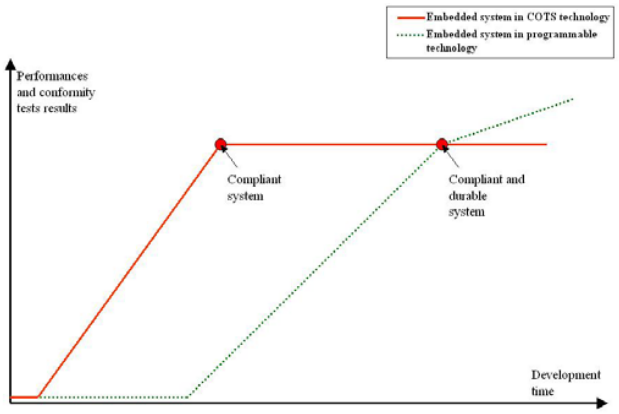


Fig. 6 Comparison of ASIC and FPGA system development approaches

During our development as shown in figure 7, we gain the benefits of using hybrid platform in terms of assessing the performances over time and of durability. The development contains four steps : proof of concept with ASIC and IP, ASIC/IP to VHDL migration test, software development and final migration toward durable component/system. These steps correspond to two main phases: evaluation of feasibility, then the design itself (conception in figure 7).

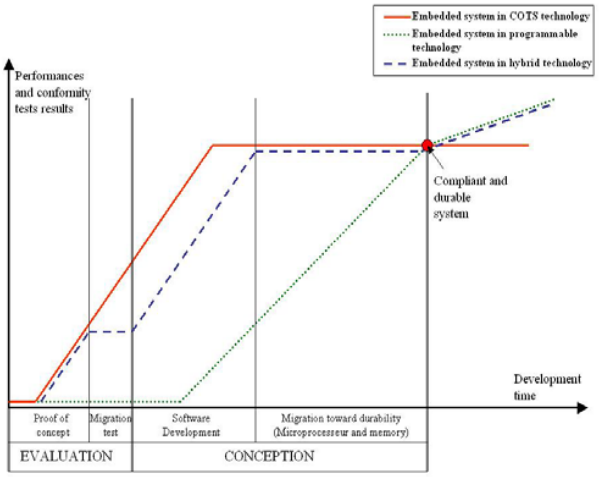


Figure 7: Benefits of using hybrid platform with four development steps.

The above approach gives other benefits such as ensuring more rapidly the system performance while being able to reduce the risks of a long development cycle.

V. Conclusions and Future works

We have presented a new system development approach that uses hybrid platform in which ASIC and FPGA components can be interconnected and configurable. To illustrate such approach, the implementation of the OCARI WSN has been used to assess the relevance of this development methodology. To fully assess the expected benefits, we continue to go further by realizing the whole OCARI embedded system and then benchmarking it with a SoC on which OCARI is currently implemented.

Acknowledgment

Authors thank Future Electronics and Actel for their kind support. This work is fully supported by EDF R&D.

References

[1] Khaldoun Al AGHA, Marc-Henri BERTIN, Tuan DANG, Alexandre GUITTON, Pascale MINET, Thierry VAL, Jean-Baptiste VIOLLET, “Which Wireless Technology for Industrial Wireless Sensor Networks? The Development of OCARI Technology”, IEEE Transactions on Industrial Electronics, volume 56, issue 10, October 2009, pp.4266-4278.

[2] G. Chalhoub, A. Guitton, M. Misson, MAC specifications for a WPAN allowing both energy saving and guaranted delay - Part A: MaCARI: a synchronized tree-based MAC protocol, IFIP 2008 Conference on Wireless Sensor and Actor Networks.

[3] E. Livolant, A Van den Bossche, T.Val, MAC specifications for a WPAN allowing both energy saving and guaranted delay - Part B: Optimisation of the intra cellular exchanges for MaCARI, IFIP 2008 Conference on Wireless Sensor and Actor Networks.

[4] S. Mahfoudh, P. Minet, An energy efficient routing based on OLSR in wireless ad hoc and sensor networks, PAEWN 2008, IEEE International Workshop on Performance Analysis and Enhancement of Wireless Networks, Ginowan, Japan, March 2008.

[5] P. Minet, S. Mahfoudh, G. Chalhoub, A. Guitton, Node coloring in a wireless sensor network with unidirectional links and topology changes, IEEE WCNC 2010, Sidney Australia, April 2010.

[6] http://www.actel.com/products/SmartFusion/default.aspx, March 2011.

[7] W. Wolf, “A decade of hardware/software codesign,” IEEE Computer, vol. 36, pp. 38–43, April 2003.

[8] P. Garcia, K. Compton, M. Schulte, E. Blem, andW. Fu, “An overview of reconfigurable hardware in embedded systems,” EURASIP Journal on Embedded Systems, vol. 2006, pp. 1–19, 2006.