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A Single-chip Proportional to Absolute Temperature Sensor Using CMOS Technology

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Abstract—Nowadays it is a trend for electronic circuit designers to integrate all system components on a single-chip. This paper proposed the design of a single-chip proportional to absolute temperature (PTAT) sensor including a voltage reference circuit using CEDEC 0.18m CMOS Technology. It is a challenge to design asingle-chip wide range linear response temperature sensor for many applications. The channel widths between the compensation transistor and the reference transistor are critical to design the PTAT temperature sensor circuit. The designed temperature sensor shows excellent linearity between $-100°$C to $200°$ and the sensitivity is about 0.05mV/°C. The chip is designed to operate with a single voltage source of 1.6V.

Keywords—PTAT, single-chip circuit, linear temperature sensor, CMOS technology.

I. Introduction

A simple CMOS PTAT circuit is shown in Figure 1 which is the basic foundation of a wide range of linear temperature sensors. A fully integrated CMOS PTAT [1] temperature sensor with a linear range of only between $32°$C to $127°$C, was designed through a complex structure using 27 elements including transistors and other components. The variation of voltage range due to temperature is only 1.6 V with a power supply of 3 V. A better linear response circuit [2], was designed using Independent PTAT Absolute Temperature (IOAT) sensor with a range of $-55°$C to $170°$C,Its design was also complex and used many components. A simple CMOS temperature sensor of linear range only within $-40°$C to $140°$Cwas designed and simulated[3] by using Mentor Graphics Toolkit (ADK-3) v2006.2_4.1 (2006.2b).

This paper proposed a simple CMOS PTAT sensor circuit with a wide range of linearity using only eight CMOS transistors. The circuit is developed based on CMOS current reference without resistance [4]. They propose, The construction of this type of PTAT circuit is similar to Figure 1. In addition an NMOS transistor is added in the circuit to compensate the transistor current variation in PTAT circuit due to temperature, which results in better performance. This modification increases the compensation transistor linear response as well as the temperature sensor. Further a current reference and voltage reference circuits can improve the linearity of the sensor [5] furthermore, by adjusting the transistors channel width ratio (W2/W1) with supply voltage.

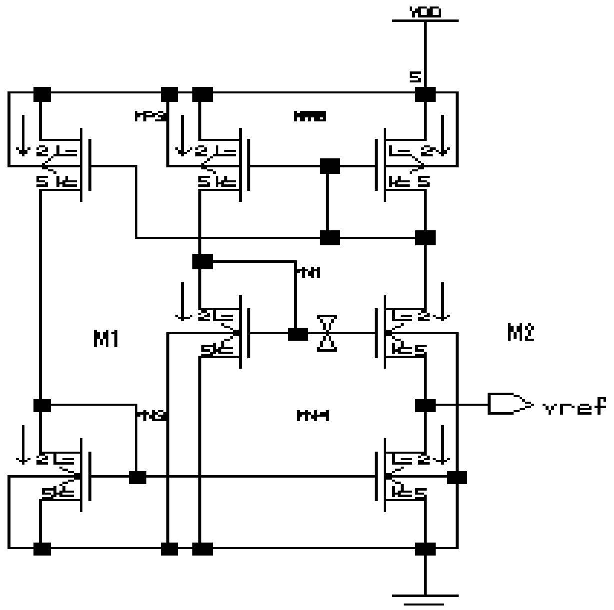

Fig. 1. Basic CMOS PTAT temperature sensors

II. Methodology

At first a schematic is drawn according to the basic PTAT temperature sensors as shown in Figure 1 using Mentor Graphics Toolkits (ADK-3) v2006.2_4.1 (2006.2b) and the design is verified by simulation. Initially a suitable width ratio (W2/W1) of the transistors is chosen and the supply voltage (VDD) is varied from 0.1 V to 3.0 V until is obtained the best linear response from the circuit.

In the second step, simulation is carried out by setting the voltage supply VDD as constant using the best range in the first step of simulation. The width W1 of the transistor M1 and width W2 is obtained M2 continue are adjusted until a best result. During this simulation the transistors width ratio W2/W1 is varied from 1 to 4 and the appropriate value which shows the best linear response and better sensitivity

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is selected. Then the optimal parameter values of the circuit are determined and the final circuit diagram for the PTAT temperature sensors is shown in Figure 2.

Third end final step of the simulation is carried out by using the optimal value of W2/W1 and VDD for the circuit shown in Figure 6. In this simulation industry standard liberty cell toolkit CEDEC for Silterra Version 2008.6 is used.

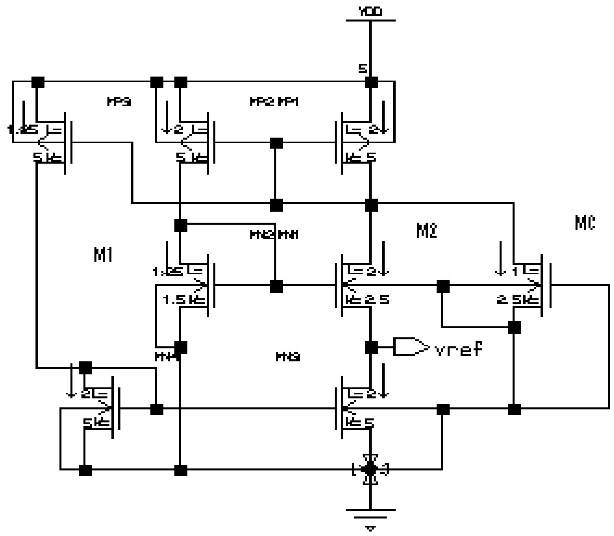

Fig. 2. CMOS PTAT temperature sensors with transistor Compensation

III. Results and Discussion

Figure 3 shows the simulated graphical results of the basic PTAT temperature sensor with fixed value of W2/W1 and the supply voltage (VDD) varied from 0.1 V with increment of 0.25 V up to 3 V approximately. The linear response of the output voltage of the sensor increases with increase in the supply voltage. The graph shows that VDD has no effect to improve the linearity up to 60°C when the transistor length ratio W2/W1 remains fixed. The graphs in Figure 3 show that best sensitivity of the sensor is obtained when the supply voltage VDD is between 1.5 V to 3.0 V.

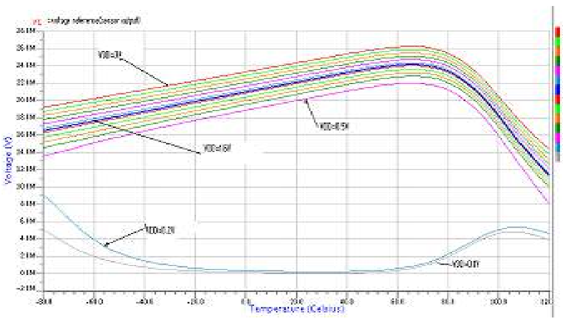

Fig. 3. The respond of the basic PTAT with various VDD

Figure 4 shows the output voltage response of the PTAT temperature sensors with fixed supply voltage VDD and changing the transistor width ratio W2/W1 from 5 / 1 to 5 / 6 with a constant decrement. From this graphical result it is shown that best linearity and sensitivity are obtained when the transistors width ratio W2/W1 is 5 / 2.

Figure 5 shows the graphical result of the proposed PTAT temperature sensors with addition of the compensation transistor as shown in Figure 2, supply voltage VDD equals 1.6 volt and transistors width ratio W2/W1 equals 5/2. The result shows that the sensor linear range is extended from -40°C to 140°C. This simulation result is better than the simulation result obtained without using the compensation transistors.

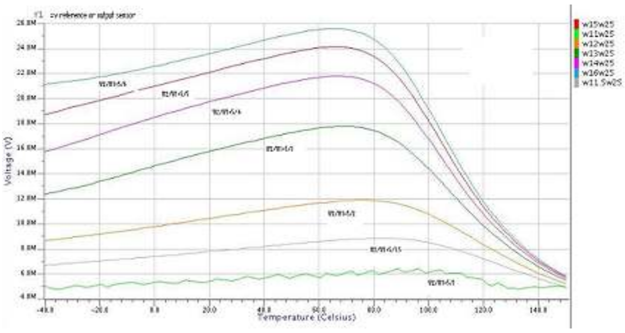

Fig. 4. The responds PTAT temperature sensors voltage reference with various of composition (w2/w1)

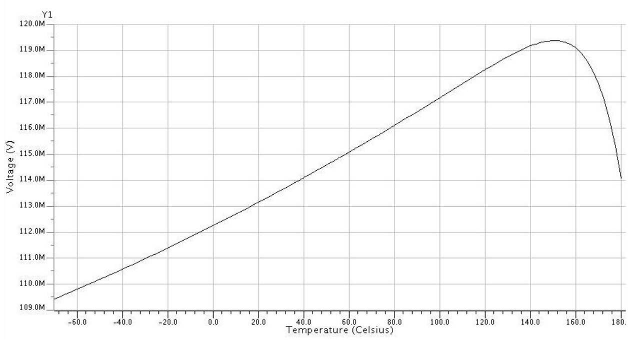

Fig. 5. The responds PTAT temperature sensors voltage reference with fix's Vdd

Figures 6 and 7 show the design and simulation results respectively when industry standard cell library toolkit CEDEC for Silterra version 2008.6 is used. Figure 7 shows the graphical result of the final proposed design. It is seen that the linear range of response is -100°C to 200°C which is much larger than previous works. The slope at any point on the response curve is the measure of sensitivity of the sensor. In the linear portion of the response curve as shown in Figure 7 the sensitivity of the sensor is measured as 0.05 mV/°C.

Figure 8 shows the chip layout design of the complete circuit including power supply and I/O pads, which occupied maximum 520x430 μm^2 of silicon area.

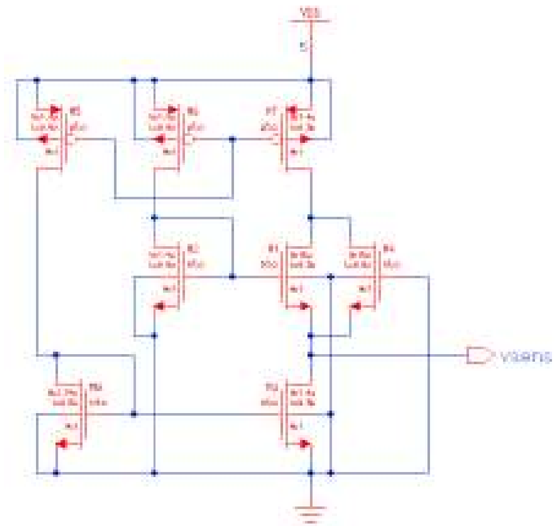

Fig. 6. Proposed CMOS PTAT temperature sensors with transistor compensation Cedec' Silterra design

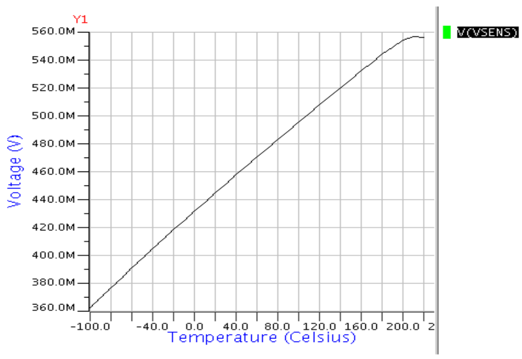

Fig. 7. The graph of responds PTAT temperature sensors voltage reference By Cedec' Silterra design

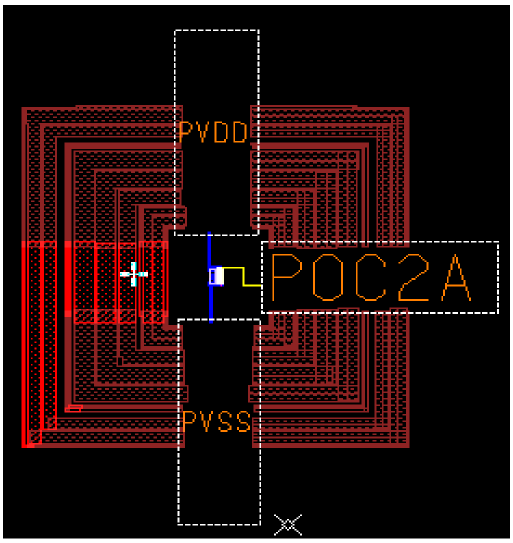

Fig. 8. Form a completed chip design

IV. Conclusion

A simple PTAT temperature sensor is designed and verified by simulation using Mentor Graphics VLSI design software. The final chip is designed by CEDEC industry standard I/O cell library for fabrication lab Silterra, Malaysia. The designed chip size is 520x430 μm^2 and consumes 8.5 μW power. The sensor shows excellent linear response in the temperature range between $-100°C$ to $200°C$. The sensitivity of the PTAT temperature sensors is 0.05 mV/°C when compensation CMOS transistors width ratio W2/W1 equals to 5/2 and power supply equals to 1.6 V.

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