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Data-driven ASIC for Multichannel Sensors

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***Abstract*—**An approach and its implementation in 0.18 μm CMOS process of the multichannel ASIC for capacitive (up to 30 pF) sensors are described in the paper. The main design aim was to study an analog data-driven architecture. The design was done for an analog derandomizing function of the 128 to 16 structure. That means that the ASIC structure should provide a parallel front-end readout of 128 input analog sensor signals and after the corresponding fast commutation with appropriate arbitration logic their processing by means of 16 output chains, including analog-to-digital conversion. The principal feature of the ASIC is a low power consumption within 2 mW/channel (including a 9-bit 20Ms/s ADC) at a maximum average channel hit rate not less than 150 kHz.

***Keywords*—**Data-driven architecture, derandomizer, multichannel sensor readout

I. Introduction

THE hardware for modern multichannel experiments clearly tends to increase its integration degree. It's enough to mention a number of physical experiments at large accelerators, the development of medical equipment, recognition and monitoring systems. In accordance with this the SoC, based on advanced digital CMOS, can provide the density, low power and analog integration capability needed for the high volume and small form factor applications of the future[1]. Although traditional MOSFET scaling techniques have not been good for analog circuits due to degraded transistor gain g_m/g_{ds}, reduced dynamic range, and worse transistor mismatch, modern SoC have successfully incorporated a larger number, and a wider range, of high performance analog circuits, than in the past, due to circuit innovations [2]. Moreover the traditional parallel architectures have become unacceptable for now, due to high power consumption and low cost efficiency. Therefore along with the technology and circuital innovations, there are architectural challenges, particularly concerning the development of the asynchronous data-driven system.

The primary information data streams have an essential non informational part that is desirable to be reduced at the early stages of processing in near-to-real time scale. It is important not to lose useful information and reduce the dead time, which is often necessary to analyze the data. This problem can be solved by using digital signal processing, but the area occupied on-chip by the fast highbit-ADCs, as well as their power consumption are still a technical challenge, when they are used for each channel. The second major problem is the random nature of the input sensor information, while digital systems are preferable to function clocked, that is, the digital inputs should change in short predetermined intervals, that significantly reduces malfunctions in digital processing.

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II. Data-Driven Architecture And Control Logic

One of the major trends in the modern readout microelectronics is the need of the asynchronous physical sensor data readout. The increasing number of the readout channels often along with low data density induces the development of the ASICs using data-driven architecture [3-6]. Such ASICs use different implementations of the data-driven architectures. They exhibit definite both advantages and drawbacks. The main direction during the development of the data-driven ASIC for multichannel sensors is to focus on the next features: real-time data processing and transfer to the acquisition system, reduced number of blocks in the design (which is necessary to reduce the power consumption and the area occupied by the chip). In certain applications such as a modern physical experiment or medical equipment it's also important to have highly integrated ASICs, containing all the needed data processing blocks within one chip.

Taking into account that as a rule the sensor system does not have 100% load on the total number of channels and it is spatially distributed in a certain way, one can connect the chip so that the maximum number of loaded channels will not exceed a definite value of N when M are to be read out.

The ratio of M/N may be called as a derandomization factor. It has practical value when M > N. In architectural terms, this means the system with M sensor readout channels and N output processing channels.

While the input channel occupancy is incomplete, the use of an analog derandomizer permits to minimize the number of data processing channels. From the viewpoint of reducing the number of architecture blocks and using an on-line data processing, the system is designed as an unbuffered one. The derandomization factor is chosen so, as to make the signal loss not to exceed the specified error probability at a known maximal average hit-rate of the read-out channel.

The technique of choosing the derandomization factor is based on analyzing the probability of a simultaneous occupation of a number of processing channels (1), using the binomial distribution with $P_0 = (f/F)$ and taking into account the maximum average hit-rate (f) and known event rate (F).

Fig. 1 presents the results of analysis for a maximum average hit-rate in a channel from 150 to 1200 kHz at 128 read-out channels (P – probability of a simultaneous occupation of N channels).

$$P(N,f) = \frac{M!}{N! \times (M-N)!} \times \left(\frac{f}{F}\right)^M \times \left(1-\frac{f}{F}\right)^{M-N} \quad (1)$$

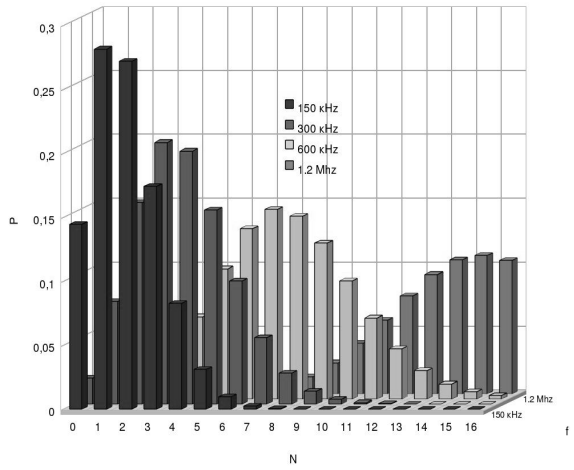

Fig. 1 Probability of a simultaneous occupation of N channels

It's also necessary to take into account the variation of probability of simultaneous pulses in N channels due to increasing pulse width at the output of the sensor amplifier-shaper. This can be achieved by using P_{max} (2) instead of P_0 in the binomial distribution, where k is the ratio of pulse width at the output of the shaper to the one at the input. This effect is not very significant in this case, but potentially it can become such under certain conditions, and thus this step is important in the data-driven mixed signal ASIC design methodology [8].

$$P_{\max} = 1/(\sum_{i=1}^{k} 2\times(1-\frac{i}{k}) + (\frac{F}{f} - 2\times(k-1))) \quad (2)$$

The function of de-randomization of analog signals is provided by an analog key matrix, controlled by a logical unit that can analyze the chaotic appearance of the input signals in the readout channels and the possibility of their transfer to the free processing channels.

The logic of the derandomizer is based on the fact that the pulse shape is known, and the other fact that the maximum load on the system is possible only in the case of simultaneous events in all N channels. The number of occupied readout channels is not greater than the number of processing channels (provided that they are ready), and repetition period of the event exceeds the signal processing time in the employed channel.

In order to avoid distortion of the amplitude information it is necessary to switch all channels in a time not exceeding a certain peaking time of the signal.

Given that every act of switching the readout channel to a processing one occurs at the front of clocking signal. It is sufficient to establish its frequency so, that the duration of N cycles will be less than the peaking time of the input signals. This case is presented in Fig. 2.

III. ASIC DESIGN

The derandomization technique was implemented in the ASIC for the read-out of microstrip sensors. It has been under development for the last few years. The requirements of the silicon tracker station in the international CBM experiment

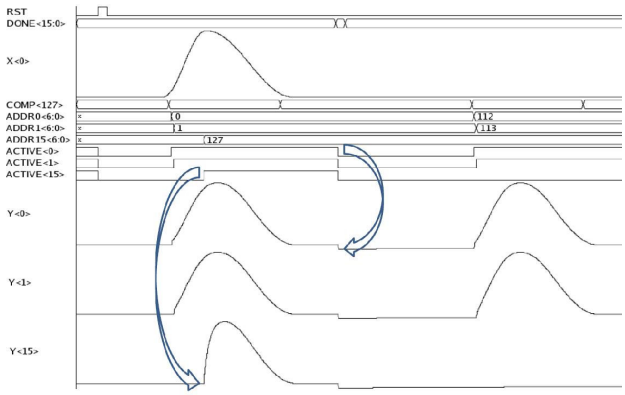

Fig. 2 The mixed-signal swithing time diagram

(GSI/FAIR, Darmstadt) were used in the design [7]. The ASIC block diagram is presented in Fig. 3 and a more detailed description given in [9]. The ASIC consists of a set of analog channels for readout of microstrip sensors, analog switch matrix (derandomizer core) with control logic and output processing channels. Such a derandomizing structure allows to readout 128 sensors by means of the 16 processing channels only.

The readout chain contains a DC charge-sensitive amplifier (CSA) with a circuit of sensor leakage current compensation (up to 1 μA), followed by a shaper (active filter) and fast leading edge comparator. The data processing channel includes a peak detector for amplitude storage and an ADC.

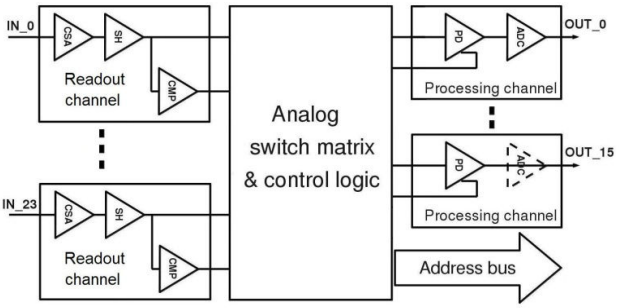

Fig. 3 The ASIC structure

CSA has a gain of 50 mV/fC and is optimized for the signals not more than 7.5 fC and sensor capacitance up to 30 pF. Fig.4 shows the typical output response of CSA for both polarities of input charge. The shaper circuit is a semi-Gaussian filter of a CR-RC type. It forms the response with a peaking time of about 100 ns and a fall time of about 300 ns. A leading edge comparator provides information about the time of analog signal occurrence. Its threshold is set to a minimum value, but high enough to be 3-4 times higher than the noise level. Most important for timing is the weak dependence of the comparator propagation delay versus amplitude over threshold. The variation of the propagation delay in the dynamic range of interest is less than 1 ns.

Derandomizer commutes the occupied front-end channels to the free processing channels. The structure of arbitration logic is shown in Fig.5.

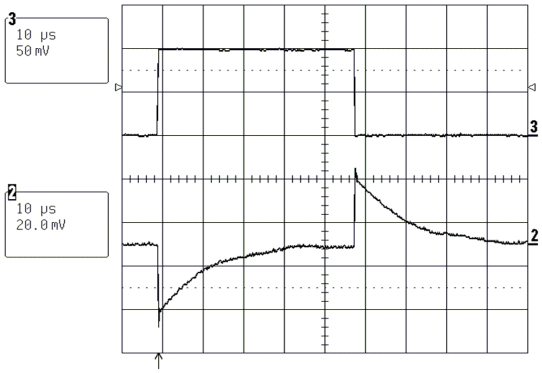

Fig. 4 The CSA response

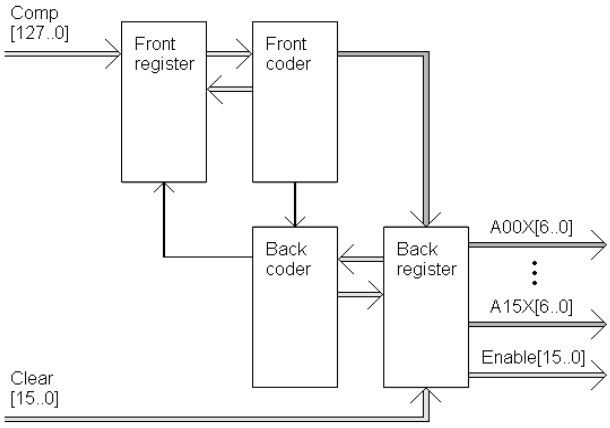

Fig. 5 The arbitration logic

As a peak detecting circuit in the ASIC design there has been used the topology, based on the rectifying current mirror [10]. The ADC block has a pipe-lined structure and provides a 20 Ms/s sampling rate at 9-bit resolution [11].

IV. PHYSICAL IMPLEMENTATION

The ASIC has been prototyped using the UMC 0.18 µm CMOS MM RF process via the Europractice foundation and the corresponding testing environment has been also developed.

The ASIC layout is given in Fig. 6. Its area has a size of 1525 × 3240 µm^2. The middle part presents a full scaled (128 to 16) analog switch matrix and control logic. The number of the front-end read-out chains has been reduced down to 24. That provided a cost-effective approach at prototyping, but still allowed to check functionality (firstly the derandomizing algorithm) and parameters of the building blocks.

The principal goals for the experimental checkout of ASIC samples were to verify its functioning against the specified algorithm. From this viewpoint especially important were the checkouts of operation at some extreme conditions. These are: 1) the number of overlapping input signals equals or even exceeds the number of available outputs; 2) the leading edges of input signals have close delays relative to each other or are overlapping; 3) the operation frequency of the clock generator is ultimate.

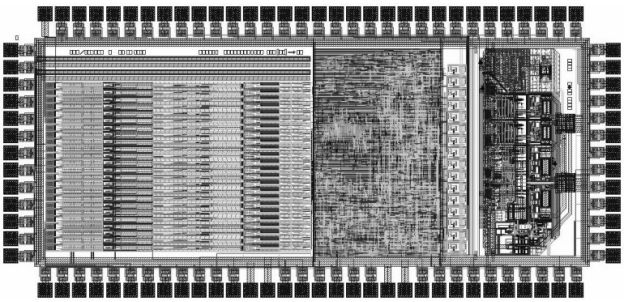

Fig. 6 The ASIC layout

The checking equipment contains a specialized unit, the core of which is a multichannel generator with the options of altering such signal parameters, as: amplitude, duration, shape and delay relative to the trigger pulse. The multichannel generator has been fitted with the analog elements, controlling duration and delay, in order to create a pseudo-random set of input signals, having an arbitrary delay relative to the leading edge of clock pulse.

One of the typical sets of transient responses is shown in Fig.7. It shows the switching of the 4 input read-out channels (top) to the 2 output processing ones (bottom). It should be noted that the two input signals occur simultaneously, but can be processed by two different output chains.

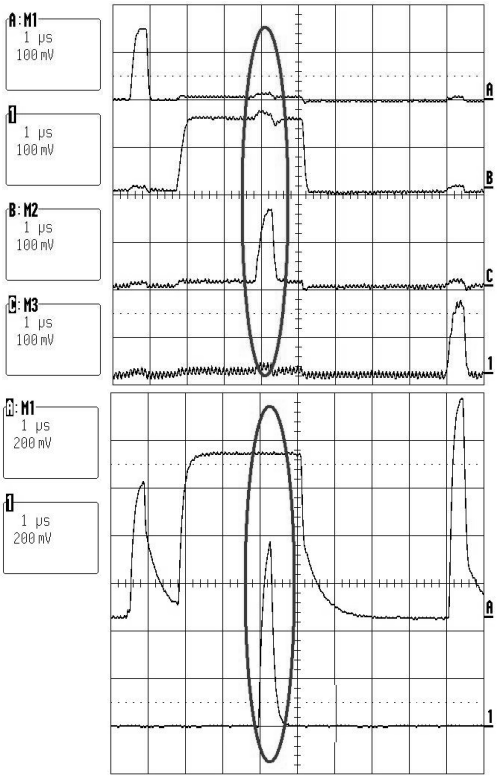

Fig. 7 The switching of the 4 read-out channels (top) to 2 processing ones (bottom)

V. Conclusion

The results of developing an asynchronous data-driven architecture for multichannel capacitive (up to 30 pF) sensors have been presented. The simulation and testing results of an analog data-driven system, implemented in a 0.18 μm CMOS process as a mixed-mode ASIC, have been discussed. During the design a compromise in a set of parameters, focused on low power consumption, performance and no dead time, has been achieved. The requirements of the silicon tracker station in the CBM experiment were used in the design. The lab test results have confirmed the expected functionality and specifications. The principal feature of the ASIC is a low power consumption within 2 mW/channel (including a 9-bit 20Ms/s ADC) at a maximum average channel hit rate not less than 150 kHz. A future implementation of a full-scaled 128 channel version of the ASIC is expected via direct multiplication of the front-end analog chains and output ADC developed. At present a logic part has been designed and built into the ASIC as a full scale 128 channel one. The number of sensor readout chains was reduced and provided a cost-effective approach at prototyping.

Acknowledgment

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