Analysis of Current Mirror in 32nm MOSFET and CNTFET Technologies

Mohini Polimetla and Rajat Mahapatra

Abstract—There is need to explore emerging technologies based on carbon nanotube electronics as the MOS technology is approaching its limits. As MOS devices scale to the nano ranges, increased short channel effects and process variations considerably effect device and circuit designs. As a promising new transistor, the Carbon Nanotube Field Effect Transistor(CNTFET) avoids most of the fundamental limitations of the Traditional MOSFET devices. In this paper we present the analysis and comparision of a Carbon Nanotube FET(CNTFET) based 10μA current mirror with MOSFET for 32nm technology node. The comparision shows the superiority of the former in terms of 97% increase in output resistance,24% decrease in power dissipation and 40% decrease in minimum voltage required for constant saturation current. Furthermore the effect on performance of current mirror due to change in chirality vector of CNT has also been investigated. The circuit simulations are carried out using HSPICE model.

Keywords—Carbon Nanotube Field Effect Transistor, Chirality Vector, Current Mirror

I. INTRODUCTION

AS semiconductor devices and integrated circuits continue to scale down into nanometer ranges, the semiconductor industry is starting to face several difficult challenges. Scaling has resulted in increased short-channel effects, reduced gate control, exponentially rising leakage currents, severe process variations, and unmanageable power densities. The scaling of CMOS technology has progressed rapidly for three decades, but may soon come to an end because of the increased short channel effects and power-dissipation constraints. Therefore, alternative technologies to bulk silicon transistors are being explored. A candidate transistor that may allow for both the shrinking process to continue , and for the development of novel architectures, is the carbon nanotube field-effect transistor(CNTFET)[1].

Carbon nanotube field effect transistors (CNTFETs) utilize semiconducting single-wall CNTs to assemble electron devices similar to MOSFETs, and fabrication of CNTFETs has been reported in recent years. With an ultralong (~1um) mean free path (MFP) for elastic scattering, a ballistic or near-ballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under a low voltage bias to achieve

improvements in performance[2] . Also, a CNTFET has a significantly smaller off current; therefore the power consumed when the transistor is off is greatly reduced in CNTFET designs. These properties make CNTFET one of the promising new devices to extend or complement traditional silicon technology for high performance and low power designs.

Current mirrors (CM) are essential and widely used building blocks in analog integrated circuits. They are used to perform current amplification, biasing, active loading and level shifting. Hence, their efficient design improves the overall performance of the system. The most important parameters of current mirrors are accuracy, input/output compliances, input/output impedances, bandwidth, linearity, noise and sensitivity to changes in load impedance. Due to technology down scaling and its intrinsic benefits, the trend in VLSI design is to reduce voltage supply. Hence, low voltage and low power circuit designs are in great demand. So, it is necessary to develop some new structures of Current Mirror under low voltage low power conditions [3]. CNTFET 's low threshold voltages and high output resistances has made it a good candidate for current mirror designs. Furthermore, the MOSFET-like CNTFET model is reported to be scalable down to 10nm channel length, a substantial improvement compared with the available MOSFET model (with a minimum channel length of 32nm). Therefore, a current mirror design with CNTFET requires a significantly less area than its CMOS counterpart.

II. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

CNT is a graphene sheet that shaped to a cylindrical nanostructure and based on number of rolled layers is categorized to single-walled nanotube (SWNT) and multi-walled nanotube (MWNT). Electrical properties of nanotubes, deeply depends on its structure. Similar to MOSFET, CNTFET has three terminals; source, drain and gate[4]. The gate terminal will electrostatically turn on or off the transistor. Nanotube in CNTFET acts as channel in MOSFET and electrons are conducted inside of that. Based on their operation, there are two types of carbon nanotube transistors[4]. The first type is schottky barrier CNTFET transistor. Source and drain junctions are metal and transportation of electrons occurs by tunneling through a Schottky barrier at the source-channel junction .These transistors use direct contact of the metal with the nanotube in their fabrication process; hence they have Schottky Barrier at the metal Nanotube junction[5] . The barrier width is modulated by the application of gate voltage and thus the

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transcondutance of the device is dependent on the gate voltage[5] .The second type is ballistic CNTFET. In ballistic CNTFET the channel is intrinsic, where source and drain are doped . An electrostatic potential barrier, prevents flowing electrons through the channel. By a positive gate voltage the barrier is passed down and current will flow across the semiconducting nanotube, hence ballistic CNTFET is more appropriate for MOSFET like CNTs.

A. Ballistic SWCNT Model:

Single-wall Carbon nanotube (or SWCNT) consists of one cylinder only, and are the most promising type for use as a transistor. An SWCNT can act as either a conductor or a semiconductor depending on the angle of the atom arrangement along the tube. This is called the chirality vector and is represented by the integer pair (n, m). If n-m is not a multiple of 3 then it is semiconducting carbon tube. The diameter of the CNT can be calculated as follows[2]:

$$D_{CNT} = \frac{\sqrt{3}\, a_0}{\pi} \sqrt{n^2 + nm + m^2} \tag{1}$$

where $a_0 = 0.142$nm is the inter-atomic distance between each carbon atom and its neighbour. Fig.1 shows the schematic diagram of a CNTFET[2]. Similar to the traditional silicon device, the CNTFET has also four terminals. A dielectric film is wrapped around a portion of an undoped semiconducting nanotube, and a metal gate surrounds the dielectric. Heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance during the on-state[6] . As the gate potential increases, the device is turned on or off electrostatically via the gate.
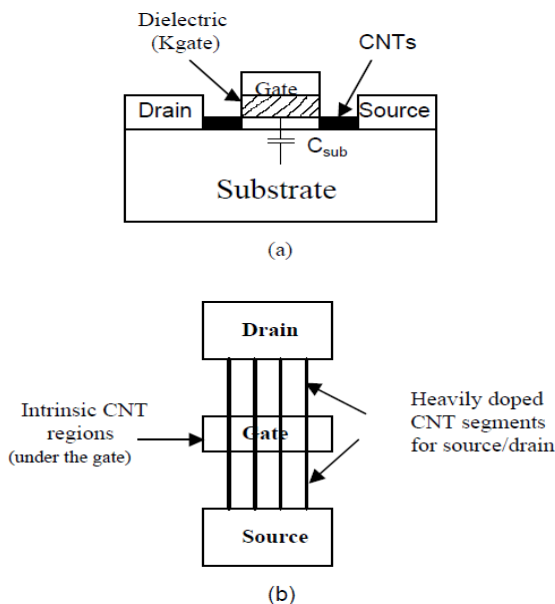

Fig 1 Schematic Diagram of a Carbon Nanotube Transistor:(a) Cross sectional view (b) Top view.

B. Threshold Voltage:

The threshold voltage is defined as the voltage required to switch on a transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap that is an inverse function of the diameter[2] :

$$V_{TH} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\, \frac{aV_\pi}{eD_{CNT}} \tag{2}$$

Where a = 2.49 Å is the carbon to carbon atom distance, V_π = 3.033 eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. Since D_{CNT} of a (19, 0) CNT is 1.49 nm, the threshold voltage of a CNTFET using (19,0) CNTs as channels is 0.289 V from Equation (2). Simulation results confirmed this threshold voltage.

C. Current-Voltage Characteristics:

The current-voltage (I-V) characteristics of the ballistic CNTFET are in close relation to the band structure of a CNT. The energy band of the CNT consists of many subbands. As the drain bias of the CNTFET increases, the drain Fermi level is depressed to traverse a sub-band minimum and the current increase occurs between the drain and source. When the drain Fermi level is below the lowest sub-band bottom, the current saturates[7].

Fig.2 shows the I-V characteristics of the ballistic CNTFET with different channel lengths , at the power supply of 0.9V and room temperature.The I-V characteristics of the CNTFET are similar to that of the MOSFET, which makes the CNTFET a good candidate for current MOSFET based VLSI designs. The current of the CNTFET can be increased by increasing the number of tubes in a CNTFET. As shown in Fig.2 the current level of the CNTFET decreases with channel length (when the channel length is very short) due to the energy quantization in the axial direction (as limited by optical phonon scattering).
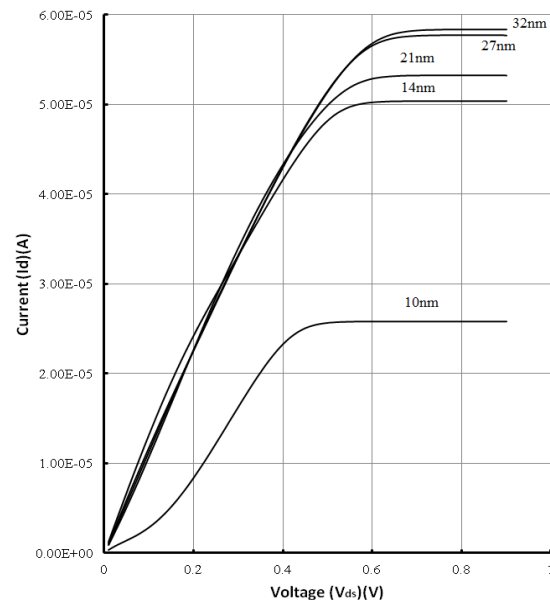

Fig. 2 Current- Voltage Characteristics of a Ballistic CNTFET

III. CURRENT MIRROR

Current Mirror is used for generating single or multiple-replica of an input current. Besides its conventional function as current copier, it is used to convert source to sink current and vice versa. Current mirror is a primitive element in Multiple Valued Logic (MVL) circuits and it is used to implement many other circuits. Thus, the realization of high performance current mirror will result a high performance MVL circuit. There are different types of current mirrors to increase the speed, decrease power consumption and temperature stability. Based on aspect ratio, the output current can be: same as input, multiplication or reverse sign of input current. Different ratios of input current can be received on output by using proper ratio values in a simple current mirror. There are several types of current mirrors. They are represented from classic one to high speed low voltage. Fig.3 shows classic current mirror. As a result of the connection between gate and source of M1 , $V_{DS1}= V_{GS1} = V_{GS2}$.
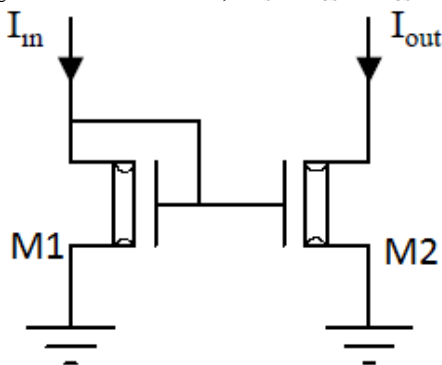

Fig. 3 Simple Current Mirror with CNTFET

Smaller channel lengths tend to introduce non-idealities in conventional DC biasing schemes designed at 32nm causing unstable biasing currents etc. Consequently, device mismatches come into picture requiring the mirror transistor widths to be large. In addition, lower widths cause decreased effective channel area below the gate of the MOS transistor (i.e. Cox increases) which in turn increases the power dissipation. A 10µA current mirror is designed using CNTFET. Table I summarizes the results for power supply variations.

TABLE I
VARIATIONS OF PARAMETERS WITH SUPPLY VOLTAGE FOR CNTFET CURRENT MIRROR

Vdd	0.9V	0.8V	0.7V
Minimum Voltage V_{min}(V)	0.324	0.328	0.336
Output Current I_{out}(µA)	10	10	10
Power Dissipation(µW)	7.75	7.79	7.87

For arbitrary specified widths and default values of CNT pitch and diameter in addition to the adjustment of effective channel length (Leff) to 12.6nm to compare fairly with 32nm CMOS technology in terms of device geometry, the number of tubes required is fixed to 3 and Current Mirror parameters are reported in Table I for different values of operating voltages. We find that the reduction in supply voltage 'Vdd' significantly increases the power dissipation and minimum voltage. Hence a selection of 0.9V is made on the basis of overall performance.

IV. PERFORMANCE COMPARISON OF CNTFET WITH MOS TECHNOLOGY DESIGN

CNTFET shows the potential to sustain Moore's law in the nearby future because of its good similarity with CMOS and capability to reduce the leakage power with continued scaling. For simulation purposes, we have used BSIM v4.6.1 BPTM models[8] of MOSFET at 32nm using HSPICE. High performance Stanford model[2] is used which successfully accounts for CNTFET practical non-idealities, such as scattering, effects of the source/drain extension region, and inter-CNT charge screening effects etc. apart from accurate predictions of dynamic and transient performance with more than 90% accuracy . In our analysis, we have used top gated undoped semiconducting (19, 0) MOS-CNFETs with 4nm thick HfO2, high-k dielectric (k=16).

TABLE II
PERFORMANCE COMPARISON OF CNTFET BASED CURRENT MIRROR WITH MOSFET AT 32NM NODE

Model	Minimum Voltage V_{min} (V)	Output Current I_{out} (µA)	Output Resistance (KΩ)	Power dissipation (µW)
MOSFET	0.549	9.7613	3	10.259
CNTFET	0.324	10	117	7.75
CNTFET (19,3)	0.315	10	117	7.31

Simulation results obtained show that CNTFET based Current mirror outperforms the MOS Mirror in various parameters like 97% increase in output resistance,24% decrease in power dissipation and 40% decrease in minimum voltage required for constant saturation current as shown in Table II . For better comparision, simulation plots showing DC response for CNTFET and MOSFET are shown in Fig 4.
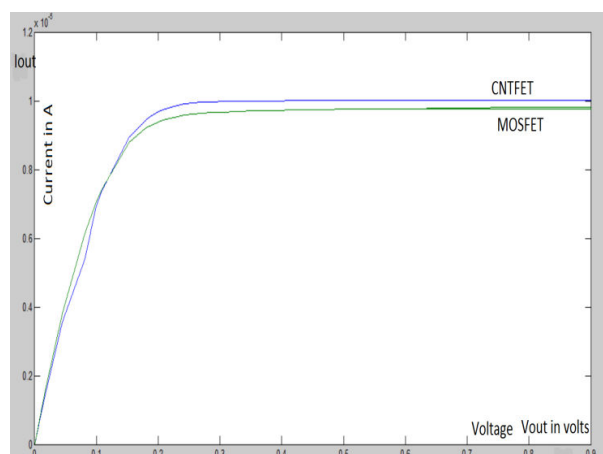

Fig. 4 DC Output Characteristics of Current mirror

A. Effect of Chirality Vector on characteristics

The diameter of the CNTFET depends on the chirality vector. The threshold voltage can be reduced by increasing the diameter. If the threshold voltage is reduced then the CNTFET can be made to work at lower supply voltages, thus reducing the power dissipation. In order to show this effect we have taken CNTFET with chirality vector of(19,3) into consideration. Almost 6% decrease is observed in power dissipation on increasing the chirality, the results are depicted in Table II. Furthermore, a decrease in the minimum voltage required to attain saturation current has been noticed. The DC output characteristics of CNTFET with modified chirality vector are shown in fig 5.
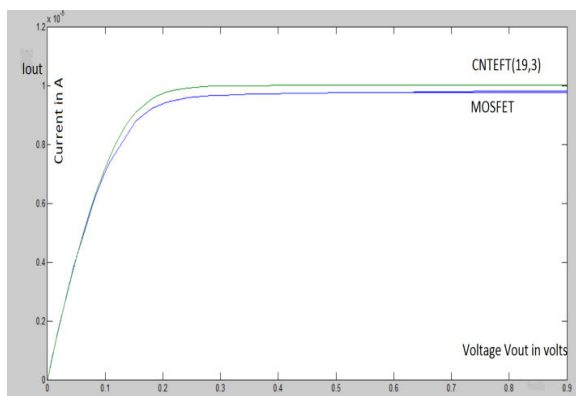

Fig. 5 DC Output Characteristics of Current Mirror with CNTFET of (n,m) = (19,3)

Simulations are carried out with other current mirror circuits like Wilson current mirror and Regulated Cascode current mirror. In these simulations, the supply voltage and reference current source are fixed to 0.9V and 10μA respectively. The chirality vector of CNT is taken as (19,0) and values are tabulated in Table III.

TABLE III
PERFORMANCE COMPARISON OF CNTFET BASED CURRENT MIRRORS WITH MOSFET AT 32NM NODE

Model		CNTFET	MOSFET
Wilson Mirror	$V_{min}(V)$	0.513	0.783
	$I_{out}(\mu A)$	10	9.05
Regulated Cascode Mirror	$V_{min}(V)$	0.531	0.675
	$I_{out}(\mu A)$	9.998	9

V. CONCLUSION

We have investigated the use of MOSFET -like CNTFET in the current mirror design. It has been observed that carbon nanotube current mirror show better stability and performance than MOSFET circuits . It is also shown that variation of chirality could produce much better results. On comparision of both the circuits , there is noticable decrease in minimum voltage, increase in output resistance and decrease in power dissipation of CNTFET. Through a detailed technology assessment, this paper demonstrates that the CNTFET design is a vaible candidate for analog design in nano scales.

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