

Nuclear medical image treatment system based on FPGA in real time

B. Mahmoud, M.H. Bedoui, R. Raychev and H. Essabbah

Abstract— We present in this paper an acquisition and treatment system designed for semi-analog Gamma-camera. It consists of a nuclear medical Image Acquisition, Treatment and Display chain (IATD) ensuring the acquisition, the treatment of the signals (resulting from the Gamma-camera detection head) and the scintigraphic image construction in real time. This chain is composed by an analog treatment board and a digital treatment board. We describe the designed systems and the digital treatment algorithms in which we have improved the performance and the flexibility. The digital treatment algorithms are implemented in a specific reprogrammable circuit FPGA (Field Programmable Gate Array).

Keywords—Nuclear medical image, scintigraphic image, digital treatment, linearity, spectrometry, FPGA.

I. INTRODUCTION

The evolution in the technology of the integrated circuit contributes to a migration of the Gamma Camera designed towards simpler and more preferment ones. Most recent are the digital cameras where the digitalization is done directly on each Photomultiplier's (PM) output (local event detection). The former generation which continues to equip much nuclear medicine clinical is known as hybrid camera. It is an "Anger pseudo-camera". We haven't access to the PM output signal but to a signal resulting from a signals' summation of all the PMs (total event detection) [1]. In this category we distinguish, according to the treatment held by the electronics of the Detection Head (DH), two types of Gamma Cameras. In the first, called analog gamma camera, the DH generates two position signals (X , Y) and an energy signal (E), all analogical. In the second, called semi-analog gamma camera, the DH generates an energy signal (E) and four position signals (X^+ , X^- , Y^+ , Y^-), all analogical.

To make this generation profit from the hybrid camera of advanced data-processing tools for images treatment without calling to an acquisition station suggested high-cost by the constructor and provided with closed software, we make an

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interface for semi-analog cameras of Sopha Medical Vision (SMVi) by taking as example SOPHY DS7. The developed system consists of an Image Acquisition, Treatment and Display (IATD) ensuring the acquisition and the treatment of the signals resulting from the DH. The developed chain is formed by a treatment analog board and a digital treatment board designed around a DSP [2]. In this paper we have presented the architecture of a new version of our chain IATD in which the integration of the treatment algorithms is executed on an FPGA (Field Programmable Gate Array) circuit.

II. MATERIALS AND METHODS

A. System's architecture

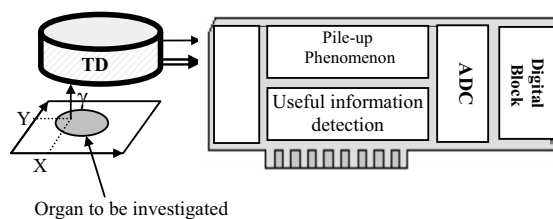


Fig. 1. System Architecture

The architecture of the whole system is given in figure 1. The DH is the element to be preserved in the system. It is equipped with a NaI(Tl) crystal (5/8 inches in thickness and 15.5 inches diameter) coupled to 63 PM and an analysis of electronics. Five signals are delivered in the output. An energy signal E and four position signals (X^+ , X^- , Y^+ , Y^-).

The analog board consists of four parts (fig. 1):

- A part of gain and offset compensation: It enabled us to align all five signals on a base line and to adapt the analog signal amplitude to the analog/digital conversion range.
- A part of event detection and useful information localization: our solution, known as "vertical", is based on the exploitation of the amplitude component of the pulse, without utilizing the time component.
- A part of pile-up pulses treatment: the traditional solution for the treatment of the pile-up phenomenon consists of a spectrometric analysis and a rejection of the resulting pulse. Our solution consists of a detection of the first pulse which has occurred and a rejection of the second piled up pulse.
- A part of analog/digital conversion: we choose a systematic conversion of the five signals without condition of belonging

to the maximum of the energy signal to a spectrometric window (Sw) preset.

The digital board ensures the acquisition of the signals resulting from the DH, the treatment and the image reconstruction. We describe a configuration based on an FPGA circuit.

B. Digital board based on an FPGA circuit

We developed a specific circuit of elementary treatment to the nuclear medical images. It is designed around an FPGA circuit (figure 2). It ensures the spectrometric analysis algorithm, the position calculation algorithm, the linearity correction algorithm and the communication with the PC. The whole algorithms are executed in real time and in parallel way during the scintigraphic image construction.

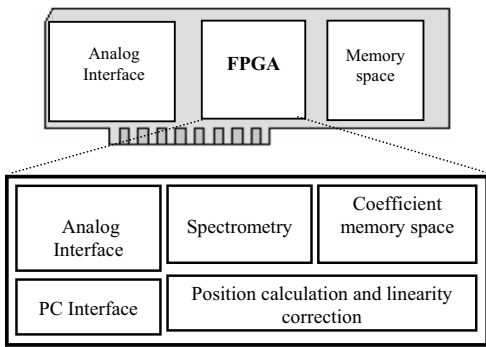


Fig. 2. Digital board design

This circuit has an important resource memory for the storage of the correction and calibration matrices. The modeling of the used algorithms is made by the VHDL language with the Foundation 3.1 tool of Xilinx. The circuit functions with a frequency of 25 MHz which makes it possible to reach a counting rate higher than 500 Kcps. This circuit is extensible, allows the updating of the integrated algorithms. The FPGA circuit used is a Spartan XCS40 of the Xilinx family.

B.1. Spectrometric analysis

We choose a step which leaves to the user the possibility to fix the spectrometric windows number (Sw_n) and to choose the analysis method. The study of the belonging of the signal to the various windows is implemented and executed in parallel on the FPGA circuit.

$$\begin{cases} \text{If } E \in Sw_0 \cup Sw_1 \cup \dots \cup Sw_{n-1} \Rightarrow \text{event accepted} \\ \text{If } E \notin Sw_0 \cup Sw_1 \cup \dots \cup Sw_{n-1} \Rightarrow \text{event rejected} \end{cases}$$

B.2 Position calculation algorithm

The pixel co-ordinates (X, Y) of the image matrix are defined by the following formulas [4]:

$$X = k \frac{X^+ - X^-}{X^+ + X^-} \text{ and } Y = k \frac{Y^+ - Y^-}{Y^+ + Y^-} \tag{1}$$

Where K is a weight factor.

The X and Y calculation is done in parallel in the FPGA circuit (fig. 3).

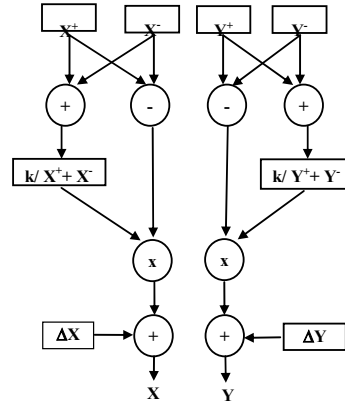


Fig. 3. Position calculation and linearity correction algorithms

To minimise the number of gate used in the FPGA circuit and to reduce the execution time of this algorithm we transform the calculation operation of (k/ X⁺+ X⁻) and (k/ Y⁺+ Y⁻) to a simpler access data memory table. The memory is implemented in the FPGA circuit and configured on the startup of the system.

B.3. Linearity correction algorithm

The geometrical linearity is the aptitude to restore the exact shape of an object. A bad linearity introduces a deformation of the image. In our chain the correction on X and Y is applied in real time for each event detected. Two tables of linearity correction (x and y) for all the X and Y values are beforehand definite and loaded in two storage blocks in FPGA circuit (fig. 3). The corrected co-ordinates (X', Y') of the event impact are given by the following relation:

$$X' = X \pm \Delta x \quad \text{and} \quad Y' = Y \pm \Delta y \tag{2}$$

C. Software

The developed software (in Visual C++) for the IATD chain consists of tow parts: the hardware driver and the user interface. The first allows the configuration and the calibration of IATD, the acquisition and the co-ordinates filtering of the pixel and the data acquisition spectrometric. The second ensures visualization, the treatment and the filing of the images in a preset format.

III. RESULTS

A. Analog treatment

The stages of gain and offset compensation functions with a band-width of 160Mhz, conversion is done with a resolution of 8 bits and a sampling rate of 1Mhz. The dead time for this board is 2 μ s, which authorizes a maximum counting rate of 500Kcps. The analog treatment of the piled up pulses enabled us to avoid the losses related to this phenomenon with a rate of success of 46.8% [2].

B. Digital treatment

The digital part, designed around FPGA circuit, ensures the signals treatment (position calculation, spectrometry, linearity) in real time and the data transfer towards the PC where the image construction is assured. The chain IATD functions in order to execute the acquisition and treatment in the parallel way. Table 1 gives the execution time value for each used algorithm on FPGA circuit. Let us note that the analog treatment time is higher than the total execution time of the various Digital parts.

C. Software

The software ensures the starting configuration, the signals acquisition and treatment of the event detected. It fixes the acquisition time or the count rate per image and the spectrometric windows. It allows the visualization and the safeguard of the image and the acquired spectrum.

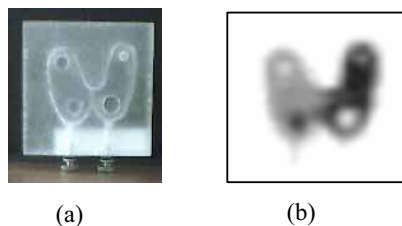


Fig. 4. (a) thyroid phantom;
(b) Scintigraphic image acquired by the system.

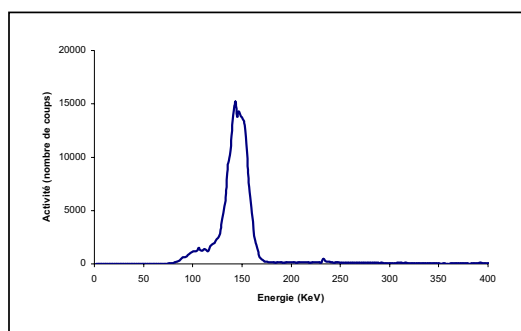


Fig. 5. The Technetium 99m spectrum

We make the scintigraphic image of a thyroid phantom one which makes it possible to model the demonstrations anomalies, namely a hot nodule and a cold nodule and two areas with reduced activity (fig. 4a). The image is made with an activity of 7.2 MBq of technetium 99m. The DH provided

with a collimator low energy high resolution, is placed at 7cm of the phantom acquisition and executed during 2mn in the 128*128 matrix form. The scintigraphic image of this phantom, obtained by our system, is given by the figure 4b. The spectrometry recorded by our system is reported in figure 5.

IV. DISCUSSION

The analog board provides the function requested by using components large band width and from low noise. This allows it to minimize the noise without increase in the dead time. The energy and amplitude of the various signals linearity is checked [2].

The pile-up phenomenon generates a loss of information and increases the dead time of gamma camera. The solutions described for the analysis of the pile up phenomenon are to be ignoring the piled up pulses from where loss in counting is to use calculation methods at important response time [4]. In digital gamma camera, management PM by PM of the signals makes it possible to take into account only two sufficiently distant simultaneous events [5].

Our solution, not only makes it possible to reduce the loss by 46.8% in counting rate, but also it avoids the increase in the dead time [2].

The digital part is designed so that it allows flexibility in treatment algorithms integration. The user has the possibility to fix the spectrometric windows number and to choose the analysis method without risk to increase the dead time or to add other components to the system. Various approaches can be adopted, the window traditional method of 20%, the method of window of Jaszak (JAS) [6], method of triple window (TEW) [7-8]. The use of an FPGA circuit made it possible to carry out the treatment algorithms very continuously to acquire the analogical signals. This parallel solution allowed us the treatment, the correction and the calibration of Gamma Camera in real time without increasing the dead time of the system and without loss in count rate. Table 1 reports the execution times of the various algorithms integrated on the old configuration based on a DSP (TMS320c6x)[2] and on the news designed around the FPGA.

TABLE 1

EXECUTION TIME OF THE VARIOUS ALGORITHMS FOR THE TWO CONFIGURATIONS: DSP AND FPGA

		Execution time (μ s)	
		DSP	FPGA
Digital treatment algorithm	Data Collection	0.26	0.24
	Spectrometry (1 window)	0.15	0.03 (n Windows)
	Position calculation	0.25	0.42
	Linearity correction	0.20	0.017
	Data transfert	0.54	0.54
Total (μ s)		1.4	1.247

The developed software provides the functions required to fix the acquisition parameters, to visualize, treat and safeguard the image. It allows, contrary to the acquisition

stations suggested by the constructor, to follow the evolution of the tools for treatment data-processing. The comparative analysis of the thyroid phantom images realized by our system and SOPHY DS7 (SMVi), suggests the need for improving the linearity correction and the use of treatment algorithms.

V. CONCLUSION

We realized an acquisition system of the signals resulting from the detection head of hybrid gamma camera SOPHY DS7 (SMVi). The developed IATD chain is consisted of two parts, for analog treatment and for digital treatment. It is compatible with bus ISA of the PC. The operation parallel of the analog part and the digital part enabled us to reach count rates comparable so not greater than those proposed by the constructor. The realized system provides the functions required by the implementation of original solutions.

The main board is extensible hardware and software side. The use of re configurable circuits of type FPGA enabled us to increase the total performances of our system. Adequate digital filters can be established. A parallel execution of various tasks, spectrometry or methods of analysis and correction, can be ensured by these programmable circuits.

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