# A new Configurable Decimation Filter using Pascal's Triangle Theorem

A. Chahardah Cherik, E. Farshidi

*Abstract*—This paper presents a new configurable decimation filter for sigma-delta modulators. The filter employs the Pascal's triangle's theorem for building the coefficients of non-recursive decimation filters. The filter can be connected to the back-end of various modulators with different output accuracy. In this work two methods are shown and then compared from area occupation viewpoint. First method uses the memory and the second one employs Pascal's triangle's method, aiming to reduce required gates. XILINX ISE v10 is used for implementation and confirmation the filter.

*Keywords*—Decimation filter, sigma delta, Pascal's triangle's theorem, memory

## I. INTRODUCTION

DECIMATION filters are widely used in sigma-delta ($\Sigma\Delta$) modulators to design high accuracy analog to digital (A/D) converters. A simple form of these filters is presented by Hogenauer [1]. As about the half part of these filters works in high frequency, using of this filters in not suitable for the systems that need low power consumption. For achieving the low power systems, polyphase decomposition is used to reduce the input frequency [2]; non-recursive topology is used for reducing the input frequency in each step [3]. In some purposes with changing in structure of the hardware, filter can occupy less space besides the reducing the input frequency. The main drawback of the all decimation filter is that each filter can be connected to a specific $\Sigma\Delta$ modulator, because the specifications of these filters are not adjustable. In this paper, a new decimation filter that is usable for wide range of $\Sigma\Delta$ modulators is presented by employing Pascal's theorem.

The paper is organized as followed: Section 2 is reviewing some theorems of decimation filters and Pascal's triangle. In section 3, the multipurpose decimation filter is addressed in details. Simulation results are presented in section 4.

## II. BASIC PRINCIPLE

### A. Two-quadrant squarer/divider

$\Sigma\Delta$ converters have two main parts: one of them is modulator at the front-end of converter and another one is decimation filter at the back-end of converter.

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Generally, $\Sigma\Delta$ modulator has one bit stream output and decimation filter has one bit input and multi bits output. A $\Sigma\Delta$ is used as a method for providing the output of the analog to digital converter. This goal is achieved by encoding high resolution signals into lower resolution signals using pulse-density modulation. These kinds of modulators are based on oversampling method. This means that sampling frequency is much higher than input signal's frequency. The input of filter will be connected to the output of $\Sigma\Delta$ modulator to form A/D converter. The digits number of the output of decimation filter is related to the order of $\Sigma\Delta$ modulator.

The transfer function of simple form of decimation filter in general form is:

$$H(z) = \left( \frac{1 - z^{-M}}{1 - z^{-1}} \right)^N = \left( 1 - z^{-M} \right)^N \times \left( \frac{1}{1 - z^{-1}} \right)^N \qquad (1)$$

where M is down sampling ratio (DSR) and *n* is the order of filter. Figure 1 shows block diagram of the filter based on (1).
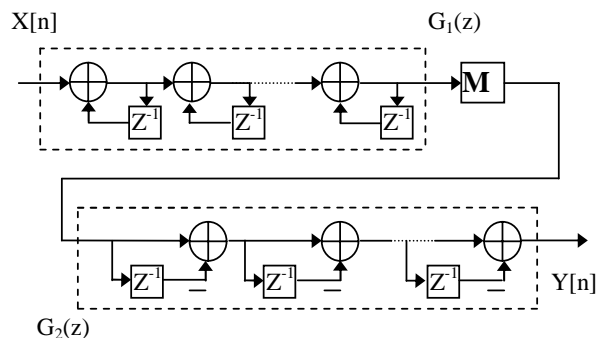


Fig. 1 Decimation filter

This filter has some integrators with infinite impulse response (IIR), differentiators with finite impulse response (FIR) and one down sampler. The IIR part is $G_1(z) = \left( 1 - z^{-M} \right)^N$ and the FIR part is $G_2(z) = \left( \frac{1}{1 - z^{-1}} \right)^N$

For having the stability, the minimum word length of input of decimation filter should be [4]:

$$B_{out} = B_{in} + N \log_2 M \qquad (2)$$

The $B_{in}$ is the bit-number of the output of the $\Sigma\Delta$ modulator, N is order of the filter, or the number IIR and FIR filters and M is the down-sampling ratio.

## B. Pascal's triangle

One of the mathematical theorems that presents by Pascal is relationship between the order of binomial expression and the coefficient of that expression when it's powered by its order [5]. Assuming $z(x, y) = (x + y)^N$ for binomial expression, some of these equations are presented as:

$$N = 1 \quad \rightarrow \quad z(x, y) = x + y \tag{3a}$$

$$N = 2 \quad \rightarrow \quad z(x, y) = x^2 + 2xy + y^2 \tag{3b}$$

$$N = 3 \quad \rightarrow \quad z(x, y) = x^3 + 3x^2 y + +3xy^2 + y^3 \tag{3c}$$

$$N = 4 \quad \rightarrow \quad z(x, y) = x^4 + 4x^3 y + 6x^2 y^2 + 4xy^3 + y^4 \tag{3d}$$

Figure 2 shows a Pascal triangle that shows the coefficient of the various orders. In this triangle, each row expresses coefficients of different binomial expressions. The basic of this triangle is that the summation of two sequentially coefficient in each row will make corresponding coefficient of lower row. For example in code $N = 3$ for making the code 3, the upper codes 1 and 2 must be added.



Fig. 2 The Pascal's triangle

## III. CONFIGURABLE DECIMATION FILTER

### A. Main block

It can be shown that the non-recursive form of (1) is obtained as [5]:

$$H(z) = \left( \sum_{i=0}^{M-1} z^{-i} \right)^N = \left( 1 + z^{-1} + \dots + z^{-(M-1)} \right)^N \tag{4}$$

Aiming to preparation of binomial expression, in this paper M is chosen 4 (M=4). In such case (4) will be converted to:

$$H(z) = \left( 1 + z^{-1} + z^{-2} + z^{-3} \right)^N \tag{5}$$

If the H(z) is separated, the equation (5) will be converted:

$$H(z) = \left( 1 + z^{-1} \right)^N \left( 1 + z^{-2} \right)^N \tag{6}$$

Now, each of these parts ( $\left( 1 + z^{-1} \right)^N$ and $\left( 1 + z^{-2} \right)^N$ ) can be used for achieving the Pascal's triangle's theorem. The block diagram of equation (6) is presented in Figure 3.
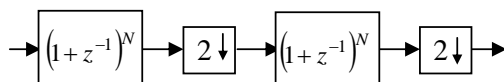


Fig. 3 Non-recursive decimation filter

The proposed filter has 4 main blocks; two FIR blocks and two down sampling blocks. First down sampler is used to satisfy the power of the second part of right hand side of (6), and the second one is used to content the DSR (M=4). As the input has 1 bit ($B_{in}$=1), decimation factor is M=4 and the order of the filter is N, the number of output bits ($B_{out}$) will be:

$$B_{out} = 1 + N \log_2 4 = 1 + 2N \tag{7}$$

For having the wide range of output can be achieved by choosing appropriate N. Table 1 shows output bits for different N.

TABLE I
RELATIONSHIP BETWEEN $N$ AND $B$

| N | $B_{out}$ |
|---|---|
| 4 | 9 |
| 5 | 11 |
| 6 | 13 |
| 7 | 15 |
| 8 | 17 |

The configurable decimation filter consists of two main parts. One of them is the FIR filter that has delays, adders and multipliers. Another one is the block of the coefficient builder that makes the coefficient for first part depends on the accuracy of ΣΔ modulator that connected to this decimation filter. First part for this purpose is shown in Figure 4.
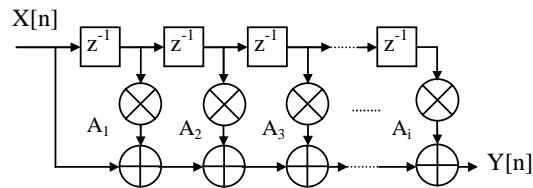


Fig. 4 The half of Main FIR filter

### B. Coefficient builder

As mentioned before coefficient builder block makes the coefficients for the main FIR part. In the traditional one, these coefficients can be stored in the memory which we call it memory method. For achieving this purpose the coefficients can be stored as shown in Table 2. In this table, the coefficients are shown for different N. For realization this block, some multiplexers are needed. Each coefficient needs a multiplexer. The size of these multiplexer depends on the maximum length of the coefficient in each column. For $A_1$, this multiplexer block is shown in Figure 5.

TABLE II
THE STORED COEFFICIENTS

| N | Const. | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 2 | 1 | 0 | 0 | 0 | 0 |
| 3 | 1 | 3 | 3 | 1 | 0 | 0 | 0 |
| 4 | 1 | 4 | 6 | 4 | 1 | 0 | 0 |
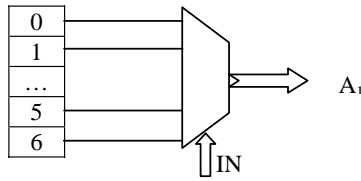
Fig. 5 Selecting coefficient $A_1$

In this paper a new method for building the coefficient that uses the basic of the Pascal's triangle is presented. As it's mentioned in section 1.2, for making each coefficient, two corresponding sequentially coefficients will be added; so in our proposal, preparation of each coefficient has been done by just one adder plus one register to store the coefficient for each coefficient. Figure 6 shows the proposal coefficient builder.
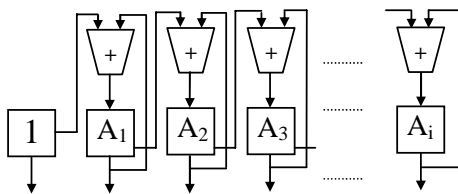


Fig. 6 The block diagram of Pascal's method

The sequences that needed to obtain coefficient is as following. In the initialization time all coefficients ($A_i$) are zero. Constant coefficient, 1, is the source of making coefficients after passing some clocks. When first clock occurs, constant 1 will be added to 0 from the $A_1$ and will be stored in the $A_1$ again. In the second clock, 1 in $A_1$ will be added with the 0 in $A_2$ and $A_2$ becomes 1. Constant 1 adds with the 1 that was stored in $A_1$ and makes it 2. Continually clock time can increment this coefficient by each clock. So, the number of clock depends on the coefficients that filter needs. For example for building the filters with coefficients 1-5-10-10-5-1 the coefficient builder needs 5 clocks.

The advantage of the proposal method is that the consumed chip area of the new method is fewer than the memory method. Because in Pascal method by adding a digit, one register and one adder will be added but in memory method a new registers with one more digit number with respect to the former digits is needed. It can be concluded that by increasing the order of the filter the difference of the required memory size will be increased. Figure 7 shows this difference.



Fig. 7 The effect of adding one digit in memory method (a) and in Pascal method (b)

## IV. SIMULATION RESULTS

For implementation and comparison between memory method and the proposal Pascal method the XILINX ISE v10 is used. In Figure 8 difference between two methods is depicted. It can be seen from this Figure that for the filters that have the length more than 6-bit ($B_{out}>6$), the Pascal method requires fewer gate rather than traditional memory method.
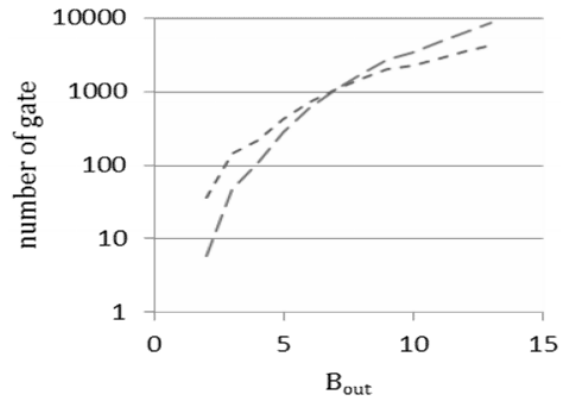


Fig. 8 Difference in number of gate versus output bit ($B$)
$- -$ Pascal method          $-\!-$ Memory method

As the most $\Sigma\Delta$ modulator needs much upper bit number than 6, so this architecture can be helpful for these modulators. As it is mentioned before for building coefficients, some clock is needed. For example for N=5, 5 clocks should pass. Figure 9 shows these changes in coefficient to produce the filter one. From this figure, it can be seen that after 5 clocks, filter's coefficients, 1-5-10-10-5-1, have been made. First clock occurs at times 250ns, and the fifth one at 650ns. After this time expected coefficients are obtained.
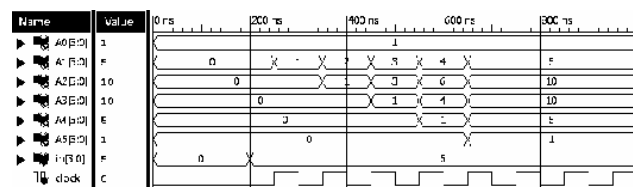


Fig. 9 Filter coefficients during building

## V. CONCLUSION

In this paper a novel non-recursive decimation filter is presented. This filter can be implemented with the coefficients employing Pascal's theorem for building these ones. The filter has main block and coefficient builder. This filter can joined with wide range of $\Sigma\Delta$ modulators because the architecture of the filter can save the cost.

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