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A Low-Voltage Current-Mode Wheatstone Bridge using CMOS Transistors

Ebrahim Farshidi

***Abstract*—**This paper presents a new circuit arrangement for a current-mode Wheatstone bridge that is suitable for low-voltage integrated circuits implementation. Compared to the other proposed circuits, this circuit features severe reduction of the elements number, low supply voltage (1V) and low power consumption (<350uW). In addition, the circuit has favorable nonlinearity error (<0.35%), operate with multiple sensors and works by single supply voltage. The circuit employs MOSFET transistors, so it can be used for standard CMOS fabrication. Simulation results by HSPICE show high performance of the circuit and confirm the validity of the proposed design technique.

***Keywords*—**Wheatstone bridge, current-mode, low-voltage, MOS.

I. Introduction

WHEATSTONE bridge has found widespread use in the instrumentation and measurement systems for sensing strain, temperature, pressure, force, displacement and humidity [1-4]. Voltage-mode Wheatstone bridge (VMWB) offers a good method for measuring small resistance changes accurately. Recently, a method based on the circuit duality concept [5] has been proposed to develop a current-mode Wheatstone bridge (CMWB) [6]. It is based on the use of current-mode as an alternative to conventional voltage-mode Wheatstone bridge. It has the following advantages: It uses the principle of superposition without adding any signal conditioning circuitry. Also, it has a smaller area because it reduces the sensing passive elements, and uses only two resistors without degradation in the performance. The new CMWB has a much-improved common-mode cancellation; furthermore, it has a high accuracy [6]. Following this technique Some CMWB designs based on the second-generation current conveyors (CCII) [7] and operational floating current conveyor (OFCC) [8] to implement a CMWB have been proposed [6, 9, 10 , 11]. The main drawbacks of theses proposed circuits are as follows: firstly, the extra needed circuits lead to a large number of transistors and high power consumption; secondly, most of them are area-intensive, due to the use of more circuitry and additional resistors for balance networks and also for linearization;
Thirdly, they need two separate supply voltage; and finally, the proposed circuits are based on the bipolar transistors. However, the need for low-voltage/low-power CMOS analog circuits is growing due to the downscaling of CMOS processes and also, in many situations, particularly in the mixed analog-digital systems, it is desirable to implement the circuits in the MOS technology [12].

In this paper, a new CMWB design to overcome the above problems is presented [13]. The circuit is designed in CMOS technology, which exhibits flexible characteristics with respect to other CM or VM devices, Its main features are reducing circuit elements, area efficient implementation, operation in single supply voltage, current output signal and possibility of low-voltage and low-power due to the fact that MOS transistors are employed.

The paper is organized as follows. In section 2, basic principle of Wheatstone bridges is presented. In section 3, the circuit design of the proposed CMWB is proposed. Section 4 explains the new linearization technique. Simulation results are presented and discussed in section 5 and concluding remarks are provided in section 6.

II. Basic Principle Wheatstone Bridges

A. Voltage-mode Wheatstone bridge

Traditionally, the voltage-driven Wheatstone bridge configuration is used for the measurement of small resistance changes. It consists of four resistors connected in a quadrilateral form in addition of an excitation voltage connected across one diagonal of the bridge. The output voltage of the bridge is measured differentially between the voltage divider outputs connected across the other diagonal. The deviation of one or more resistors in the bridge from a nominal value is measured as an indication of change in the measured physical variable, and the output voltage across the bridge indicates the resistance change. The bridge can have one, two, or four resistors, whose values are deviated with the applied physical variable, as shown in Fig. 1. Typically, in sensor applications, the nominal values of four resistors are chosen to be equal. The differential output voltage and the end-point linearity error of the bridges in Fig. 1 are summarized in Table 1, where V_{ref} is the excitation voltage to the bridge. The linearity error is calculated as the maximum error in percentage full scale from a straight line that connects the origin and the end point at full scale. Table 1 shows that inherent linearity between the resistance variation and the

Ebrahim Farshidi is with the Electrical Engineering Department, University of Shahid Chamran , Ahvaz, Iran, 61357-8313 (e-mail: farshidi@scu.ac.ir).

output voltage variation can be obtained with the all-element and two-element varying configurations in Fig. 1b and Fig. 1c, respectively. However, linearity error is not critical because it can easily be compensated by using software in digital systems [14]. More importantly, to reduce offset and increase the sensitivity of the sensor, the bridge should have accurate resistance matching among resistors and equal absolute resistance variation. These requirements are difficult to achieve in the all-element and two-element varying bridges, not to mention the drawbacks in terms of larger area and cost. The previously mentioned difficulty can be alleviated by using a single resistor as shown in Fig. 1d. One drawback of voltage-driven Wheatstone bridges is that the bridge sensitivity ($S= V_{ref}/(\Delta R/R0)$) is proportional to V_{ref} and inversely proportional to the baseline resistance of the resistors. Therefore, to obtain high sensitivity, large V_{ref} and small resistance are preferred, which prevent low voltage operation and lead to high power consumption of the bridge.

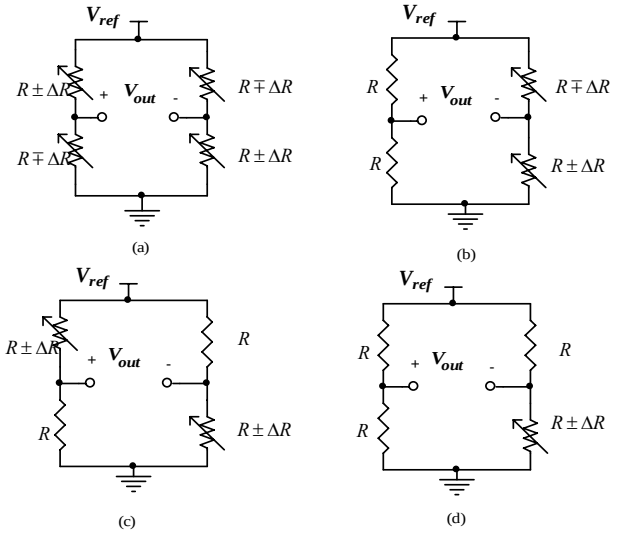


Fig. 1 Conventional voltage-mode Wheatstone bridge configurations

B. Current-mode Wheatstone bridge

One approach to design Wheatstone bridge is based on the use of current-mode as an alternative to conventional voltage-mode Wheatstone bridge [6], which employs the circuit duality concept [5]. A current-mode dual network for the all-element varying Wheatstone bridge is shown in Fig. 2. It is straightforward to show that the current difference, $\Delta I = I_1 - I_2$, is linearly proportional to the change in resistance, ΔR, as shown in Table 1. Due to the circuit duality, the current-mode Wheatstone bridge inherits all characteristics and behavior of its voltage-mode counterpart in the current domain, such as sensitivity, linearity, stability, and so on. The input sensitivity is proportional to the constant excitation current value, I_{ref}.

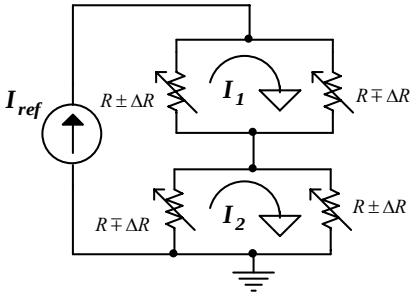


Fig. 2 Current-mode Wheatstone bridge configurations

TABLE I COMPARISON OF WHEATSTONE BRIDGE CONFIGURATIONS

Input configuration	Output voltage or current	Linearity error (%)
Fig. 1a	$V_{out} = \frac{\Delta R}{R} \cdot V_{ref}$	0
Fig. 1b	$V_{out} = \frac{\Delta R}{2R} \cdot V_{ref}$	0
Fig. 1c	$V_{out} = \frac{\Delta R}{2R + \Delta R} \cdot V_{ref} \cong \frac{\Delta R}{2R} \cdot V_{ref}$	0.5
Fig. 1d	$V_{out} = \frac{1}{2} \cdot \frac{\Delta R}{2R + \Delta R} \cdot V_{ref} \cong \frac{\Delta R}{4R} \cdot V_{ref}$	0.5
Fig.2	$\Delta I = I_2 - I_1 = \frac{\Delta R}{R} \cdot I_{ref}$	0

III. CIRCUIT DESIGN OF THE PROPOSED CMWB

This paper proposes a new simplified circuit design for CMWB, employing configuration of Fig. 2. Fig. 3 shows MOS implementation of the proposed CMFB. It uses two sensitive resistors (R1, R2), a constant excitation current (I_{ref}), an operational amplifier (A1) and three current mirrors (formed by transistors M1-M6). One end of both resistors is tied together, while the other end is forced to be equi-potential, that is, $V_X = V_Y$. This can be done by a number of circuit arrangements with second generation current conveyors [5] or operational floating current conveyors [8]. In Fig. 3, the voltage change of node X will mirror a similar change to node Y owing to the virtual short-circuit provided by the operational amplifier A1. It can be shown that the circuit in this Figure exhibits the same properties and behavior as those reported before [5, 8] while severe reduction of the elements number.

From Fig. 3 the currents of sensitive resistors R1 and R2, as the arms of CMWB, are calculated as follows:

$$I_1 = \frac{V_Z - V_X}{R_1} \quad (1)$$

$$I_2 = \frac{V_Z - V_Y}{R_2} \quad (2)$$

in which I_1 and I_2 are the currents of resistors R1 and R2, respectively.

Dividing (1) by (2) and using equation $V_X = V_Y$, it is obtained as follows:

$$\frac{I_1}{I_2} = \frac{R_2}{R_1} \tag{3}$$

Incorporation KCL for nodes (Z) and (OUT) gives:

$$I_{ref} = I_1 + I_2 \tag{4}$$

$$I_{out} = I_1 - I_2 \tag{5}$$

where I_{ref} is the current reference and I_{out} is the output current. Substituting (3) into (4), the currents of resistors R1 and R2 are given by:
By assumption that:

$$I_1 = \frac{R_2}{R_1 + R_2} \cdot I_{ref} \tag{6}$$

$$I_2 = \frac{R_1}{R_1 + R_2} \cdot I_{ref} \tag{7}$$

$$R_1 = R - \Delta R \quad , \quad R_2 = R + \Delta R \tag{8}$$

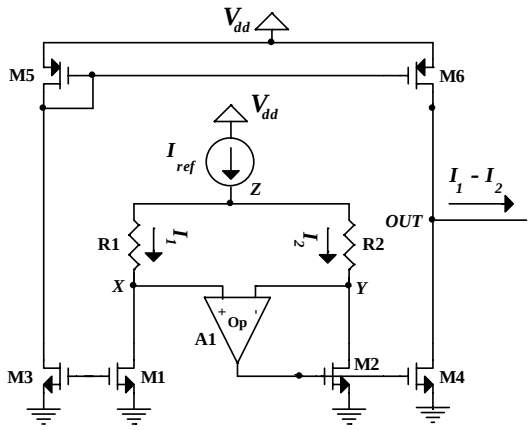


Fig. 3 Circuit diagram of the proposed CMWB

and substituting (6)-(8) into (5), the output current of CMWB in Fig. 3 is obtained as follows:

$$I_{out} = \frac{\Delta R}{R} \cdot I_{ref} \tag{9}$$

in which R is resistance at the reference input signal and ΔR is resistance variation, which change proportional to the signal variation.
The relative resistance variation is defined as:

$$x = \frac{\Delta R}{R} \tag{10}$$

From (9) and (10), the output current in Fig. 3 is linearly related to the relative resistance variation.

As Fig. 3 shows, the number of components in the proposed circuit is much less than those reported before [5, 8]. Also, in this circuit, without degradation in the performance, two resistors are used, so it occupies smaller area. The circuit employs MOS technology, in which the sources of MOS transistors are connected to the substrate, so the body effect is eliminated. The output of the circuit is current signal; therefore, by applying superposition principle, it is possible to add the effects of any number of sensors without adding signal conditioning circuitry. The CMWB circuits in [5, 8] has been performed by current conveyors. These current conveyors operate in double supply voltage, and use stacked translinear loops. However, from Fig. 3, the proposed circuit can operate in single supply voltage, and without extra stacking of transistors that lead to low minimum supply voltage.

IV. Proposed Linearization Technique

In the case, where only one sensitive resistor is used to the variation measuring, i.e.:

$$R_1 = R \quad , \quad R_2 = R + \Delta R \tag{11}$$

then, the output current of Fig. 3 by using of (5)-(9) is given by:

$$I_{out} = \frac{\Delta R}{2R + \Delta R} \cdot I_{ref} \tag{12}$$

From (12) it is evident that the output current causes some nonlinearity [5, 8]. For compensation of nonlinearity, the circuit of Fig. 3 is modified. Fig. 4 shows the proposed linearization circuit. In this Figure, instead of injection current reference I_{ref} into the both resistors R1 and R2, this reference current is only injected into the resistor R2. Therefore the current of resistor R2 is kept constant and can be written as:

$$I_2 = I_{ref} \tag{13}$$

Using (1)-(3) for Fig. 4, the current of resistor R1 in this Figure is related to the current of resistor R2 by (3). Therefore, substituting (11) and (13) into (3), it results:

$$I_1 = \frac{R + \Delta R}{R} \cdot I_{ref} \tag{14}$$

and then, substituting (13) and (14) into (5) the output current

I_{out} is obtained as:

$$I_{out} = \frac{\Delta R}{R} \cdot I_{ref} \qquad (15)$$

From (15) it can be observed that the output current in Fig. 4 is linearly related to the resistance change ΔR.
Evidently, the proposed circuit for linearization technique, shown in Fig. 4, has the same advantages that are described in the preceding section for Fig 3.

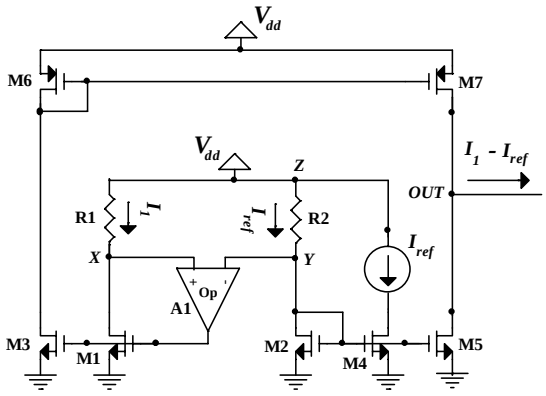


Fig. 4 Circuit diagram of the proposed linearazion technique for CMWB

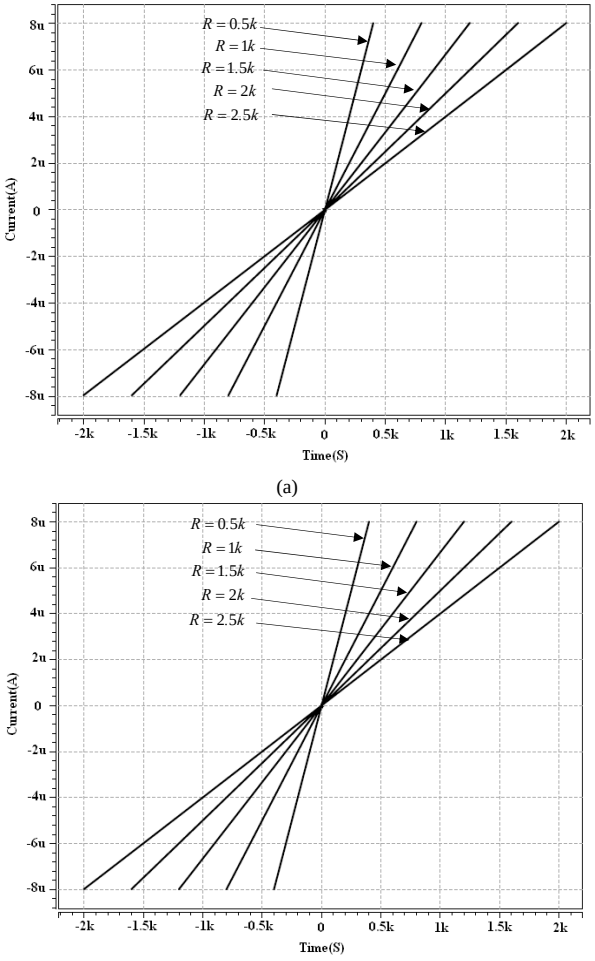
V. Simulation Results

The proposed circuits of Fig. 3 and Fig. 4 were simulated using Hspice with 0.18um TSMC CMOS process parameters. The supply voltage of $1V$ was employed. The aspect ratios of NMOS and PMOS transistors were chosen 10um/2um and 30um/2um, respectively. Fig. 5a and Fig. 5b show the output current versus resistance variation for CMWB in Fig. 3 and Fig. 4, respectively, where the values of reference resistance have been changed from $0.5k\Omega$ to $2.5k\Omega$ in linear variation and with $0.5k\Omega$ steps .In these Figures, relative resistance variation were changed from -80% to +80% and the value of current reference I_{ref} was set to $10uA$.

From these Figures, we can observe a linear dependence of output current versus resistance variation for different values of reference resistances.

In a similar way, in Fig. 6a and Fig. 6b the output current against relative resistance variation for CMWB in Fig. 3 and Fig. 4 are shown at five different values ranging from *2uA* to *10uA* in linear variation. In these simulations the value of reference resistance R was set to $1k\Omega$. From these Figures, it can be seen a linear dependence of output currents versus resistance variation for different values of reference current.

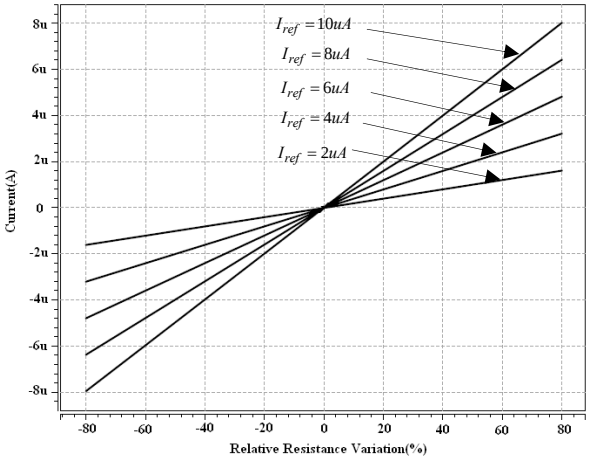
Simulation results showed that the power consumption is less than 350uW and dynamic range is more than 80dB. Also, the maximum absolute error for 1% relative resistance variation is less than 0.35%.



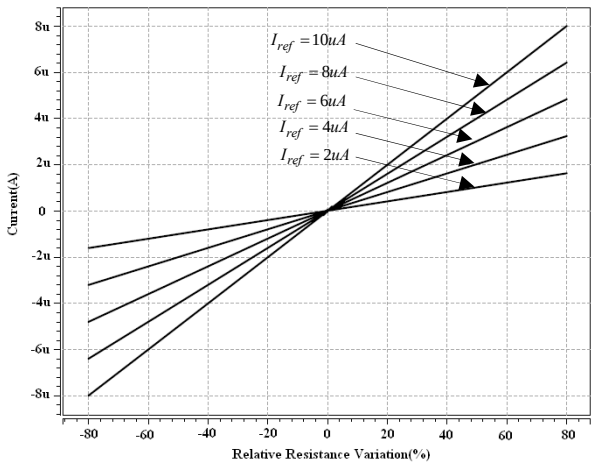
(a)

(b)

Fig. 5 Output current V.S. resistance variation at different reference resistance values for a) CMWB of Fig. 3 b) CMWB of Fig. 4



(a)



(b)

Fig. 6 Output current V.S. relative resistance variation at different reference current values a) CMWB of Fig. 3 b) CMWB of Fig. 4

VI. Conclusion

By using of MOS transistors a new CMWB circuit design is presented. The proposed CMWB is not complicated, which shows flexible properties with respect to other current or VM circuits. Also, we can add the sensor effects, superposition ability, without using complicated circuitry, which is an excellent advantage over the traditional VMWBs. Furthermore, we can reduce the number of sensing passive elements; i.e., we can use two resistors instead of four and get the same performance as the VMWBs. Therfore, the circuit facilitates reduced multiple sensor operation, has low circuit complexity, is immune from body effect, works at low supply voltage and consume low power. Also a modified circuit for linearization technique is proposed. Simulation results of the proposed circuit shows that the technique is promising and can be successfully applied in a wide range of mixed A/D instrumentation and measurement integrated circuits.

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Ebrahim Farshidi was born in Shoushtar, Iran, in 1973. He received the B.Sc. degree in 1995 from Amir Kabir University, Iran, the M.Sc. degree in 1997 from Sharif University, Iran and the Ph. D. degree in 2008 from electrical engineering at IUT, Iran, all in electronic engineering. He worked for Karun Pulp and Paper Company during 1997–2002. From 2002 he has been with shahid chamran university, Ahvaz, where he is currently assistant professor and head of electrical engineering department. He is author of more than 25 technical papers in electronics. His areas of interest include current-mode circuits design, low power VLSI circuits, and data converters.