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Subthreshold Circuit Performance Investigation under Temperature Variations

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***Abstract*—**Ultra-low-power (ULP) circuits have received widespread attention due to the rapid growth of biomedical applications and Battery-less Electronics. Subthreshold region of transistor operation is used in ULP circuits. Major research challenge in the subthreshold operating region is to extract the ULP benefits with minimal degradation in speed and robustness. Process, Voltage and Temperature (PVT) variations significantly affect the performance of subthreshold circuits. Designed performance parameters of ULP circuits may vary largely due to temperature variations. Hence, this paper investigates the effect of temperature variation on device and circuit performance parameters at different biasing voltages in the subthreshold region. Simulation results clearly demonstrate that in deep subthreshold and near threshold voltage regions, performance parameters are significantly affected whereas in moderate subthreshold region, subthreshold circuits are more immune to temperature variations. This establishes that moderate subthreshold region is ideal for temperature immune circuits.

***Keywords*—**Subthreshold, temperature variations, ultralow power**.**

I. INTRODUCTION

GORDON E. Moore in 1965 predicted that the number of transistors per chip will roughly double after every two years [1], thereby increasing the functionality per chip. This trend is enabled by technology scaling, which results in speed improvement for logic gates to support the higher clock frequency along with the reduction in the energy per operation. Despite this reduction in energy per operation, the total power consumption per chip has increased significantly [2]. Accelerated technology scaling, to satisfy Moore's law, is driven primarily by the demand for high performance keeping power dissipation a secondary design issue. This significant rise in the maximum number of devices on a chip by evolutionary device scaling and/or increased chip size along with higher frequency increase both dynamic/leakage power dissipation, self heating and reduces the robustness of the device. However, due to the significant rise in the demand of portable and biomedical applications in the last decade and increase in both dynamic/leakage power dissipation gradually made power dissipation a vital design issue with speed as a secondary design criteria. Increased power dissipation in nanometer regime can be tolerable for highest performance circuits. However, it is the most demanding design issue for intended ULP applications. Numerous efforts have been undertaken to manage the growing power problem [3-6], however to achieve ULP consumption, a transistor needs to operate in the subthreshold region [7].

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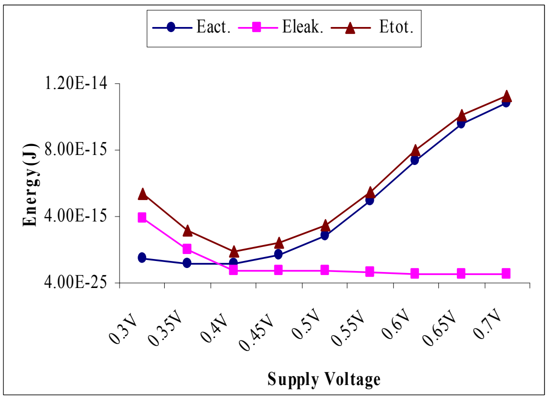

Fig. 1 Energy as a function of Supply Voltage

Fig. 1 shows different energy consumption components as a function of supply voltage. It is clear from Fig. 1 that minimum energy operation can be obtained only under subthreshold conditions. To fulfill ULP demand of portable biomedical applications, research community has shifted their focus towards subthreshold operating region [8-10]. Device operating in subthreshold regime has shown strong potential towards satisfying the ULP requirements of moderate throughput portable systems. As supply voltage (V_{DD}) is scaled below the threshold voltage (V_{th}) of the device to achieve ULP levels, design challenges in improving circuit delay and robustness increase [10-12]. Variations in PVT parameters largely affect the performance of subthreshold circuits and may cause the malfunctioning of these circuits as illustrated in Fig. 2. Higher speed and robustness of subthreshold circuits will expand their application domain. This paper mainly contributes towards investigating the deviation in device and circuit performance parameters due to temperature variations under subthreshold conditions. It establishes that moderate subthreshold region is attractive for temperature immune circuits.

Rest of this paper is organized as follows. Section II explores the subthreshold region of operation of MOSFET. Section III investigates the effect of temperature variation on device and circuit performance parameters. Finally, section IV concludes this paper.

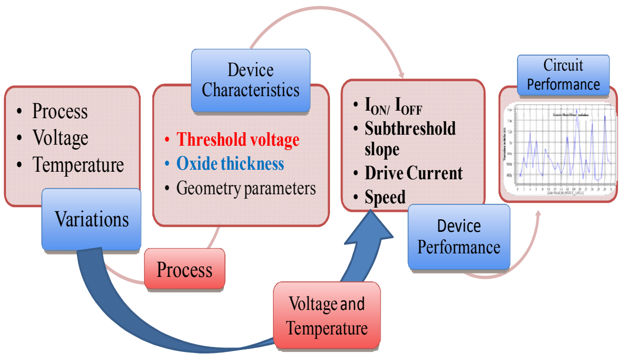

Fig. 2 Effect of PVT variation on device and circuit perfomance metrics

II. Subthreshold Region of Operation

In recent years, there is an increasing demand of battery operated mobile platforms and emerging applications such as distributed sensor networks, RFIDs, biomedical devices, cell phones, body area networks etc., having low power budget for ultra low energy operation instead of higher performance. Demanding design issue in such applications is to extend operational life as long as possible by reducing the power dissipation. Operating device in subthreshold region satisfies ULP demand of portable devices. The most important leakage current for ultra low power application is the sub-threshold leakage current, originated by the diffusion of minority carriers in a non-conducting transistor ($V_{gs} < V_{th}$). Under this condition, the transistor is operating in weak inversion region. The potential applied between drain and source creates a flow of the minority carriers on the surface of the channel. These minority carriers are used as switching current.

Subthreshold leakage current in a MOSFET exponentially depends on the gate voltage, threshold voltage and temperature and is given by equation (1) and is shown in Fig. 3 [5],

$$I_D = I_0 e^{\frac{(V_{GS}-V_{th}+\eta V_{DS})}{nV_T}} \left(1-e^{\frac{-V_{DS}}{V_T}}\right) \quad (1)$$

where I_0 is given by,

$$I_0 = \mu_0 C_{ox} \frac{W}{L}(n-1)V_T^{\,2} \quad (2)$$

where V_{th} is the transistor threshold voltage, n is subthreshold slope factor ($n=1+C_d/C_{ox}$), V_T is the thermal voltage, η is DIBL coefficient. V_{th} is given by equation (3) [12].

$$V_{th} = V_{FB} + (\Phi_{S0} - \Delta\Phi_S) + \gamma\sqrt{\Phi_{S0} - V_{bs}}\,\left(1-\lambda\frac{Xd}{L_{eff}}\right) + \Delta_{VNWE} \quad (3)$$

where, V_{FB} is the flat-band voltage, Φ_{S0} is zero bias surface potential, γ is the body factor, X_d is the depletion layer thickness.

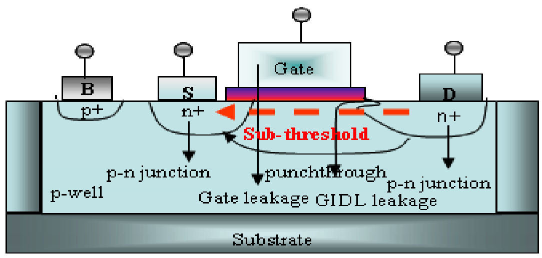

Fig. 3 Leakage components in a MOSFET

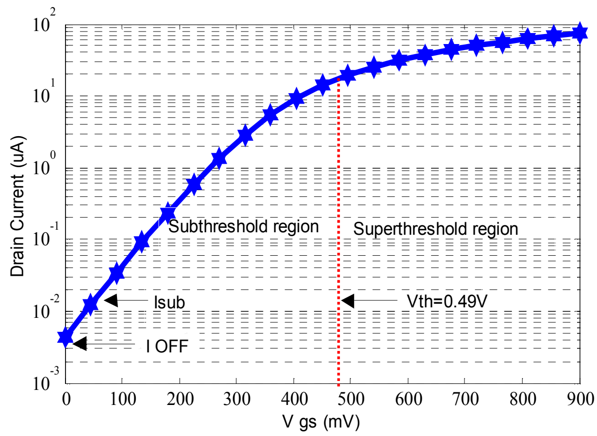

Fig. 4 I-V chracteristics of Si-MOSFET

Fig. 3 shows the leakage current components in a Si-MOSFET. The useful component is subthreshold current that flows from drain to source in a weakly inverted channel. Subthreshold current is exponentially dependent on the gate to source voltage (V_{GS}) as shown in Fig. 4 because this current is due to the flow of carriers through diffusion. Increase in temperature reduces the threshold voltage thereby, causing exponentially rise in subthreshold leakage current.

III. Effect of Temperature Variation on Subthreshold Circuit Performance

Elegant scaling requirements on V_{DD} and V_{th}, to sustain speed and to limit energy consumption, pose several technology and circuit design challenges. Though, technology scaling has achieved required speed, static leakage and variability issues are the two most important design concerns in advanced above threshold nanoscale CMOS technology. However, exponential dependency of subthreshold drive current on V_{th} , V_{DS} and temperature in subthreshold operating region makes PVT variations of great interest while designing robust ULP systems along with speed. This section explores the effect of temperature variation on subthreshold circuit performance. Unlike superthreshold, where due to the high gate-overdrive, the mobility dominates and hence transistors drain current I_{ON} decreases with increase in temperature, the subthreshold current I_{sub} increases exponentially with temperature [13]. Therefore, it is necessary to investigate the effect of temperature variation at different biasing conditions under subthreshold regime. Equation (1) can be written as [14],

$$Isub = \mu_0 C_{OX} \frac{W}{L}(n-1)\frac{K^2}{q^2} e^{\frac{(V_{GS}-V_{th})}{n(kT)}}\left[1-e^{\frac{-V_{DS}\,q}{kT}}\right] \quad (4)$$

Equation (4) shows the direct dependence of I_{sub} on temperature. This section make several key observations about temperature dependency of subthreshold leakage current and different device parameters based on HSPICE simulations using 32nm technology node PTM files. Five stage inverter chain is considered as a test bench and all measurements are carried out for the third inverter in the chain.

Fig. 5 shows the effect of temperature variation on drain current under subthreshold conditions for different gate overdrive voltage. It is observed from Fig. 5 that below 350mV V_{DD}, I_{sub} increases with the increase in temperature. At 350mV $V_{DD,}$ the effect of temperature variation on I_{sub} is minimum. Above this voltage, I_{sub} increases with the increase in temperature. Hence, it can be inferred that the rate of change of I_{sub} is dependent upon the gate-overdrive voltage. Fig. 6 shows the effect of temperature variation on the device transconductance at different biasing voltages. It has been observed from Fig. 6 that in deep subthreshold region (V_{DD}=0.2V), the transconductance increases with temperature. As supply voltage increases, transconductance decreases with temperature especially in moderate subthreshold region and in superthreshold region due to the decrease in drive current as shown in Fig. 6. At V_{DD} = 0.3V, the temperature effect on transconductance is minimum.

I_{ON}/I_{OFF} mainly determines the power dissipation of the device. I_{ON} is the subthreshold leakage current at $V_{DD}=V_{GS}=V_{DS}$ and I_{OFF} is the leakage current at V_{GS}=0V and $V_{DS}=V_{DD}$. For better performance, higher I_{ON}/I_{OFF} is preferred. Figure 7 shows the effect of increase in temperature on I_{ON}/I_{OFF} ratio. As temperature increases, I_{ON}/I_{OFF} ratio decreases significantly. This is due to higher rate of change of I_{OFF} with respect to. temperature compared to I_{ON}. Though drive current increases with rise in temperature, device OFF current also increases which results in higher leakage power dissipation. Fig. 8 shows that with the increase in temperature, threshold voltage decreases. It has also been observed that with the increase in supply voltage, threshold voltage decreases significantly. Increasing temperature from 20°C to 120°C decreases V_{th} by 7.78%, 8.88% and 13.26% for V_{DD}=0.2V, 0.4V and 0.9V respectively.

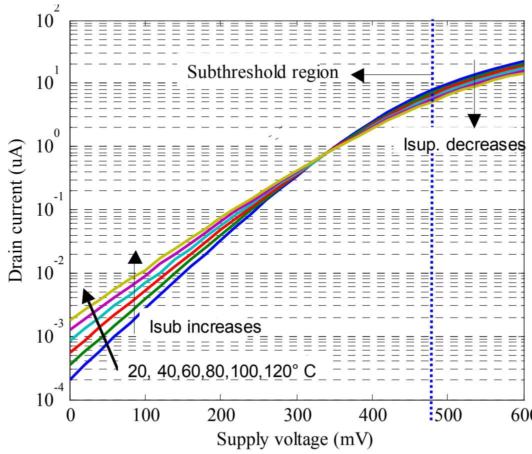

Fig. 5 I-V characteristics of Si- MOSFET at different temperatures

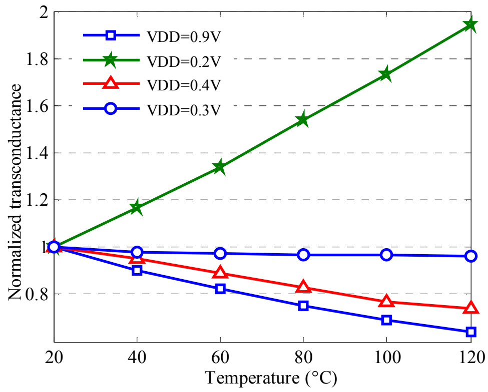

Fig. 6 Transconductance as a function of temperature

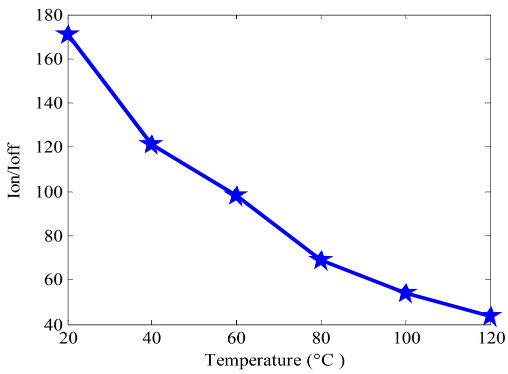

Fig. 7 I_{ON}/I_{OFF} as a function of temperature at V_{DD}=0.2V

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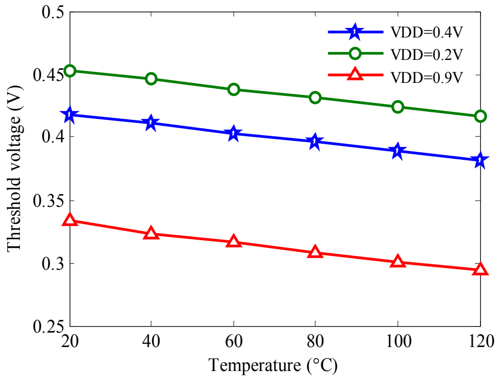

Fig. 8 Threshold voltage as a function of temperature

Fig. 9 and 10 show the effect of temperature variation on the delay and power dissipation of an inverter. It is clear from Fig. 9 that in deep subthreshold region (V_{DD} = 0.1V), delay decreases by 66.9%. However, in moderate subthreshold (V_{DD}=0.4V) region, increasing temperature from 20°C to 120°C, the delay only increases by 13% due to decrease in drive current as shown in Fig. 7. Hence, to minimize the effect of temperature variation, it is necessary to operate a circuit in moderate subthreshold region instead of deep subthreshold and near to subthreshold region. As shown in Fig. 10, it can be observed that as temperature increases, power dissipation increases significantly. It has been also observed that at V_{DD} = 0.1V, percentage increase in power dissipation is higher over V_D = 0.4V. Hence, power delay product significantly rises at lower V_{DD} as shown in Fig. 11. Fig. 12 shows the effect of temperature variation on Voltage Transfer Characteristics (VTC) of an inverter. It has been observed that switching threshold of inverter is not very much affected by the increase in temperature. However, it has also been observed from Fig. 12 that noise margin decreases with the increase in temperature. Fig. 13 shows the effect of temperature variation

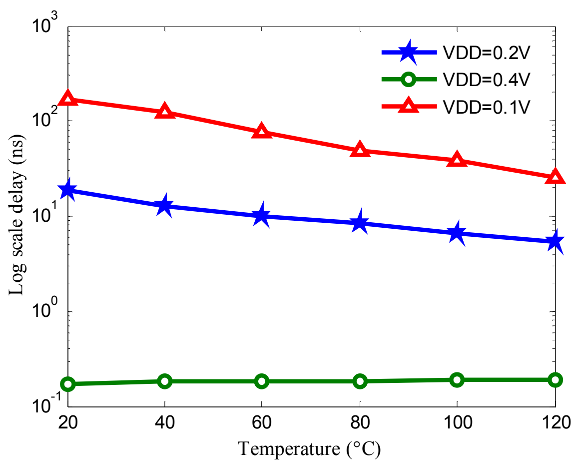

Fig. 9 Effect of temperature variation on inverter delay

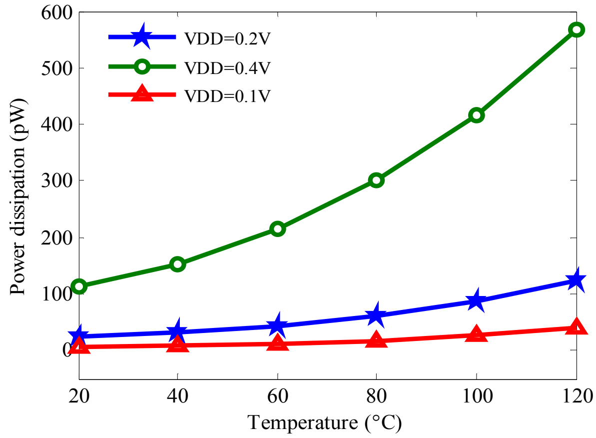

Fig. 10 Effect of tempertature on power dissipation of an inverter

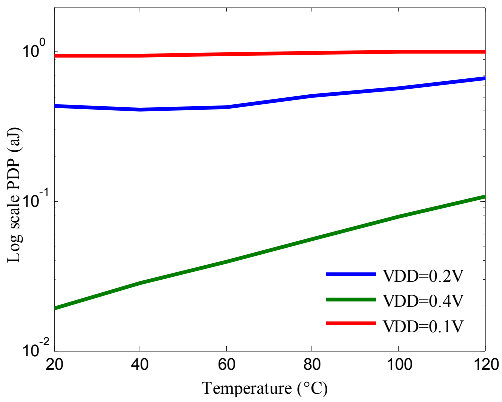

Fig. 11 Effect of tempertature on PDP of an inverter

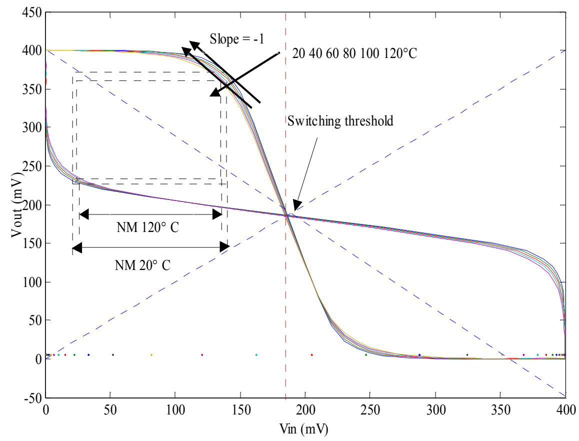

Fig. 12 Effect of tempertature on noise margin of an inverter

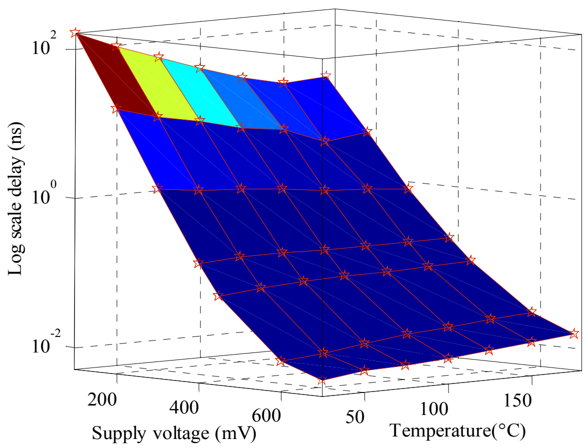

Fig. 13 Effect of tempertature on delay at different voltages

on delay across the third inverter in the chain of five inverters. It is clear that the delay variation is less in moderate subthreshold regime compared to deep subthreshold and near threshold voltage regions.

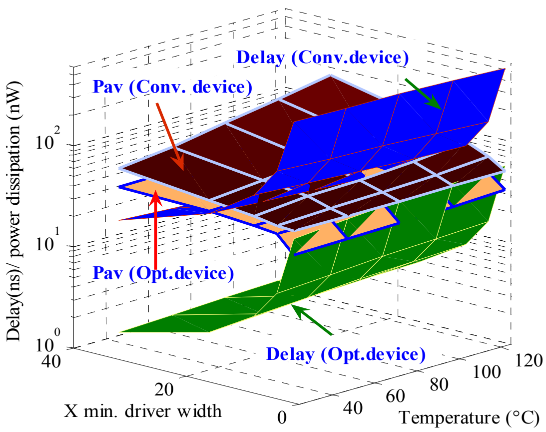

Fig. 14 Effect of tempertature on delay and power dissipation at different driver width

It is clear from the previous section that there is a need to optimize the device for minimum temperature effects. Further more, our previous work has already optimized the threshold voltage and oxide thickness of the device and investigated the performance of interconnect driver at different temperature [11]. Fig. 14 shows the delay and power variability at different temperatures [14]. It has been clear that moderate subthreshold region based driver operation reduces the effect of temperature variation significantly.

IV. Conclusion

This paper has successfully explored the effect of temperature variations on subthreshold device and circuit performance at different supply voltages. It has been observed that temperature variation significantly affects the performance of subthreshold circuits in deep subthreshold region and near threshold voltage regions. I-V characteristics of Si-NMOS device shows that operating subthreshold device in moderate subthreshold region reduces the effect of temperature variation significantly. Subthreshold region shows both positive and negative temperature dependency depending upon the gate overdrive voltage. Therefore, to mitigate the temperature variation effects on subthreshold circuit performance, an optimum supply voltage is needed to design in moderate subthreshold region. Increase in temperature reduces the noise margin due to large device OFF current. It has also been observed that temperature variation does not affect the switching threshold voltage of an inverter.

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