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A ±0.5V BiCMOS Class-A Current Conveyor

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Abstract**—**In this paper, a new BiCMOS CCII and CCCII, capable of operate at ±0.5V and having wide dynamic range with achieved bandwidth of 480MHz and 430MHz respectively have been proposed. The structures have been found to be insensitive to the threshold voltage variations. The proposed circuits are suitable for implementation using 0.25µm BiCMOS technology. Pspice simulations confirm the performance of the proposed structures.

Keywords**—**BiCMOS, Current conveyor, Compound current conveyor, Low supply voltage, Threshold voltage variation.

I. Introduction

A Current Conveyor II (CCII) has the unique feature of having both low and high impedance input port, a port generally termed as port X which serves as low input port for input current and output voltage. The low input impedance port is suitable for current mode structures, and high input impedance port suitable for voltage mode operation. Similarly it has high output impedance port for current mode structures and low output impedance port suitable for voltage mode operations. Hence a CCII is more versatile and can be used to process both current and voltage signals [1]-[8].

A CC is a grounded three-port network as shown in Fig.1. and it's characteristic is given as

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

where X and Y are the input ports and Z is the output port.

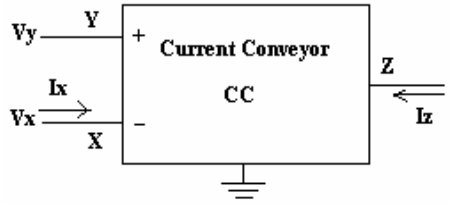

Fig. 1 CCII+ block diagram

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The bipolar transistors have higher transconductance (g_m) and high frequency performance over their CMOS counterparts [9]. Advantage of MOSFET includes high input impedance, low power consumption, and small silicon area [10]. In BiCMOS structures the advantage of the both technology have been utilized. In this paper a new CCII and Compound current conveyor (CCCII) structures suitable for integration in BiCMOS technology and capable of operate at ultra low voltage of ±0.5V have been proposed. The structures have a wide current bandwidth of 480MHz for class-A CC and 430MHz for class-A CCC with power consumption of 0.80mW and 1.0mW respectively.

II. Proposed ±0.5V Class-A BICMOS CCII Realization

The proposed BiCMOS realization for the low voltage CCII is shown in Fig. 2. The circuit has been designed using MOSFETs and BJTs in order to get the requirement of low power supply and low power dissipation. The input stage and current source have been realized through MOSFETs so that the high input impedance structure can be implemented. In order to operate at a low voltage and reducing power supply, bipolar current mirror is used because it has larger dynamic range [10]-[11]. Furthermore, it has superior high frequency performance then their CMOS counterpart [9].

The groups of the transistors (M1 and M2), (Q3 and Q4), (Q7–Q9), as well as (M11 and M12) are matched. All the MOSFETs operate in saturation region, while all the BJTs in active region. M10, M11, M12, and M13 serve as DC current sources. The current mirroring has been achieved by Q3 and Q4 forces equal currents I_B in M1 and M2, there by resulting in equal gate to source voltage This forces voltage at port X to follow the impressed voltage at port Y Mirroring action between Q7 and Q9, and M12 and M14 transfer Ix to I_{Z+}.

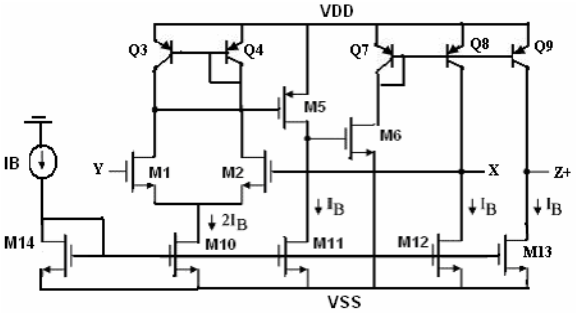

Fig. 2 Proposed Low Voltage BiCMOS Class-A CCII

The threshold voltage variation caused by the body effect of MOS transistors are negligible owing to the fact that except M1,M2 and M6, all the MOSFETs have sources that are connected to the positive or negative supply rail. Threshold voltage variations of transistors (M1 and M2) are canceled out

because of their differential configuration which canceled the equal threshold voltage variations [13]-[14].

Voltage offset of the proposed circuit is also very low. The voltage offset is given by the following relationship

$$\Delta V = V_X - V_Y \tag{2}$$

$$\Delta V \approx \left[\lambda_n \left(V_{DS1} - V_{DS2}\right)\right] \sqrt{\frac{I_B}{\mu_n C_{OX} \left(W/L\right)_1}} + \left(\Delta V_{th}\right) \tag{3}$$

where λ_n is the channel length modulation factor, V_{DS1} and V_{DS2} are the drain voltages of transistors M_1 and M_2. This offset can be cancelled by making V_{DS1} equal to V_{DS2}. The last term ΔV_{th} is owing to the threshold voltage mismatch, which is bias-current independent and is a strong function of fabrication process [13][15]. This offset cancellation is independent of the input current and voltage.

The relationship between V_X and V_Y can be expressed by performing small signal analysis. The transistors in Fig. 2 are replaced by equivalent circuits and the node equations are derived by applying the current law at nodes. To simplifying, it has been assumed that the drain conductance of the current source M10 is zero and that no body effect occurs. By solving the equations for V_X and V_Y,

$$\frac{V_X}{V_Y} = \frac{g_{m2}}{\left(g_{m2} + g_{d2} + g_{o4}\right)} \tag{4}$$

where g_{m2} and g_{d2} denote the transconductance and the drain conductance, of MOSFET M2, and g_{o4} denote output conductance of bipolar transistor.

Similarly, the port impedance at port X has been derived,, but in this case, the voltage V_Y is set equal to zero, and a test voltage V_X is applied at port X. The R_X has been given as

$$R_X \approx \frac{\left(g_{m1} + g_{m2}\right)\left(g_{d2} + g_{o4}\right)}{\left(g_{m1} \cdot g_{m2} \cdot g_{m5}\right)} \tag{5}$$

It is assume that the small signal gain and input resistance of bipolar transistor is high

The output impedance at port Z is approximately equal to the output resistance of the current mirror Q7-Q9 in parallel with the output resistance of the current sink M13, and may be approximated as

$$R_Z \approx \frac{1}{\left(g_{d9} + g_{o13}\right)} \tag{6}$$

Where g_{d9} denote the drain conductance, of BJT Q9, and g_{o13} denote output conductance of MOSFET M13.

III. Proposed ±0.5V Class-A BiCMOS CCCII Realization

The above proposed circuit can be improved to include Z- port as shown in Fig. 3 By using extra current mirrors, current through port X is conveyed to Z- port with the negative polarity. Current direction has been inverted by using current mirrors formed by Q16-Q17 and Q18-Q19 to get $I_{Z^-}=I_X$.

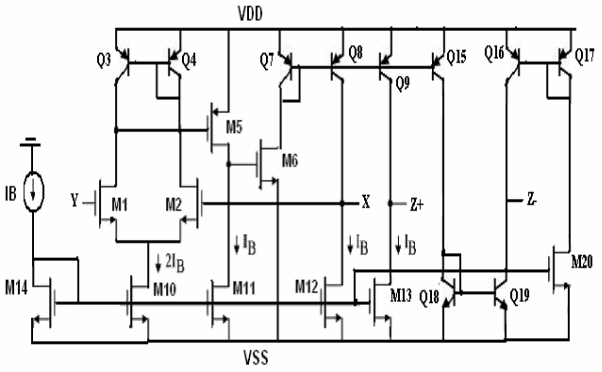

Fig. 3 Proposed low voltage BiCMOS class-A CCCII

The basic characteristic of the proposed class-A CCCII has been similar to proposed CCII.

IV. Simulation Results

The proposed BiCMOS CCII+ and CCCII structures have been simulated with the PSPICE for 0.25µm BiCMOS process at ±0.5V. The aspect ratios of the MOS transistors for CCII and CCCII are given in Table I. The voltage transfer is almost rail to rail (-0.5V to +0.5V) as shown in Fig4, within 0.1% error at the end of the transfer curve as shown in Fig. 5. Fig. 6 shows the variations of X port voltage against the current I_X. A linear input current transfer from -125µA to +125µA takes place for class-A CCII structure as show in Fig. 7 for port Z. The ac current gain between port X and port Z, has been plotted in Fig. 8 and Fig. 9, for CCII and CCCII structures respectively. The maximum bandwidth of 480MHz has been obtained for current transfer characteristics I_Z/I_X. The power consumption of the proposed structures are 0.80mW and 1.0mW for class-A CCII and CCCII structures respectively. Input current transfer for class-A CCCII structure is same as that of for class-A CCII structure as show in Fig. 10 and Fig. 11 for port Z+ and Z- respectively. The summary of the simulated result for class-A BiCMOS CCII and class-A CCCII are given in Table II.

TABLE I
Transistors Aspect Ratios of Proposed CCII Structure

Transistor	W/L (µm)
M1,M2	30/0.25
M5	50/0.5
M6	10/0.25
M10	50/0.5
M11,M12,M13,M14,M20	25/0.5

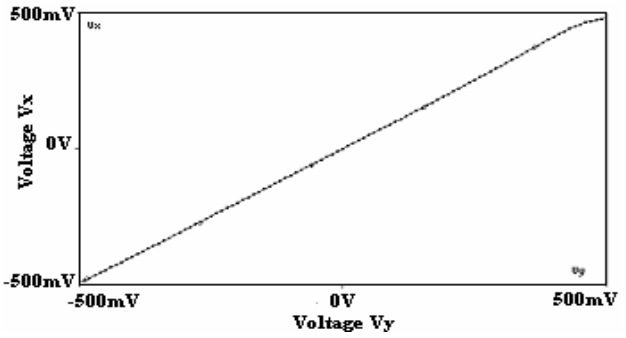

Fig. 4 Static characteristics of the conveyor voltage transfer function

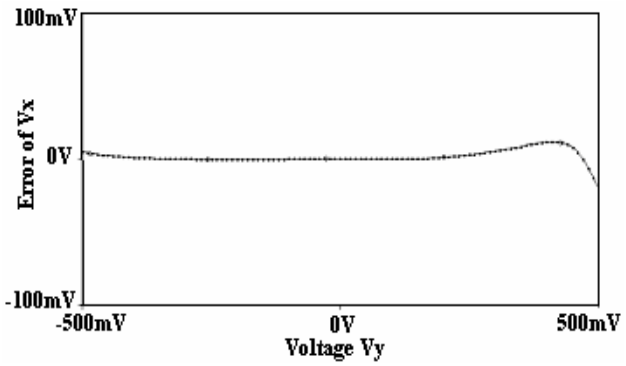

Fig. 5 Voltage transfer error at X port

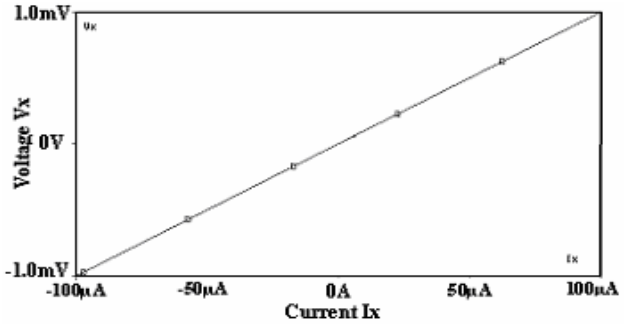

Fig. 6 Input port X characteristics

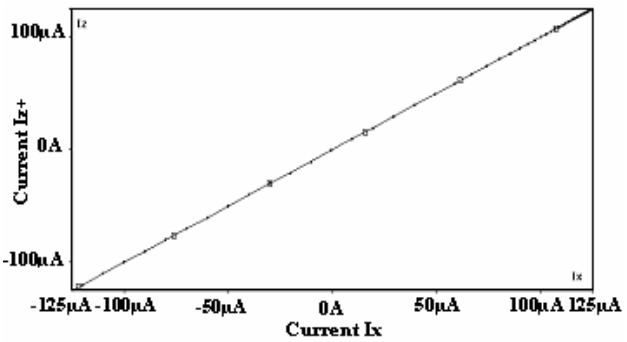

Fig. 7 Static characteristics of the conveyor current transfer function from I_{Z+} to I_X

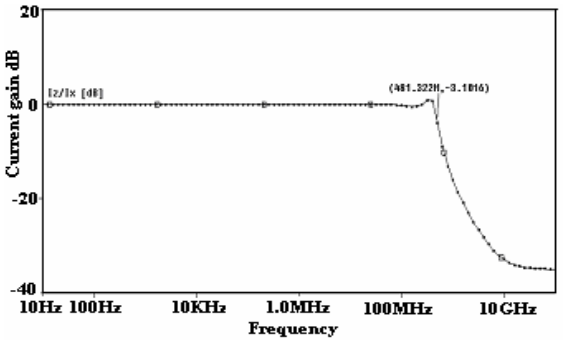

Fig. 8 Amplitude characteristics of the conveyor current transfer function I_Z/I_X [dB]

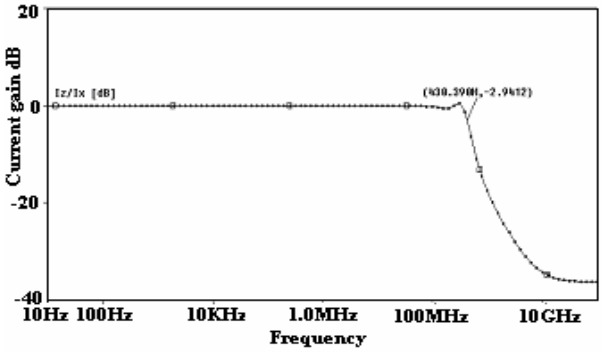

Fig. 9 Amplitude characteristics of the current transfer function I_{Z+}/I_X [dB]

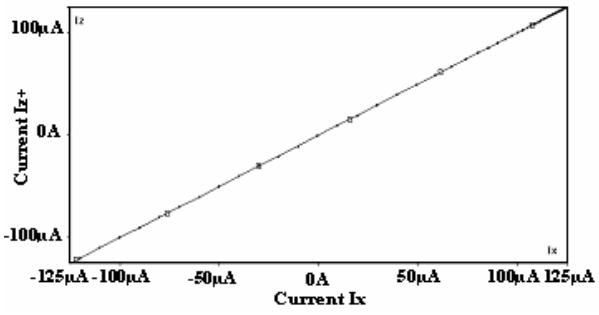

Fig.10 Static characteristics of the conveyor current transfer function from I_{Z+} to I_X

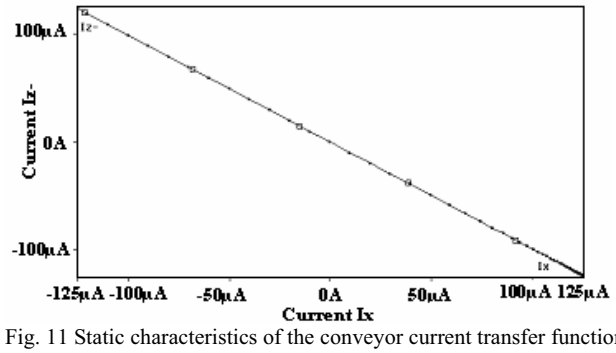

Fig. 11 Static characteristics of the conveyor current transfer function from I_{Z-} to I_X

TABLE II
BASIC CHARACTERISTICS OF PROPOSED CCII AND CCCII

Parameters	Class-A CCII 0peration	Class-AB CCCII operation
Supply Voltage	±0.5V	±0.5V
Current Gain	1.0	1.0
Voltage Gain	0.96	0.96
Current TR band width	480MHz	430MHz
Output resistance at port Rz	4.7KΩ	4.7KΩ
Input resistance at port Rx	2.57Ω	2.57Ω
Input resistance at port Ry	1.0E20Ohm	1.0E20Ohm
Power dissipation	0.80mW	1.0mW
Voltage range	-0.5V to +0.5V	-0.5V to +0.5V
Current Range	-125µA to +125µA	-125µA to +125µA

V. CONCLUSION

The proposed current conveyor structures can operate at ultra low voltage of ±0.5V and have, bandwidths of 480MHz for class-A CCII and of 430MHz for class-A CCCII, wide dynamic range of rail to rail (-0.5V to +0.5V) for both the structures, and low power dissipation. The proposed structures are suitable for the low voltage, low power VLSI Applications.

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