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A high Speed 8 Transistor Full Adder Design using Novel 3 Transistor XOR Gates

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***Abstract*—**The paper proposes the novel design of a 3T XOR gate combining complementary CMOS with pass transistor logic. The design has been compared with earlier proposed 4T and 6T XOR gates and a significant improvement in silicon area and power-delay product has been obtained. An eight transistor full adder has been designed using the proposed three-transistor XOR gate and its performance has been investigated using 0.15µm and 0.35µm technologies. Compared to the earlier designed 10 transistor full adder, the proposed adder shows a significant improvement in silicon area and power delay product. The whole simulation has been carried out using HSPICE.

***Keywords*—**XOR gate, full adder, improvement in speed, area minimization, transistor count minimization.

I. Introduction

EVER since its inception, the design of full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed [1-12]. Hosseinzadeh, Jassbi and Navi emphasized on circuit performance improvement in [1] through transistor count minimization.

XOR gates form the fundamental building block of full adders. Enhancing the performance of the XOR gates can significantly improve the performance of the adder. A survey of literature reveals a wide spectrum of different types of XOR gates that have been realized over the years. The early designs of XOR gates were based on either eight transistors [3] or six transistors [3] that are conventionally used in most designs. Over the last decade, considerable emphasis has been laid on the design of four-transistor XOR gate [2, 4, 5, 6, 7, 8, 9, 10, 11]. Radhakrishnan proposed a formal approach of minimizing the transistor count in XOR and XNOR gates in [2]. Wang, Fang and Feng in [4] proposed novel XOR architectures shown in figures 1 (a) and (b) that could operate without requiring complementary inputs which is a severe drawback of CMOS transmission gate logic based XOR gates shown in [3]. The values of W/L ratios of the transistors have been shown in the figure besides the respective transistors. Bui, Wang and Jiang further improved the XOR gate proposed in [4] and designed a XOR gate without a V_{DD} [5] shown in figure 1(c). They further designed adders with some improvements in the power-delay product and used these XOR gates in their design [6, 7] but the silicon area remained unchanged. However, the proposed XOR gates consumed considerable silicon area for their optimum performance and the power delay product is also large. Wang, Fang and Feng also proposed another XOR gate in [4] and further studied by Shams, Darwish and Bayoumi in [8]. With a view of further optimization of performance of XOR gates in terms of silicon area and power delay product, considerable emphasis has been given in the present work on the design of three transistor XOR gates.

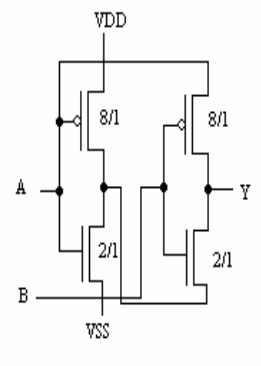

Fig. 1. (a)

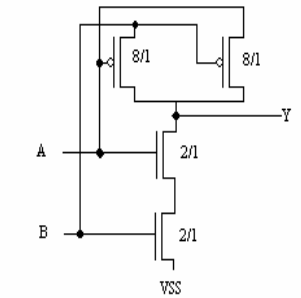

Fig. 1(b)

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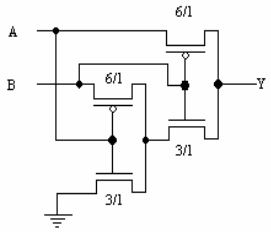
Fig. 1(c)



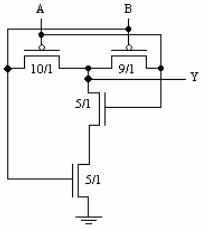


Fig. 1(c) Fig. 1(d)
Fig. 1 Previous designs of XOR gates found in literature

A survey of the contemporary literature reveals a wide spectrum of adder designs over the past few decades. The full adder design in static CMOS using complementary pull up pMOS network and pull down nMOS network shown in [13] is the most conventional one, and it also has the advantage of very low power consumption. However, it has as many as 28 transistors and thus requires considerable chip area for its implementation. The full adder design in [14] based on CMOS transmission gates and CMOS inverters uses 20 transistors. The circuit can operate with full output voltage swing. In [15], the designs were further reduced to only 16 transistors while maintaining the full output voltage swing operation. To further minimize the number of transistors, pass transistor logic can be used in lieu of transmission gate. Pass transistor logic based XOR and XNOR circuits were used in [16] and as a result the full adder design in [17] consists of only 14 transistors. In this design, an inverter is employed to generate the function $\left(\overline{A \oplus B}\right)$. In [18] a 16 transistor adder was proposed to minimize the short circuit power dissipation of the 14T full adder proposed in [17]. With an objective of further minimizing the transistor count, a pass transistor logic based static energy recovery full adder with as few as ten transistors was presented in [19]. In spite of its claimed superiority in energy consumption, the design is relatively slower than its peer designs and hence is not suitable for high speed architectures. Bui, Wang and Jiang in [6] proposed an improved 10 transistor full adder design based on systematic exploration of the combinations of various XOR, XNOR, sum and Cout modules. But it suffers from severe threshold loss problem and cannot operate properly in cascade under low supply voltage. Fayed and Bayoumi in [19] proposed another 10 transistor full adder consisting of two pass transistor based XORs and a 2-to-1 multiplexer. But again it suffers from severe threshold loss problem. Liu, Hwang, Sheu and Ho, however, could minimize the threshold loss problem in a 10 transistor adder reported in [20] as a Complementary and Level Restoring Carry Logic (CLRCL) adder. In the CLRCR adder, 2-to-1 multiplexers and CMOS inverters are used to realize the sum and cout functions using the Boolean equations:

$$Sum = (A \oplus Cin).\overline{Cout} + (\overline{A \oplus Cin}).B$$

$$Cout = (A \oplus Cin).B + (\overline{A \oplus Cin}).A$$

The inverters have been used to combat the output threshold voltage loss and also as a buffer along the carry chain to speed up the carry propagation. The logic block diagram of the CLRCL full adder as shown in [20] is shown in figure 2:

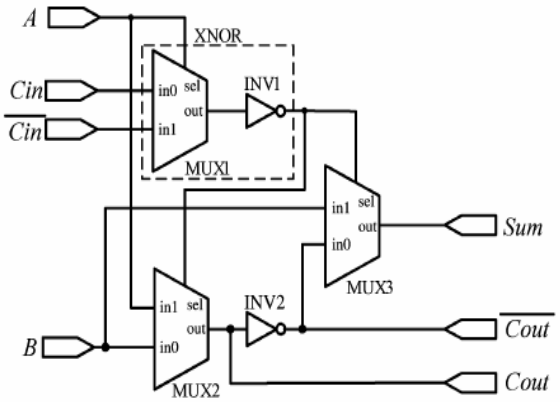


Fig. 2 Logic block diagram of CLRCL full adder.

However, the design suffers from two drawbacks. Firstly, it requires that two complementary signals Cin and $\overline{Cin}$ be available at the same time at the inputs, which is quite difficult. Otherwise $\overline{Cin}$ has to be generated from Cin using an inverter, which entails for adding two more transistors to the adder design. Secondly, the design in figure 1 indicates that three stage delays are required to generate the carry output and five stage delays are required to generate the sum and the effect of this delay is also evident from the simulation results.

The current work presents the design of a full adder using eight transistors. Our work achieves the design of full adder with sum and carry outputs with only two stage delays. The idea of minimizing the delay of circuit by minimizing the logic depth has also been corroborated by Balasubramanian et al in [21]. The full adder has been designed using three transistor XOR gates using the novel concept of combining a CMOS inverter and a pass transistor as described in details in section 2. In section 3, we have realized an 8T full adder using rather conventional logic combination of 3T XOR gates.

In order to establish the technology independence of the design, the adder has been designed using 0.15μm and 0.35μm technologies. The power-delay simulation of the adder has been carried out. Simulation results indicate that the designed full adder has much less power-delay product that its peer designs.

II. Design of the Three-Transistor XOR Gate

The design of the full adder is based on the design of the XOR gate. The proposed design of full adder uses three transistor XOR gates. The design of a three transistor XOR gate is shown in figure 3.

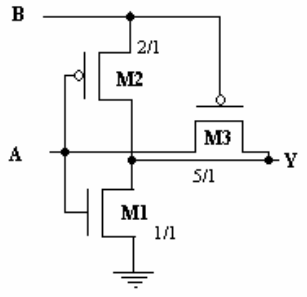


Fig. 3 Design of 3T XOR gate

The design is based on a modified version of a CMOS inverter and a PMOS pass transistor. When the input B is at logic high, the inverter on the left functions like a normal CMOS inverter. Therefore the output Y is the complement of input A. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M3 is enabled and the output Y gets the same logic value as input A. The operation of the whole circuit is thus like a 2 input XOR gate. However, when A=1 and B=0, voltage degradation due to threshold drop occurs across transistor M3 and consequently the output Y is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3. Specifically from [22], we find the following equation (1) that relates the threshold voltage of a MOS transistor to its channel length and width.

$$V_T = V_{T0} + \gamma(\sqrt{V_{SB}+\phi_o} - \sqrt{\phi_o}) - \alpha_l \frac{t_{OX}}{L}(V_{SB}+\phi_o) - \alpha_v \frac{t_{OX}}{L} V_{DS} + \alpha_w \frac{t_{OX}}{W}(V_{SB}+\phi_o) \quad \ldots.(1)$$

where V_{T0} is the zero bias threshold voltage, γ is bulk threshold coefficient, ϕ_o is $2\phi_F$, where ϕ_F is the Fermi potential, t_{OX} is the thickness of the oxide layer and α_l, α_v and α_w are process dependent parameters. From (1) it is evident that by increasing W it is possible to decrease the threshold voltage and therefore by increasing the width of transistor M3, keeping the length constant, it is possible to minimize the voltage degradation due to threshold voltage drop. The decrease of threshold voltage when the channel width of transistor M3 is increased has been studied in different technologies and shown in figure 4.

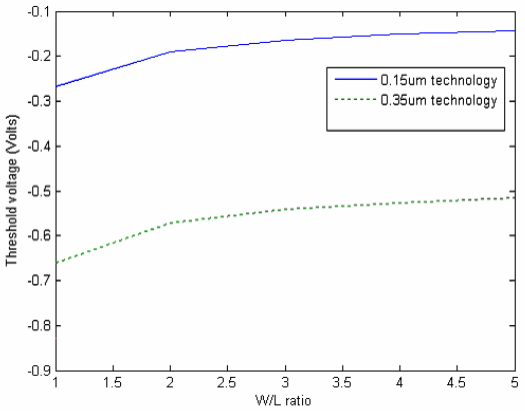


Fig. 4 Variation of threshold voltage with W/L ratio of PMOS transistor in different technologies

The absolute value of threshold voltage ($|V_{th}|$) of PMOS transistor M3 decreases from 0.661V to 0.516V when its W/L ratio is increased from 1/1 to 5/1 in 0.35 μm technology and also decreases from 0.267V to 0.143V when its W/L ratio is increased from 1/1 to 5/1 in 0.15 μm technology. Therefore, the voltage degradation due to threshold drop when A=1 and B=0, can be considerably minimized by increasing the W/L ratio of transistor M3.

A second problem of current feedback through transistor M1 also occurs when A=1 and B=0. The output of the pass transistor is fed back through transistor M1 which is operating in the active region since its gate has a logic high input. This difficulty can be overcome by decreasing the W/L ratio of transistor M1. With W=L, the channel resistance of transistor M1 amounts to 2.34 MΩ in 0.15 μm technology and 1.82 MΩ in 0.35 μm technology. With A=1 and B=0, the drain current through transistor M1 is 0.314μA in 0.15 μm technology and 1.51μA and this greatly limits the currents through it thereby minimizing the steady state power dissipation. The resistance can be further increased and the current can be further decreased by further minimizing W/L ratio. For example with W/L=0.5, the drain current through transistor M1 is 0.157μA in 0.15 μm technology and 0.755μA in 0.35 μm technology. Typical values of W/L ratios for transistors M1, M2 and M3 are 1/1 (or 1/2), 3/1 and 5/1 respectively as shown in figure 3.

III. Simulation and Performance Analysis of the 3T XOR Gate

In order to analyze the compare the performance of the proposed XOR gate with previously reported XOR gates, extensive simulation studies have been carried out on the different types of XOR gates. Each circuit is simulated with the same testing conditions. The netlists of those XOR gates are extracted and simulated using HSPICE. Since a circuit responds differently to different input combinations, so we use four input patterns to cover all input combinations.

The circuits are simulated with a 25MHz waveform with rise and fall times of 500ps.The power delay product has been computed by multiplying the average power with the average delay. The results of simulation are displayed in table I.

TABLE I
SIMULATION RESULTS OF XOR GATES

Type of XOR gate	Technology	Average Power (μW)	Average Delay (ps)	PDP (10^{-18}J)
6T [3]	0.15μm	2.316	15.021	34.788
4T (Fig. 1(a))	0.15μm	0.499	48.267	24.085
4T (Fig. 1(b))	0.15μm	0.486	68.738	33.407
4T (Fig. 1(c))	0.15μm	0.140	35.914	5.028
4T (Fig. 1(d))	0.15μm	0.434	9.083	3.942
3T	0.15μm	0.435	2.358	1.026
6T [2]	0.35μm	8.903	60.094	535.017
4T (Fig. 1(a))	0.35μm	1.623	69.497	112.794
4T (Fig. 1(b))	0.35μm	1.513	8.787	13.294
4T (Fig. 1(c))	0.35μm	1.246	35.901	44.733
4T (Fig. 1(d))	0.35μm	1.238	8.712	10.785
3T	0.35μm	1.240	6.088	7.549

The simulation results indicate that the power dissipation of the three transistor XOR gate is slightly more than that of the four transistor XOR gate shown in figure 1(d), but it has a much less delay than the four transistor XOR gate so that it has a much less power-delay product than the four transistor XOR gate. The sacrifice of a small amount of power for a considerable minimization of delay has also been found on other contemporary designs [20].

The noise margin of the XOR gate in the different technologies has also been studied. The results are shown in table II. The noise margin of the proposed XOR gate indicates quite comparable values with its peer designs.

Figure 5 shows the waveforms for the three-transistor XOR gate realized using (a) 0.15μm technology and (b) 0.35μm technology.

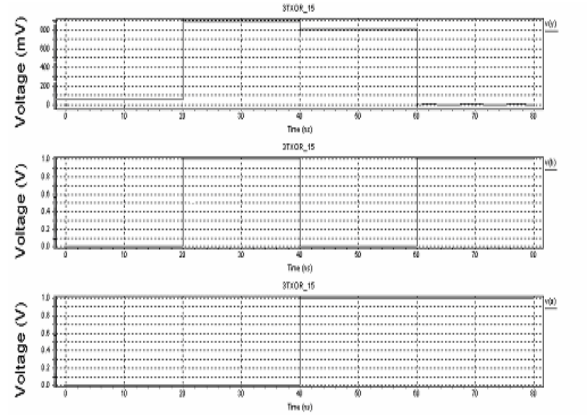


Fig. 5(a)

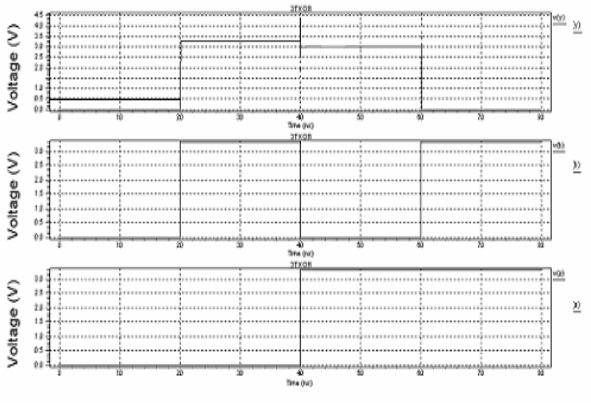


Fig. 5(b)

Fig. 5 Input and output waveforms of 3T XOR gate in (a) 0.15μm technology and (b) 0.35μm technology

The waveforms indicate that except for b=0 combinations, the output waveforms have a value of 1.0V in 0.15μm technology and 3.3V in 0.35μm technology which is equal to the input pulse values. For b=0, there is a small threshold drop of 0.143V in 0.15μm technology and 0.516V in 0.35μm technology across the PMOS pass transistor M3 which causes

TABLE II
NOISE MARGIN OF 3T XOR GATES

Type of XOR gate	Technology (μm)	V_{OH} (V)	V_{OL} (V)	V_{IH} (V)	V_{IL} (V)	NM_H (V)	NM_L (V)
6T [2]	0.15	1.000	0.000	0.550	0.480	0.450	0.480
4T (Fig. 1(a))	0.15	1.000	0.000	0.700	0.350	0.300	0.350
4T (Fig. 1(b))	0.15	1.000	0.000	0.700	0.350	0.300	0.350
4T (Fig. 1(c))	0.15	1.000	0.000	0.600	0.400	0.400	0.400
4T (Fig. 1(d))	0.15	1.000	0.000	0.580	0.450	0.420	0.450
3T	0.15	1.000	0.000	0.600	0.400	0.400	0.400
6T [2]	0.35	3.300	0.000	1.940	1.410	1.360	1.410
4T (Fig. 1(a))	0.35	3.300	0.000	2.180	1.160	1.120	1.160
4T (Fig. 1(b))	0.35	3.300	0.000	2.100	1.180	1.200	1.180
4T (Fig. 1(c))	0.35	3.300	0.000	2.070	1.230	1.210	1.210
4T (Fig. 1(d))	0.35	3.300	0.000	2.098	1.202	1.202	1.202
3T	0.35	3.300	0.000	2.075	1.220	1.225	1.220

a small degradation in the output voltage with respect to the full scale input voltage value. However, we shall be using this threshold drop advantageously in realizing the full adder, as we shall see later.

IV. Design of the Eight Transistor Full Adder

In this paper, we propose the design of a novel eight transistor full adder using novel three transistor XOR gates. The design of the three transistor XOR gate has already been described in the preceding section. The Boolean equations for the design of the eight transistor full adder are as follows:

$$Sum = A \oplus B \oplus Cin \quad (1)$$

$$Cout = BCin + CinA + AB = Cin(A \oplus B) + AB \quad (2)$$

The logic circuit of the full adder is shown in figure 6:

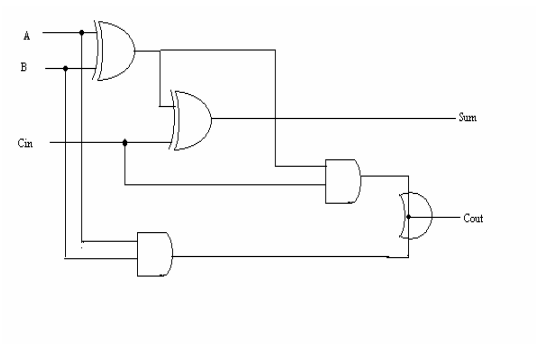


Fig. 6 Logic Circuit of the full adder

The OR gate can be realized using a wired OR logic [23]. The circuit diagram of the eight transistor full adder is shown in figure 7:

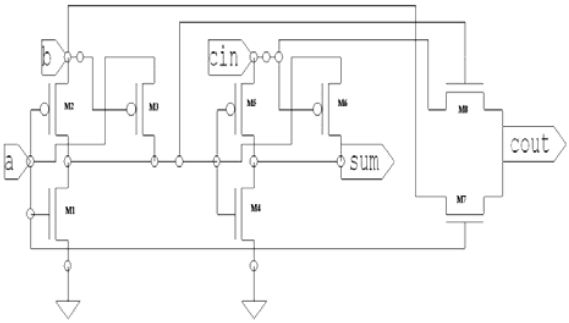


Fig. 7 Design of the eight transistor full adder

The sum output is basically obtained by a cascaded exclusive ORing of the three inputs in accordance with equation 1. The carry output is obtained in accordance with equation (2). The final sum of the products is obtained using a wired OR logic. The W/L ratios of transistors M1-M6 are same as the corresponding ones in figure 3. The W/L ratios of transistors M7 and M8 are taken as 5/1. It is quite evident from figure 6 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain the carry output which obviously stands out to be smaller than the circuit shown in figure 2. The design has been done using 0.15µm and 0.35µm technologies to establish the technology independence of the proposed design. The voltage drop due to the threshold drop in transistors M3 and M6 in figure 7 can be minimized by suitably increasing the aspect ratios of the two transistors. However, the threshold voltage drop of $|V_{T,p}|$ provided by the pMOS pass transistor M3 when a=0 and b=0 is used to turn on the nMOS pass transistor M8 and therefore we get an output voltage equal to $|V_{T,p}|-V_{T,n}$, where $V_{T,p}$ is the threshold voltage of the pMOS transistor and $V_{T,n}$ is the threshold voltage of the nMOS transistor. The difference value is very close to 0V. Similarly, the threshold drop of the transistors M7 and M8 can be minimized by suitably increasing the aspect ratios of transistors M7 and M8.

V. Layout Design of the Proposed 8T Full Adder

The layout of the proposed 8T full adder has been designed and simulated. The designed layout using 0.35 µm technology using TSMC035 is shown in figure 8.

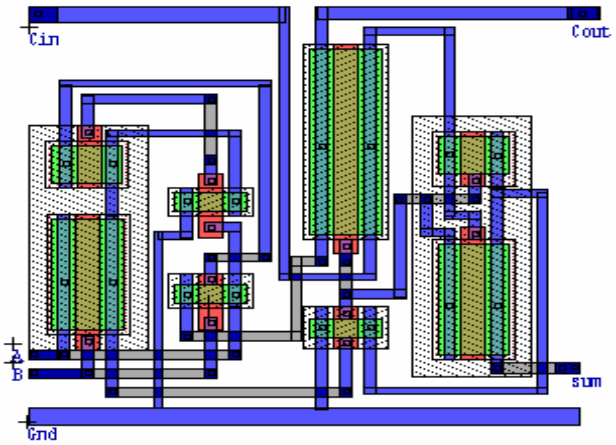


Fig. 8 Layout of the proposed 8T full adder

In order to make the layout symmetric, the big sized PMOS transistors have been laid on two n-wells with the NMOS transistors on the p type substrate in between. Moreover, since the interconnect density is low as evident from figure 8, itself, it also leads to a low power implementation of the adder [24].

VI. Simulation and Performance Analysis of the 8T Full Adder

The post layout simulation of proposed eight transistor full adder has been carried out with all combinations of inputs. Each circuit is simulated with the same testing conditions. The netlists of those XOR gates are extracted and simulated using HSPICE. Since a circuit responds differently to different input combinations, so we use eight input patterns to cover all input combinations. The circuits are simulated with a 25MHz waveform with rise and fall times of 500ps. The input-output waveforms for the eight transistor full adder are shown in figure 9.

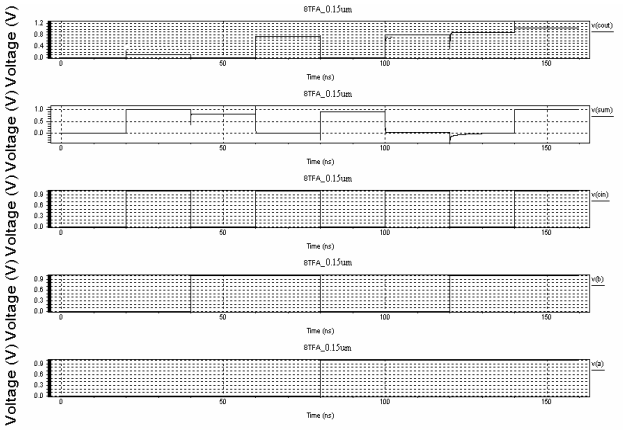


Fig. 9 (a)

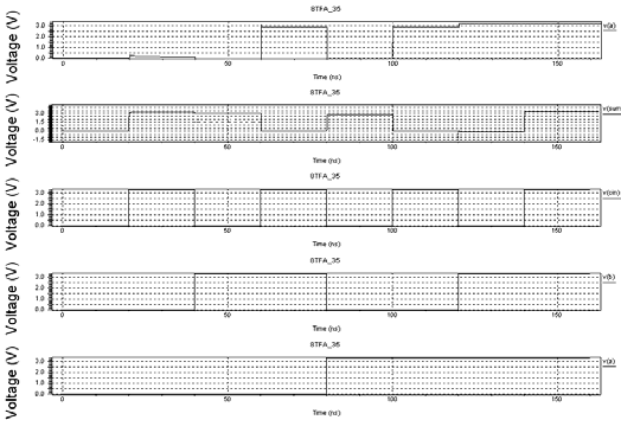


Fig. 9 (b)

Fig. 9 Post layout simulation results of the eight transistor full adder using (a) 0.15μm technology and (b) 0.35μm technology

The output waveforms show small voltage degradation for some input combinations. However these degradations can be minimized by use of CMOS inverters as level restorers at appropriate places in the circuit [20, 25]. Such type of level restoring logic is required in a long cascading chain of adders so that the penalty paid in silicon area for introducing two transistors of the CMOS inverter is minimal. The proposed full adder has been found to operate faithfully at an input voltage as low as 0.7V when using the 0.15μm technology, at an input voltage as low as 2.8V using 0.35 μm technology.

Comparative studies on the different adders found in literature have been done using the 0.15 μm and 0.35 μm technologies. Studies have been done with 28T, 20T, 16T, 14T, 10T and the proposed 8T full adders. The results have been shown in table III.

The results of the comparative study show that the performance of the 8T full adder is somewhat poorer than the 10T full adder proposed in [20], in regard to its average power dissipation. However, the delay of the proposed adder is much less compared to any other adder shown in the table 3. The net effect is that our proposed 8T full adder shows a much better power-delay product (PDP) compared to any other adders mentioned in literature. The sacrifice of a small amount of power for a considerable gain in delay has also been found on other contemporary designs [20].

TABLE III
COMPARATIVE STUDIES OF POWER-DELAY PRODUCT OF DIFFERENT ADDERS

Type of adder	Technology (μm)	Average Power (μW)	Delay (ps)	PDP (10^{-18} J)
28T [13]	0.15	1.154	39.491	45.573
20T [14]	0.15	0.858	28.623	24.558
16T [18]	0.15	0.760	32.142	24.421
14T [17]	0.15	1.171	18.481	21.641
10T [20]	0.15	0.321	29.481	9.463
8T	0.15	0.361	1.372	0.495
28T [13]	0.35	1.281	180.183	230.814
20T [14]	0.35	1.140	111.242	126.816
16T [18]	0.35	1.014	124.321	126.061
14T [17]	0.35	1.325	79.510	105.351
10T [20]	0.35	0.403	122.438	49.342
8T	0.35	0.409	1.651	0.675

A comparative study of the silicon area of the proposed adder with the earlier designed adders10 transistor full adder [18] is shown in table IV.

TABLE IV
COMPARATIVE STUDY OF THE AREA OF THE DIFFERENT ADDERS

Type of adder	Technology	Area (μm^2)
28T [13]	0.15μm	6.20
20T [14]	0.15μm	4.50
16T [18]	0.15μm	3.50
14T [17]	0.15μm	3.15
10T [20]	0.15μm	2.80
8T	0.15μm	2.10
28T [13]	0.35μm	31.45
20T [14]	0.35μm	23.15
16T [18]	0.35μm	18.26
14T [17]	0.35μm	15.95
10T [20]	0.35μm	15.12
8T	0.35μm	14.51

From table 4, it is evident that the proposed 8T full adder occupies the minimum silicon area on chip amongst all the full adders reported so far. The small silicon area of the proposed full adder makes it potentially useful for building compact VLSI circuits on a small area of chip.

VII. CONCLUSION

The current work proposes the design of an 8T full adder, which is by far the full adder with the lowest transistor count. In designing the proposed 8T full adder, a novel 3T XOR gate has also been proposed. The noise margins of the proposed XOR gate has been studied and found to have quite acceptable

values. The proposed XOR gate also has a much less delay and hence much less power delay product than its peer designs. The proposed XOR gate has been designed and studied using 0.15µm and 0.35µm technologies, which establish the technology independence of the proposed XOR gate. Using the XOR gate an eight- transistor adder has been realized using the conventional logic equations of the full adder circuit. The designed adder is found to give better performance than most of the adders mentioned in literature so far as the power-delay product is concerned. The layout of the proposed full adder has also been designed and simulated. The proposed full adder can operate at low voltages, yet giving quite a good speed.

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