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A Low Power SRAM Base on Novel Word-Line Decoding

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***Abstract*—**This paper proposes a low power SRAM based on five transistor SRAM cell. Proposed SRAM uses novel word-line decoding such that, during read/write operation, only selected cell connected to bit-line whereas, in conventional SRAM (CV-SRAM), all cells in selected row connected to their bit-lines, which in turn develops differential voltages across all bit-lines, and this makes energy consumption on unselected bit-lines. In proposed SRAM memory array divided into two halves and this causes data-line capacitance to reduce. Also proposed SRAM uses one bit-line and thus has lower bit-line leakage compared to CV-SRAM. Furthermore, the proposed SRAM incurs no area overhead, and has comparable read/write performance versus the CV-SRAM. Simulation results in standard 0.25µm CMOS technology shows in worst case proposed SRAM has 80% smaller dynamic energy consumption in each cycle compared to CV-SRAM. Besides, energy consumption in each cycle of proposed SRAM and CV-SRAM investigated analytically, the results of which are in good agreement with the simulation results.

***Keywords*—**SRAM, write Operation, read Operation, capacitances, dynamic energy consumption.

I. Introduction

DUE to the high demands on the portable products, energy consumption is a major concern in VLSI chip designs. Especially, the low power static random access memory (SRAM) becomes more important because the number of memory cells and the bit width continue to be larger.

A six-transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell. However, conventional SRAMs (CV-SRAM) based on this cell has large word-line and data-line capacitances, specially when the memory array size is high, thus in high frequency operation dynamic power consumption is very large and this is not useful for long time battery operation in mobile applications. Since, in each column of memory array in CV-SRAM there are two bit-line, therefore there are two leakages current from pre-charged bit-lines to ground through the access transistors of cells [1].

One major source of dynamic energy consumption in CV-SRAM is, whenever word-line asserted in one row of memory array, all cells in selected row connected to their bit-lines, which in turn develops differential voltages across all bit-lines, whereas one cell of connected cells to their bit-lines selected by column decoder for read/write operation and other unselected [2]. Conventionally hierarchical word-line decoding architecture used to reduce the number of unselected cells to save power on unselected bit-line in CV-SRAM [3]. In this architecture, cells in each row divided to several group and only, cells in selected group connected to their bit-lines. But this architecture needs extra logics in each row of memory array and this incurs considerable area overhead, especially when memory array size is high. Furthermore, in hierarchical word-line decoding architecture all cells in selected group connected to their bit-lines and this causes energy consumption in unselected bit-line in each group.

In this paper we describe new architecture for SRAMs based on five-transistor SRAM cell (5T SRAM cell). This new architecture uses novel word-line decoding such that, whenever word-line asserted in one row of memory array, only selected cell connected to bit-line. Hence dynamic energy consumption decreased. New architecture is based on a 5T SRAM cell and data-line capacitance reduced in this architecture. 5T SRAM cell used one bit-line and one access transistor, and thus new architecture has low bit-line leakage [4].

II. Low Power SRAM Architecture

Fig. 1 shows the architecture of one column in purposed SRAM and Fig. 2 shows overall architecture of purposed SRAM. In this architecture memory array divided into two halves thus during read/write operation only one of these halves selected by column decoder for read or write operation.

New SRAM uses novel word-line decoding. In this novel word-line decoding for each cell in memory array, we add one PMOS transistor with low threshold voltage. Our purpose from additional transistors is when word-line asserted in a row of memory array for selecting one cell during read/write operation, only selected cell connected to its bit-line as shown in Fig. 1. These results in very low energy consumption during read/write operation. Also the threshold voltage of additional PMOS transistor must be chosen as low as possible for smaller bit-line leakage. Since, new SRAM uses 5T cell,

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the additional transistors incur no any area overhead compared to CV-SRAM with same size.

The 5T cell has only one access transistor and single bit-line. The write ability of the cell is ensured by different cell sizing strategy [4]. In this cell for non-destructive read operation the bit-line pre-charged to 1V [4]. Intermediate pre-charge voltage, V_{PC}=1V requires an on-chip DC-DC converter or external power supply [4].

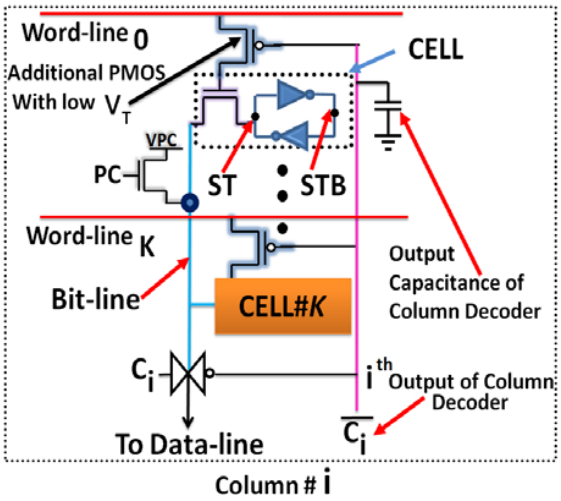

Fig. 1 Architecture of one column in purposed SRAM (PC is pre-charge control)

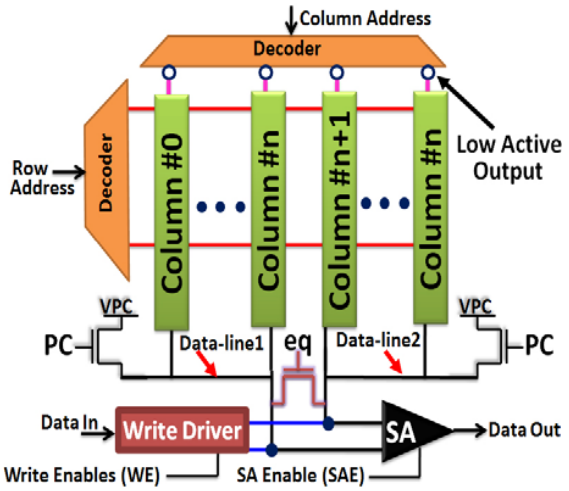

Fig. 2 Architecture of purposed SRAM (PC is pre-charge control, SA is sense amplifier, and eq is equalization control)

III. Read and Write Operation

When a write operation is issued the memory array will go through the following steps: 1) Row and column address decoding: the row address decoded for selecting a word-line. Also column address decoded for connecting a selected bit-line to selected data-line. 2) Bit-line driving: For a write, this bit-line driving conducts simultaneously with the row and column address decoding by turning on proper write buffer. After this step, selected data-line and bit-line will force into '1' or '0' logic level. 3) Cell flipping: If the value of the stored bit in the target cell is opposite to the value being written, then cell flipping process will take place. 4) Pre-charging: At the end of write operation all bit-lines and data-lines pre-charged to V_{PC}=1V. Also data-lines equalized and memory array gets ready for next read/write operation.

When a read operation is issued the memory will go through the following steps: 1) Row and column address decoding: the row address decoded for selecting a word-line. Also column address decoded for connecting a selected bit-line to data-line. 2) Bit-line deriving: After the word-line go to high voltage, and the target cell connected to its bit-line. The so-called cell current through the driver or load transistor of target cell will discharge or charged the voltage of bit-line progressively, and this resulted a change on bit-line and consequently on selected data-line. 3) Sensing: After word-line return to low voltage, the sense amplifier is turned on to amplify the small difference voltage between data-lines into full-swing logic signal. 4) Pre-charging: At the end of read operation all bit-lines and data-lines pre-charged to V_{PC}=1V. Also data-lines equalized and memory array gets ready for next read or write operation.

IV. Layout Design

Fig. 3 shows possible layout of 5T SRAM cell with additional PMOS transistor in MOSIS scalable CMOS design rules. Also for comparison, Fig. 4 shows layout of 6T SRAM cell and 5T SRAM cell with additional PMOS transistor in MOSIS scalable CMOS design rules. The 6T cell has the conventional layout topology and is as compact as possible. 6T SRAM cell requires 25.35µm^2 area with λ=0.25µm, whereas 5T SRAM cell with additional PMOS transistor requires 25µm^2 area with λ=0.25µm. Also we design full custom layout for two memory arrays with size 1Kbit for purposed SRAM and CV-SRAM in MOSIS scalable CMOS design rules as shown in Fig. 5. The memory array of purposed SRAM requires 27.02mm^2 area with λ=0.25µm, whereas memory array of CV-SRAM requires 27.34mm^2 area with λ=0.25µm. Therefore purposed SRAM incurs no area overhead compared to CV-SRAM with same size. Also all layouts designed by using L-Edit tool.

V. Capacitances in SRAMs

There are four premier parasitic capacitances in CV-SRAM and newly SRAM. These capacitances include bit-line (C_{BL-New} and C_{BL-CV}), word-line (C_{WL-New} and C_{WL-CV}), data-line (C_{DL-New} and C_{DL-CV}) and output of column decoder ($C_{out-Decoder}$). Later capacitance is considerable in new SRAM and we consider this capacitance only for new SRAM. Also we ignored wiring capacitance of bit-line, data-line and word-line in all expressions. The bit-line capacitance in CV-SRAM and new SRAM is mainly composed of the drain junction capacitance of pass transistors and this capacitance estimates by following expressions.

$$C_{BL-CV} = C_{BL-New} \cong C_J \times 2^{Row} \quad (1)$$

Where, C_J is drain junction capacitance of pass transistor of memory cells and *Row* is number of address lines in row decoder. The next large capacitance in CV-SRAM and new SRAM is word-line capacitance. In CV-SRAM this capacitance is mainly composed of gate capacitance of the pass transistor of memory cell and in new SRAM this capacitance is mainly composed of junction capacitance of additional PMOS transistors. This capacitance estimates by following expressions.

$$C_{WL-CV} \cong 2 \times C_g \times 2^{Column} \quad (2)$$

$$C_{WL-New} \cong C_{J-Add-P} \times 2^{Column} + C_g \quad (3)$$

Where, C_g is gate capacitance of pass transistor of memory cell, $C_{J\text{-}Add\text{-}P}$ is junction capacitance of additional PMOS transistor, and *Column* is number of address lines in column decoder. The next large capacitance in CV-SRAM and new SRAM is data-line capacitance and this capacitance is mainly composed of junction capacitance of access column transistors and estimates by following expressions.

$$C_{DL-CV} \cong C_{J\_ColumnAccess} \times 2^{Column} \quad (4)$$

$$C_{DL1-New} = C_{DL2-New} \cong C_{J\_ColumnAccess} \times 2^{Column-1} \quad (5)$$

Where, $C_{J\text{-}ColumnAccess}$ is drain junction capacitance of column access transistors and *Column* is number of address lines in column decoder. From expressions (5) and (4) it is quite clear that data-line capacitance of new SRAM is smaller than data-line capacitance of CV-SRAM, since number of column access transistor connected to data-line1 or data-line2 reduced in new SRAM. Finally the next capacitance that considerably in new SRAM is output capacitance of column decoder. This capacitance is due to gate capacitance of additional PMOS transistors (attention to Fig. 1) and estimates from following expression.

$$C_{Out\_Decoder} \cong C_{g-Add-P} \times 2^{Row} \quad (6)$$

Where, $C_{g\text{-}Add\text{-}P}$ is gate capacitance of additional PMOS transistor, and *Row* is number of address lines in row decoder.

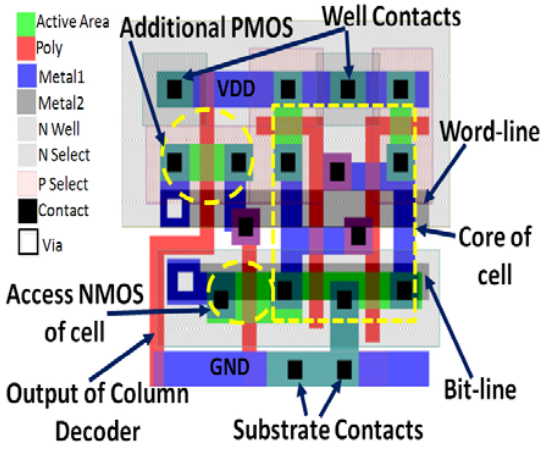

Fig. 3 Possible layout of 5T SRAM cell with additional PMOS

VI. Dynamic Energy Consumption in SRAMs

The In each cycle of SRAMs, a read or write operation performs. Therefore dynamic energy consumption in SRAMs consumes due to the charging and discharging capacitances during read/write operation. Thus during each cycle of SRAMs a certain amount of energy is drawn from the power supply and dissipates. The amount of energy consumption in each cycle depends on type of operation in current cycle. Furthermore, when the capacitor charged from GND to V_{DD} and then discharged to GND, amount of energy is drawn from the power supply and dissipated, equals $C_L V_{DD}^2$ [5]. And stored energy on the capacitor C_L with voltage V_C equals $\frac{1}{2} C_L V_C^2$. Thus whenever the capacitor C_L charged from V_C to V_{DD} and then discharged to V_C amount of energy drawn from the power supply and dissipated, obtains by following expression.

$$E_{Supply} = C_L(V_{DD}^2 - V_C^2) \quad (7)$$

In CV-SRAM, the best case of energy consumption of each current cycle occurs when a read operation performs in current cycle. Thus during current cycle (a read operation) of CV-SRAM word-line charged form GND to V_{DD} and then discharged to GND and bit-lines and data-line from V_{DD} discharged to $V_{BL\text{-}Read}$ and then charged to V_{DD}. Therefore the best case energy consumption of each cycle in CV-SRAM estimates by following analytical expression.

$$E_{BC-CV} \cong C_{WL-CV} V_{DD}^2 + C_{DL-CV} \times (V_{DD}^2 - V_{BL\text{-}Read}^2) + 2^{Column}\left[C_{BL-CV} \times (V_{DD}^2 - V_{BL\text{-}Read}^2)\right] \quad (8)$$

Where, $V_{BL\text{-}Read}$ is voltage of bit-lines and data-line just after word-line activation in read operation.

In new SRAM, the worst case of energy consumption of each current cycle occurs when in current cycle a write operation with data '1' will be performed. Thus during current cycle (write operation with data '1') of new SRAM word-line charged from GND to V_{DD} and then discharged to GND, output of column decoder from GND charged to V_{DD} and discharged to GND, and selected bit-line and data-line1 (or data-line2) charged from V_{PC} to V_{DD} and then discharged to V_{PC}. Thus the analytical worst case energy consumption after each cycle in new SRAM obtained by following expression.

$$E_{WC\text{-}New} \cong (C_{WL\text{-}New} + C_{out\text{-}Decoder}) \times V_{DD}^2 + (C_{DL1\text{-}New} + C_{BL-NEW}) \times (V_{DD}^2 - V_{PC}^2) \quad (9)$$

Fig. 6 shows the worst case energy consumption of new SRAM and best case energy consumption of CV-SRAM in each cycle, according to size of memory array in standard 0.25µm CMOS technology and with parameters listed in Table 1. As shown in Fig. 6 dynamic energy consumption in each cycle of new SRAM is very smaller than CV-SARM. On the average analytical worst case energy consumption of new SRAM is %89 smaller than analytical best case energy

consumption of CV-SRAM.

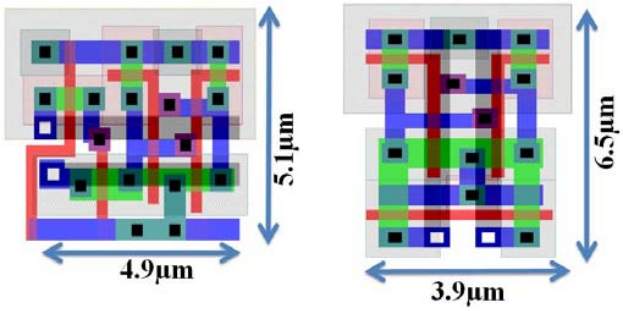

Fig. 4 Layout of 6T SRAM cell and 5T SRAM cell with additional PMOS

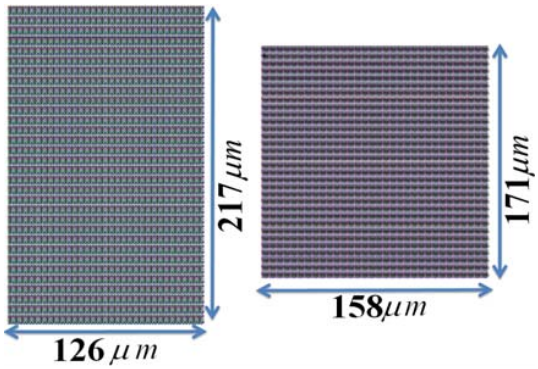

Fig. 5 Fully custom layout for two memory arrays

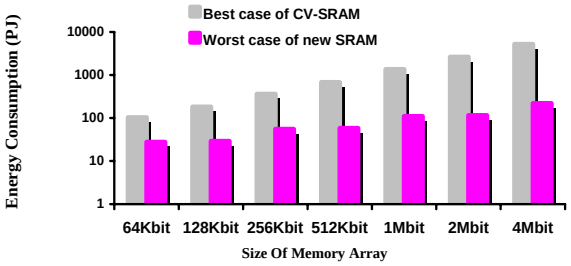

Fig. 6 Analytical best case and worst case energy consumption in each cycle of CV-SRAM and new SRAM

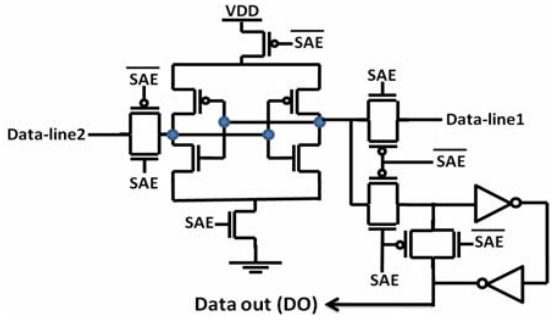

Fig. 7 Circuit schematic of sense amplifier

VII. Simulation Results

To verify correct operation of new SRAM, and delay comparison with CV-SRAM, we simulate a new SRAM and CV-SRAM with size 256Kbit using HSPICE in standard 0.25µm CMOS technology with 2.5V for supply voltage and 0.5V for threshold of additional PMOS transistor. For optimizing the delay of row and column decoders pre-decoding scheme has been used in proposed SRAM and CV-SRAM [1]. Based on layouts Fig. 4, all parasitic capacitances and resistances of bit-lines, data-lines and word-lines are included in the circuit simulation. Fig. 7 shows circuit schematic of the sense amplifier used in new SRAM and CV-SRAM and Fig. 8 shows circuit schematic of the write driver used in new SRAM and CV-SRAM uses convectional write driver. For test the correctness of read and write operation of new SRAM, following scenario applied to new SRAM.

- Writing '0' in to one cell and then read it
- Writing '1' in to one cell and then read it

Fig. 9 and Fig. 10 show simulated waveform from applying above scenario. Table II shows delay comparisons of new SRAM and CV-SRAM.

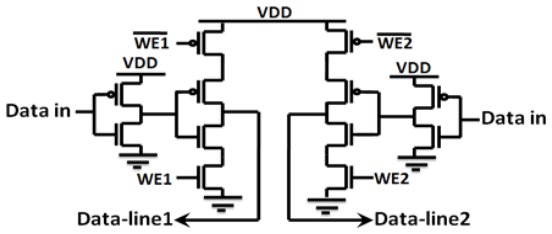

Fig. 8 Circuit schematic of write driver

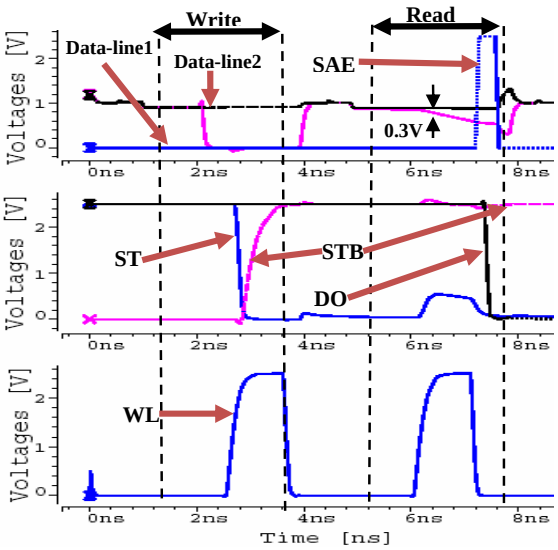

Fig. 9 Simulated waveform of write '0' and read '0' (SAE is sense amplifier enable, OSA is sense amplifier output, and WL is word-line and ST and STB specified in Fig. 1)

Also to evaluate the effectiveness of new SRAM for saving dynamic energy consumption and precision of derived analytical expressions, based of layouts Fig. 4 we simulate read/write operation of new SRAM, CV-SRAM for different size of memory array in standard 0.25µm CMOS technology. On the average simulated worst case energy consumption of

new SRAM is %80 smaller than simulated best case energy consumption of CV-SRAM. Thus the simulation results are in good agreement with the analytical expressions and proposed new SRAM has great potential to save the dynamic energy consumption, especially when dimensions of memory array are high.

VIII. Conclusion

This paper presents a low power SRAM. In novel SRAM for each column there is one bit-line. We add PMOS transistor with low threshold voltage for each cell. Our purpose from additional transistors is, whenever one row selected in new SRAM, only on cell connected to bit-line. And thus dynamic energy consumption reduced. Since we use 5T cell there is not any overhead constrain compared to conventional SRAM with same size. Furthermore in this paper we present explicit analytic expressions for estimating the capacitances and dynamic energy consumption in proposed SRAM and CV-SARM. Simulation results in standard 0.25µm CMOS technology show that this new SRAM have great potential to save the dynamic energy consumption. And the purposed SRAM has comparable read/write performance versus CV-SRAM.

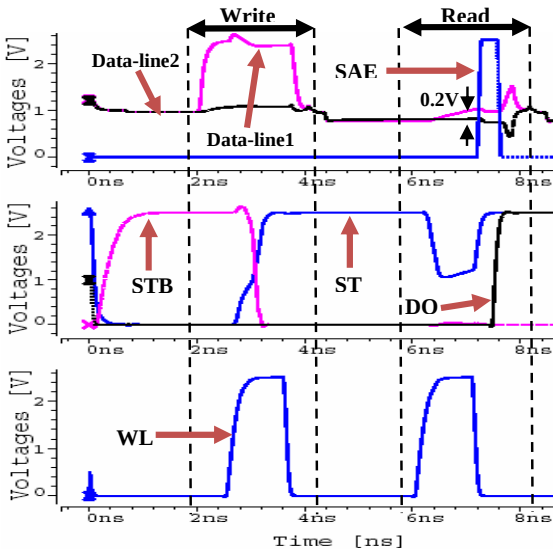

Fig. 10 Simulated waveform of write '1' and read '1'

TABLE I
Parameter Values Used in Analytical Expressions

Symbol	Parameter	Value
V_{DD}(V)	Supply voltage	2.5
V_{PC}(V)	Pre-charge voltage	1
$V_{BL\text{-}Read}$	Voltage of bit-lines after word-line activation during read in CV-SRAM	2.25

TABLE II
Delay Comparison of SRAMs

Metrics	CV-SRAM	New SRAM
Read delay (word-line high to equalization)	2.1 ns	2.2ns
Write delay (data-line driving to equalization)	1.9ns	2.1ns

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