

Decoder Design for a New Single Error Correcting/Double Error Detecting Code

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Abstract—This paper presents the decoder design for the single error correcting and double error detecting code proposed by the authors in an earlier paper. The speed of error detection and correction of a code is largely dependent upon the associated encoder and decoder circuits. The complexity and the speed of such circuits are determined by the number of 1's in the parity check matrix (PCM). The number of 1's in the parity check matrix for the code proposed by the authors are fewer than in any currently known single error correcting/double error detecting code. This results in simplified encoding and decoding circuitry for error detection and correction.

Keywords—Decoder, Hsiao code, Parity Check Matrix, Syndrome Pattern.

I. INTRODUCTION

SINGLE bit error correcting and double-bit error detecting (SEC/DED) codes are widely used in computer memory systems. An SEC/DED code has a minimum Hamming distance of 4. One such code is the Hsiao code [1]. It uses multiple parity bits to uniquely identify an erroneous bit in a code word as well as to define the error-free condition.

In Hsiao code the columns corresponding to the information bits are assigned all combinations of 3-out-of- k bits, where k is the number of check bits; this is followed by all combinations of 5-out-of- k bits and then by 7-out-of- k bits and so on until all information bits have unique columns. The check bits are assigned 1-out-of- k code words. The equations for the check bits in the PCM are derived by taking the linear sum (EX-OR) of all the information bits with 1s in a row in which the check bit is also a 1. A single bit error results in a syndrome pattern that matches a column of the PCM. Thus, matching a syndrome pattern to a column in the PCM can identify an erroneous bit. If the column corresponds to a check bit, then no correction is necessary. However, for maintenance purposes the error information is logged. Since the Hsiao code uses only odd number of 1's in the columns of its PCM, a

syndrome pattern corresponding to a single bit error has odd parity. If the syndrome has an even parity, the presence of a double bit error in a code word is indicated.

The speed of error detection and correction in a code is largely dependent upon the associated encoder and decoder circuits. The complexity and the speed of such circuits are determined by the number of 1's in the parity check matrix (PCM). The fewer the number of 1's in the PCM the less complex the encoding and decoding circuits are; fewer 1's also enhance the speed of these circuits [2]. Among all the well-known SEC/DED codes the Hsiao code has the minimum number of 1's in the PCM [3].

A new coding technique for single bit error correction and double bit error detection has been proposed in Ref.[4]. It differs from the Hsiao code in that columns are assigned m-out-of- k code where $m \leq k$, with all combinations of 2-out-of- k chosen first followed by increased values of m till all columns get unique code words; it also appends to each column two residue bits that are set to the mod-3 residue of the number of 1's in the corresponding column. Two columns are also incorporated, one for each residue bit. Each of these columns is assigned a 1-out-of- $(k+2)$ code word such that together with other assigned check bits they form a identity submatrix. The PCM for the proposed code is constructed as follows:

i. Assuming k check bits ($c_{k-1}, c_{k-2}, \dots, c_1, c_0$) and two residue bits (r_1, r_0), a $(k+2)$ -bit column with a single 1 is assigned to the check bit c_i and residue bit r_j .

ii. If the length of the information bits is n and ${}^kC_2 \leq n$ then n columns out of kC_2 are selected. If ${}^kC_2 = n$, all kC_2 columns are selected.

iii. If ${}^kC_2 < n$, all kC_2 columns are selected; the remaining columns are selected first from kC_3 columns, then from among kC_4 columns and so on. This process is continued till all n columns in the PCM have been specified.

iv. Append two bits to each column of the information bits by taking the mod-3 residue of the sum of the number of 1's in the columns corresponding to the information bits. Every PCM column is treated as a binary number and the top most bit is considered as the least significant bit.

To illustrate let us assume $d_7d_6d_5d_4d_3d_2d_1d_0 = 11010000$. The corresponding check/residue bits are $r_1r_0c_3c_2c_1c_0 = 101010$. The PCMs for other $(n+k+2, n)$ codes, where n is the number of information bits, can be derived in a similar manner. For example, the PCMs for the $(41, 32)$ is shown in Fig. 1.

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00100110001000001100001000001110	000000001
0000100101000000101111001111010	000000010
1000010000100110001000010010001	000000100
0001100010110100000001010010100	000001000
01100001100000010010000101100100	000010000
10000100000011000010111011010000	000100000
01010000010010101000000110000111	001000000
0000000000000000000000000000000	010000000
11111111111111111111100000000000	100000000

Fig. 1 PCM for the (41, 32) Code

The error detection and correction strategy for a single bit error in the proposed code is similar to that in the Hsiao code. A single bit error will produce a syndrome pattern, $(k + 2)$ bits that matches a column in the PCM, the parity of the pattern is not important. Note the last two syndrome bits, m_1m_0 , will be referenced as the residual syndrome bits from here onwards. In other words, the last two bits of every column in the PCM will be referenced as residual syndrome bits. The double error detection approach in the proposed code is different than in Hsiao code where a double bit error produces a syndrome pattern that has even parity. In the proposed code the double error detection is based on the following three lemmas proposed in [4]:

Lemma 1: A double bit error composed of two erroneous information bits in a code word will result in the residual syndrome bits to be 11 if one of the corresponding columns in the PCM has 01 in the last two bits and the other one has 10.

Lemma 2: A syndrome pattern with p 1's in the first k bits of a syndrome pattern where p is greater than the highest m in the m -out-of- k code words assigned to each bit in the PCM, indicates a double or a multi bit error in a code word.

Lemma 3: A syndrome pattern with 00, 01 or 10 in the residual syndrome bits, m_1m_0 , indicates a double bit error if the recomputed mod-3 residue bits of the first k syndrome bits, $m_1'm_0'$, are not 00, 01 or 10, respectively.

The following lemma only applies to information bits up to 256 bits ($^{10}C_2 + ^{10}C_3 + ^{10}C_4$).

Lemma 4: A syndrome pattern that does not have 10 at the residual syndrome bits, m_1m_0 , indicates a double bit error if the sum of 1's of the first k syndrome bits is exactly 2.

Proof: The mod-3 residue bits of a column in the PCM can only be 10 if the number 1's in the other bits of the column is equal to two. A syndrome with two 1's in the first k bits does not guarantee a single bit error since a double bit error can also produce two 1's. Table I shows all double bit errors that generate two 1's in the first k bits of the syndrome pattern along with the residual syndrome bits. ■

The first two columns in Table I show the number of 1's in the error patterns corresponding to a double bit error. The third column states whether there exists a possibility of two 1's in the first k syndrome bits given that the first erroneous pattern only has s_i number of 1's in its first k bits and the seconds

TABLE I
ANALYSIS OF SYNDROME BITS DUE TO DBE

s_i^a	s_i^b	Possibility	m_1m_0
1	1	YES	00
2	1	NO	n/a
2	2	YES	00
2	3	NO	n/a
2	4	YES	11
3	1	YES	00
3	2	NO	n/a
3	3	YES	00
3	4	NO	n/a
4	1	NO	n/a
4	2	YES	11
4	3	NO	n/a
4	4	YES	00

erroneous pattern only has s_i number of 1's in its first k bits. The fourth column indicates the value of the residual syndrome bits should there be a possibility of two 1's in the first k bits of the syndrome pattern in the presence of a double bit error. In the absence of a possibility of two 1's in the first k bits of the syndrome pattern, as noted in the third column using 'NO', the corresponding fourth column value is 'n/a'. In the presence of two 1's in the first k bits of the syndrome pattern, the resulting residual syndrome bit is either 00 or 11 and not 10. Using Table I, it can be concluded that only single bit errors with two 1's in the first k syndrome bits can have 10 in the residual syndrome bits.

Similarly, it can be shown that a syndrome pattern that does not have 01 or 00 at the residual syndrome bits indicates a double bit if the sum of 1's of the first k syndrome bit is exactly 4 or 3, respectively.

A major advantage of the code in [4] is the number of 1's in the PCM is fewer than that in the Hsiao code except when $k = 16$ or 32 in which case the number of 1's is almost the same as in Hsiao code. Table II shows the comparison of the number of 1's in the new code in Ref.[4] and the Hsiao code.

A procedure for correcting single bit errors and detecting double bit errors in an encoded word based on the proposed coding technique is given below:

- i. Calculate the syndrome $s = (m_1m_0s_{k-1} \dots s_0)$
- ii. If $(s_{k-1} \dots s_0)$ bits are all zero then there are no errors in the information/check bits of the word, exit. Else

TABLE II
NUMBER OF 1'S IN THE HSIAO PCM(HC) VS. THE NEW CODE (REF. 4)

n	k	HC	Ref.[4]
16	8	54	56
32	9	103	105
64	10	216	202
128	11	481	411
256	12	1050	962

- iii. Compute the mod-3 residue of the syndrome bits $s_{k-1} \dots s_0$; identify these as $m_1' m_0'$.
- iv. If $m_1 m_0 \neq 00$ and $(s_{k-1} \dots s_0)$ bits are all zero then Residue Bit Error (RBE) exists, exit.
- v. If $m_1 m_0 = 00$ and $(s_{k-1} \dots s_0)$ bits contain only a single 1, a check bit (CBE) identified by the syndrome pattern is erroneous, exit.
- vi. If $m_1 m_0 = 00$ and $m_1' m_0' = 00$ and the number of 1's in the first k syndrome pattern equals 3, a single bit error (SBE) is identified, decode.
- vii. If $m_1 m_0 = 01$ and $m_1' m_0' = 01$ and the number of 1's in the first k syndrome pattern equals 4, a single bit error (SBE) is identified, decode.
- viii. If $m_1 m_0 = 10$ and $m_1' m_0' = 10$ and the number of 1's in the first k syndrome pattern equals 2, a single bit error (SBE) is identified, decode.
- ix. There is a double bit error (DBE) in the code word, exit.

II. DECODER DESIGN FOR THE PROPOSED CODE

A block diagram of the decoder circuit is shown in Fig. 2. The inputs to decoder are original information/check/residue bits and output is corrected information bits in the presence of a single bit error. In the case of no error / check bit error / residue bit error / double bit error, the information bits go through the decoder without correction. The decoder consists of the following:

A. Syndrome Bit Generator (SBG)

The syndrome bits $m_1 m_0 s_{k-1} \dots s_0$ are calculated by EX-ORing the stored check/residue bits with the recomputed check/residue bits from information bits. The SBG only uses 2-input EX-OR gates and the total gate count, SBG_c , depends on the total number of 1's in the PCM, T . The relationship between the SBG_c and T is as follows:

$$SBG_c = T - (k + 2)$$

where k is the total number of check bits. The output of the SBG, syndrome bits $m_1 m_0 s_{k-1} \dots s_0$, are later used by the No Error Detector block, the 1's Counter block and the Single Bit Error Locator block. Note that the first k syndrome bits, $s_{k-1} \dots s_0$, are computed using original and recomputed check bits and the residual syndrome bits, $m_1 m_0$, use original and recomputed residue bits, $r_1 r_0$.

B. No Error Detection (NED)

Using the first k syndrome bits from the SBG the absence of errors can be identified. The NED block consists of only 2-input NOR gates and will output a 1 only if all k syndrome bits are 0's.

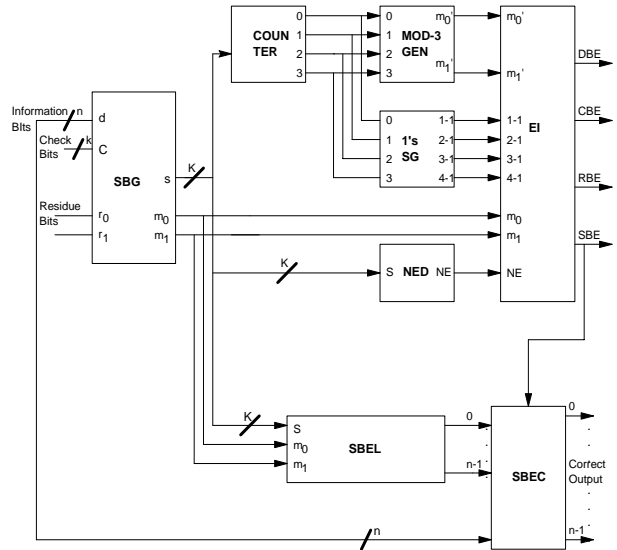


Fig. 2 Block diagram of the Decoder

C. 1's Counter (Counter)

This block counts the number of the 1's in the first k syndrome bits from the SBG block using only Half Adders. The output is a binary representation of the number of 1's in the first k syndrome bits.

D. 1's Signal Generator (SG)

Using the output from the 1's Counter, the SG block assigns individual outputs to binary representations of one, two, three, or four. To convert a binary representation of x bits to a single output, only $(x - 1)$ 2-input gates are needed. Thus the outputs of the SG block are 1-1, 2-1, 3-1, and 4-1; in other words one-1, two-1's, three-1's, and four-1's, respectively. During normal operation, only one output can be active at any given time.

E. MOD-3 Generator (M3G)

The MOD-3 Generator block also uses the output from the 1's Counter to compute the mod-3 residue of the sum of 1's in the first k bits of syndrome pattern, and these are denoted as $m_1' m_0'$. For $7 < k < 16$, only two 2-input EX-OR gates are needed. The proposed code uses these outputs in the Error Identifier block to primarily identify double bit errors.

F. Error Identifier (EI)

The EI block identifies the type of error or no error during each memory read cycle. The inputs to the EI block include the output from the NED block, the output from the SG block, the outputs from the M3G block, along with m_1 and m_0 . The outputs from the EI block are: Single Bit Error (SBE), Check Bit Error (CBE), and Residue Bit Error (RBE), as shown in Table III.

TABLE III
ERROR IDENTIFICATION

Inputs									Outputs		
m_0	m_1	m_0'	m_1'	1-1	2-1	3-1	4-1	NE	SBE	CBE	RBE
0	0	0	0	x	x	1	x	0	1	0	0
0	1	0	1	x	1	x	x	0	1	0	0
1	0	1	0	x	x	x	1	0	1	0	0
0	0	x	x	1	x	x	x	0	0	1	0
0	1	x	x	x	x	x	x	1	0	0	1
1	0	x	x	x	x	x	x	1	0	0	1

All other combinations yield a Double Bit Error (DBE) and this is the final output of the EI block. In Table III, x denotes *don't care*. A SBE is present when any of the following conditions are met:

- $m_1 = 0, m_0 = 0, m_1' = 0, m_0' = 0$ and $3-1 = 1$ or,
- $m_1 = 0, m_0 = 1, m_1' = 0, m_0' = 1$ and $2-1 = 1$ or,
- $m_1 = 1, m_0 = 0, m_1' = 1, m_0' = 0$ and $4-1 = 1$.

A CBE output is 1 when the first k bits of the syndrome has only one 1. The RBE identifies errors in the residue bits and becomes 1 whenever either m_0 or m_1 is 1 in the presence of no error. The EI block is implemented using twenty two 2-input gates and 5 inverters.

G. Single Bit Error Locator (SBEL)

This block is responsible for locating the erroneous bit based on the syndrome bits. The SBE Locator block identifies the erroneous bit in the presence of a SBE using the all bits of the syndrome patterns. It consists of 2-input EX-OR gates and 2-input AND gates. The total number of 2-input gates are proportional to the number of 1's in the PCM. In order to represent every PCM Column in the SBEL block we first need to identify which of the following cases is applicable:

Case 1: Only 2-out-of- k (where m equals 2) code is used in the PCM. This is the simplest case where a single AND gate can individually represent any PCM column.

Case 2: If $m = 2$ and 3, then both types of column will need two 2-input AND gate. For $m = 2$, two inputs to the AND gate correspond to the 1's from the first k bits of PCM column and the remaining input corresponds to the most significant residue bit. For $m = 3$, all three inputs to the AND gate correspond to the 1's in the first k bits of the PCM column.

Case 3: If m equals 2 and 3 and 4, then 2 and, 2 and 3 2-input AND gates are needed to represent individual PCM columns, respectively. For $m = 2$ and 3, see *Case 2*. For $m = 4$, all four inputs to the 2-input AND gate correspond to the 1's in the first k bits of the PCM column.

H. Single Bit Error Corrector (SBEC)

Using the SBE output from the EI block, the (SBEC) block gets enabled only if either SBE is 1. In the other cases, the information bits are transmitted without correction. The inputs to the SBEC block include all information bits, output from

the SBEL block along with the control output (SBE) from the EI block. The functionality of the SBEC block and SBEL block are identical to that used in [1]. In the presence of a SBE the SBEC block is enabled to correct the bit that is identified as erroneous by the SBEL block.

The method of obtaining the syndrome bits used was similar to Hsiao code and likewise the encoder can also be obtained from the first part of the decoder without using check bits as inputs. Additionally, the encoder also needs to compute the residue bits which are not required in the Hsiao encoder.

The proposed decoder significantly outperforms the decoder for Hsiao code for 64 or higher information bits in terms of 2-input gate count. In the following section, detailed analysis of the proposed code/decoder is presented.

III. DISCUSSION OF RESULTS

The total number of 2-input gates used for decoding is significantly less in the proposed code than in Hsiao code. Table IV compares the Hsiao decoder with the decoder for the proposed; only 2-input gates and inverters are used to implement the decoder.

In Table IV, the negative percentages indicate the improvements of the proposed code over Hsiao code. For information bits 64 or high there is a significant difference in the gate usage; this can be primarily attributed to the design of the SBEL block. In order to locate an erroneous bit, every bit position is represented by a small network of 2-input AND gates based on their respective PCM column. In a Hsiao decoder, with $n = 32$, the PCM only uses 3-out-of- k code and therefore every column of the PCM can be represented by only two 2-input AND gates. In contrast, when $n = 64$, the PCM uses 3-out-of- k code as well as 5-out-of- k code, this requires $(k-1)$ 2-input AND gates per PCM column, and in this case seven 2-input AND gates are needed since $k = 8$. If a bit error corresponds to a column with a 4-out-of- m code, then bit locations where m equals 2 or 3 will never be unintentionally corrected. This is because both of these cases incorporate the use of residue bits which unlike in Hsiao code eliminates the possibility of a bit being corrected erroneously. Hsiao decoder as mentioned previously can handle this by incorporating all the bits in a PCM column to identify SBE locations, at the expense of higher gate usage.

TABLE IV
GATE LEVEL COMPARISON OF HSIAO DECODER VS. PROSED DECODER

n	k	r	HC	PC	Diff
16	8	2	109	151	+39
32	9	2	207	251	+22
64	10	2	737	450	-39
128	11	2	1643	946	-42
256	12	2	3621	2003	-45

In Table IV, the gate outputs are not shared to eliminate the risk of a multiple error resulting from a single stuck at fault.

In the decoding circuit proposed in [1], the check bits are also corrected. Correcting any bit is simple once it is identified

to be erroneous. The decoder for Hsiao code uses 3-input AND gates to identify the erroneous check bits when only 3-out-of- k code is used. This is not possible if all 3-out-of- m code words are used by the PCM; in other words a $(k - 1)$ -input AND gate is required to identify the check bits as well as information bits if check bit correction is required. Memory systems do not use check bits during computation, thus we have intentionally excluded the identification and correction of check bits in the decoder design.

IV. CONCLUSION

The main feature of the code in Ref.[4] is the reduced number of 1's in the PCM. This results in an efficient encoding and decoding circuits for 64, 128, and 256 information bits. In addition the decoding of a syndrome pattern to identify the presence of a double bit error is considerably simplified. When the last two bits of a syndrome pattern are 11 a double bit error is immediately identified, no further decoding is necessary. When the last two bits are 00, 01 or 10, the decoding circuitry can locate and correct an erroneous bit or indicate the presence of a double/multi-bit error.

REFERENCES

- [1] M. Hsiao, "A class of optimal minimum odd-weight-column sec-ded codes," *IBM J. Res. Dev.*, vol. 14, pp. 395-401, July 1970.
- [2] D. Pradhan, *Fault-Tolerant Computer System Design*. Upper Saddle River, NJ: Prentice Hall, 1996.
- [3] T. Rao and E. Fujiwara, *Error-Control Coding for Computer Systems*. Upper Saddle River, NJ: Prentice Hall, 1989.
- [4] P.K. Lala, P. Thenappan, and M. Anwar, "Single error correcting and double error detecting coding scheme," *IEE Electronics Letters*, vol. 41, pp. 758-760, June 2005.