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A Comparison Study of Electrical Characteristics in Conventional Multiple-gate Silicon Nanowire Transistors

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***Abstract*—**In this paper electrical characteristics of various kinds of multiple-gate silicon nanowire transistors (SNWT) with the channel length equal to 7 nm are compared. A fully ballistic quantum mechanical transport approach based on NEGF was employed to analyses electrical characteristics of rectangular and cylindrical silicon nanowire transistors as well as a Double gate MOS FET. A double gate, triple gate, and gate all around nano wires were studied to investigate the impact of increasing the number of gates on the control of the short channel effect which is important in nanoscale devices. Also in the case of triple gate rectangular SNWT inserting extra gates on the bottom of device can improve the application of device. The results indicate that by using gate all around structures short channel effects such as DIBL, subthreshold swing and delay reduces.

***Keywords*—**SNWT (silicon nanowire transistor), non equilibrium Green's function (NEGF), double gate (DG), triple gate (TG), multiple gate, cylindrical nano wire (CW), rectangular nano wire (RW), Poisson_ Schrödinger solver, drain induced barrier lowering (DIBL).

I. Introduction

DOUBLE gate MOSFETs are considered as promising candidates to overcome short channel effects (SCE) usually encountered in nanometer-scale MOSFET. When the Si body

is thin, gate control is good but when the channel length decreases, the silicon body looks thicker compared with the channel length [1], thus the gate in DG MOSFET will lose its control specially when the channel length is under 10nm[2]. The SNWT provides better scaling capability than MOSFET.

In this paper we investigate various kinds of a rectangular SNWT and a cylindrical SNWT which vary in the number and shape of the gates. A double gate, triple gate, and gate all around nano wires were investigated using NANO TCAD ViDES [3] and *ATLAS* as the Device simulator [4]. This simulation uses quantum mechanical transport approach based on non equilibrium Green's function in effective mass approximation with the use of uncoupled mode space approach (UMS) [6]. In this approach the coupling between the modes is negligible and all the modes are uncoupled as a result of uniform shape of the Si body. Thus the device Hamiltonian becomes a block-diagonal matrix. This approach greatly reduces the computation time. This method is widely explained in [1],[5]. The solution is based on the self consistent solution of Poisson, Schrödinger in 3D. The electron concentration is computed by solving a two dimensional Schrödinger equation for each cross section along z direction, within the effective mass approximation [6],[9]. We assume that confinement is in the transversal plane x-y. Then 3D density of state is computed by NEGF method, and this density is fed back to Poisson equation to get the new electrostatic potential. Then current is computed as shown bellow [7]:

$$I = \frac{2q}{h}\int dE T(E)[f\ (E - E_{F_S}) - f\ (E - E_{F_D})] \tag{1}$$

$$\mathrm{T} = -Tr[(\sum_S - \sum_S^+)G(\sum_D - \sum_D^+)G^+] \tag{2}$$

Where q is the electron charge, h is plank's constant, T(E) is transmission coefficient, G is Green's function and Σ_S and Σ_D are self energies for the source and the drain[10],[11]. The rest of the paper is organized as follows. In section 2, we describe the devices and its structural parameters.

In section 3, we investigate the short channel effects, switching speed and delay of various kinds of SNWTs. This section is followed by the conclusion.

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II. Device Structure

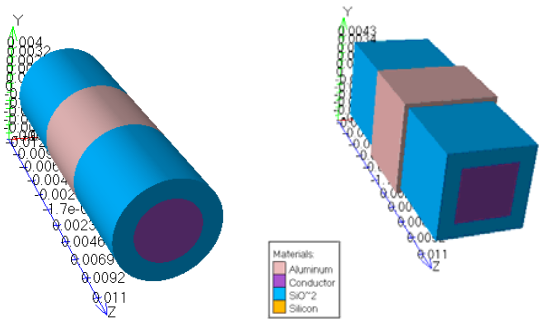

Fig. 1 Three dimensional simulation of the
Gate all around Cylindrical and Rectangular SNWT

Rectangular and cylindrical silicon nanowire transistors investigated in this study, are shown in fig.1. In this structures the channel length is 7nm (along z-direction) and channel is undoped, the gate length is equal to channel length, the SiO_2 gate oxide thickness (T_{ox}) is 1.5nm, the metallic gate is aluminum, the source and drain regions are doped with $N_D=10^{20}cm^{-3}$, the silicon body thickness (T_{si}) is 5nm and in all structures silicon body width (W_{si}) is equal to T_{si}. $m_y^*=o.19m_e$ and $m_z^*=o.98m_e$. For rectangular SNWTs we will compare different kind of DG, TG and GAA structures. In DG SNWT encounter two gates on the top and bottom of channel while TG SNWT encounters three gates around the channel. With this structure short channel effects can be reduces compare with the DG. These structures are shown in fig.2 to investigate of short channel effects. To improve the gate control another gate can be added on the bottom of channel in the case of triple gate SNWT. The capability of this structure is near to cylindrical SNWT under similar conditions. Cylindrical SNWT with gate all around (GAA) structure is the best choice to exhibit good control of short channel effects. To evaluate the performance of these structures we investigate the I_{on}/I_{OFF} ratio, DIBL, sub threshold swing and delay for all structures. We also compare these structures with a DG MOSFET to investigate the high performance of SNWTs.

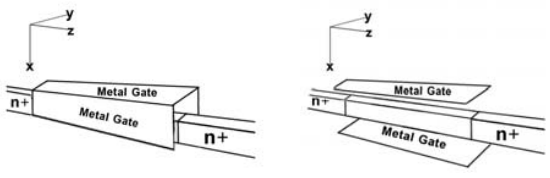

Fig. 2: Three dimensional simulation of the
Double gate (DG) and triple gate (TG) Rectangular SNWT

III. Results and Discussions

In fig. 3 I_{ON}/I_{OFF} ratio is plotted for different structures in two channel lengths. I_{on} is the computed current for $V_{DS}=0.5$ and $V_{GS}=0.5V$, and I_{OFF} is the computed current for $V_{DS}=0.5$ and $V_{GS}=0V$. By increasing the number of gates and make GAA structures gate control will increase and I_{OFF} reduces as a result of short channel effects reduction. It is clear that when the channel length increases I_{off} decreases and the I_{ON}/I_{OFF} ratio increases.

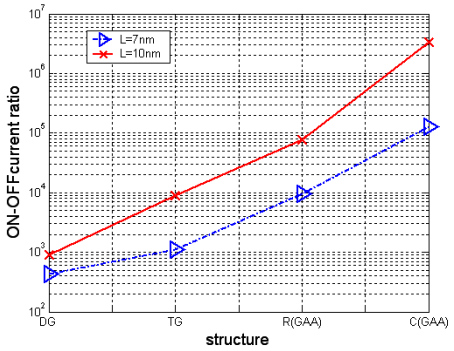

Fig. 3 I_{ON}/I_{OFF} ratio for different channel length of various SN'

Fig. 4 represents the source to drain current as a function of gate voltages when V_{DS} is equal to 0.5V, for rectangular and cylindrical SNWT, when the channel length is 7nm compared with a DG MOSFET in similar conditions. It shows that the cylindrical one has the most gate control because of its symmetry and high quantum confinement [1,6]. I_{ON} in DG MOSFET is more than others but SNWTs because of high gate control have low I_{OFF}. Thus the I_{ON}/I_{OFF} ratio increases in SNWTs. In fig.5 DIBL is plotted as a function of channel length. As the channel length is decreased the drain voltage influences the potential barrier at the source side and thus V_{th} will decrease and DIBL will increase. By comparison between different structures it can be inferred that DIBL is decreased when the number of gates increases because of improving the gate control by surrounding gates.

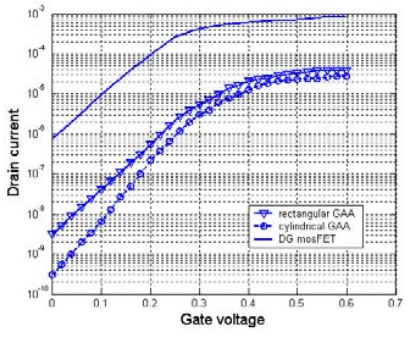

Fig. 4 Source to drain current as a function of gate voltage for CW,RW transistors and DG MOSFET

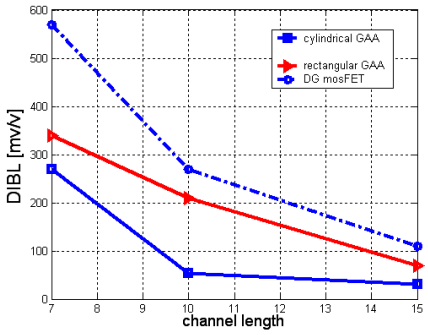

Fig. 5 DIBL as a function of channel length for various kind of rectangular and cylindrical SNWTs and DG MOSFET

In fig. 6 sub threshold swing is plotted as a function of channel length. Decreasing the channel length causes sub threshold swing to increase on the other hand, increasing the number of gates reduces the sub threshold swing, as shown in figure 6 for L_{ch}=7nm a cylindrical gate all around SNWT is the best choice. It provides ideal sub threshold swing and DIBL in the nano scale devices.

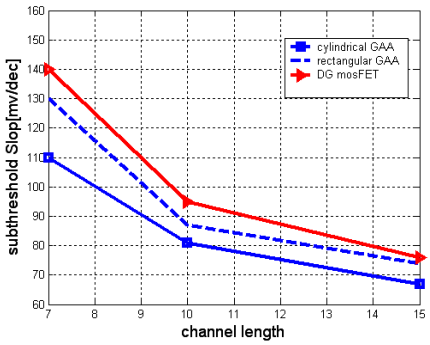

Fig. 6 Subthreshold swing as a function of channel length for rectangular and cylindrical SNWTs and DG MOSFET

Delay

The switching speed of each device which is related to two parameters: ON state current and intrinsic transistor delay. To investigate the switching speed of above mentioned structures, it is necessary to calculate the Delay for all devices. Delay is expressed as [1]:

$$\tau = \frac{C_G (V_{DD} - V_T)}{I_{ON}} \quad (3)$$

Where C_G is given by [8]

$$C_G = \frac{2\pi\kappa\varepsilon_0 L}{\ln(2h/r)} \quad (4)$$

Where V_T is threshold voltage, C_G is the gate capacitance, L is the device length, h is dielectric thickness and 2r is the silicon body thickness. The cross sections of cylindrical and rectangular nano wires are different thus it is necessary to introduce wire spacing parameter, ρ. This parameter is the distance between the centres of wires [6]. For a rectangular SNWT ρ is equal to $2W_{si}$ and for cylindrical one it is equal to minimum wire spacing (W_{wire}).Then we should divide the I_{ON} or I_{OFF} by the wire spacing to get the delay.

TABLE I
SWITCHING SPEED PARAMETERS FOR DIFFERENT KIND OF NANOWIRES

	I_{ON}(μA/μm)	ρ(nm)	τ (ps)
Double gate (SNWT)	1050	10	0.051
Triple gate (SNWT)	1050	10	0.069
Gate all around (RW)	3940	10	0.043
Gate all around (CW)	3510	8.0	0.041

In table 1 delay and on current is shown for various kind of SNWTs, the data in table indicate that increasing the number of gates I_{ON} increases while by increasing the gates delay will increase in TG compare with DG. Minimum delay is related to the cylindrical gate because of high I_{ON} and v_t.

IV. Conclusion

We have analyzed several structures for SNWT. A quantum transport model based on NEGF, was implemented different cross section of a cylindrical and rectangular nano wire. The cylindrical wire transistor has higher threshold voltage, as compared to rectangular wires, because of its cross sections. The cross section of CW is smaller than RW due to strong quantum confinement [6]. Short channel effects in CW were controlled well compare with RW. But the fabrication of CW is difficult because of its symmetry. GAA rectangular SNWT help us to keep our result close to CW compare with triple and double gate RW. Although DIBL and sub-threshold swing in this kind of multiple gate is more than CW it doesn't have fabrication problem. Indeed we investigate short channel effects. By increasing the number of gates to a surrounding gate DIBL and sub threshold swing is decreased because of increasing the gate control. When the channel length is decreases, short channel effects will be more important but we can control these effects by increasing the number of gates. The I_{ON}/ I_{OFF} ratio and delay is improved by GAA structures then the switching speed is increased more. Cylindrical SNWT with gate all around (GAA) structure is the best choice to exhibit good control of short channel effects and high switching speed.

REFERENCES

[1] J. Wang, E. Polizzi and M. Lundstrom, "A computational study of ballistic silicon nanowire transistors," *IEEE International Electron Dev. Meeting (IEDM), Tech.Digest*, pp. 695-698, Dec. 8-10 2003.

[2] J.Saint-Martin, A.Bournel, Philippe, "Comparison of multiple-gate MOSFET architectures using Monte Carlo simulation,"Dollfus Institut d'Electronique Fondamentale, UMR CNRS 8622, Université Paris Sud, Bât. 220,F-91405 Orsay cedex, France.

[3] NANOTCAD ViDES User's Manual by G. Fiori and G. Iannaccone Copyright c 2004-2008, Gianluca Fiori, Giuseppe Iannaccone, University of Pisa. www.NANOTCADVIDES.

[4] Silvaco International, Atlas User's Manual, 2008.

[5] J.Wang, E. Polizzi, and M. Lundstrom *IEDM Tech. Dig.*, 2003, pp. 29.5.1-29.5.4

[6] J.Wang, E. Polizzi, M. Lundstrom, A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation,J. Appl. Phys. 96 (2004) 2192–2203.

[7] G. Fiori, and G. Iannaccone" Three-Dimensional Simulation of One-Dimensional Transport in Silicon Nanowire Transistors" IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 6, NO. 5, SEPTEMBER 2007.

[8] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, Appl. Phys. Lett. **73**, 2447 ~1998.

[9] A. Rahman, M. Lundstrom and A. W. Ghosh, "Generalized effective-mass approach for n-type metal-oxide-semiconductor field-effect transistors on arbitrary oriented wafers," *J. Appl. Phys.*, vol. 97, pp. 053702.1-053702.12, Mar. 2005.

[10] R. Venugopal et al., "Simulating quantum transport in Nanoscale transistors: Real versus mode-space approaches," J. App. Phys.,92, 3730 (2002).

[11] S. H. Zaidi, A. K. Sharma, R. Marquardt, S. L. Lucero and P. M. Varangis, "Multiple nanowire field-effect transistors," *Proc of the 2001 1st IEEE Conference on Nanotechnology*, pp. 189-194, Oct. 2001.