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A Control Strategy Based on UTT and ISCT for 3P4W UPQC

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***Abstract*—**This paper presents a novel control strategy of a three-phase four-wire Unified Power Quality (UPQC) for an improvement in power quality. The UPQC is realized by integration of series and shunt active power filters (APFs) sharing a common dc bus capacitor. The shunt APF is realized using a thee-phase, four leg voltage source inverter (VSI) and the series APF is realized using a three-phase, three leg VSI. A control technique based on unit vector template technique (UTT) is used to get the reference signals for series APF, while instantaneous sequence component theory (ISCT) is used for the control of Shunt APF. The performance of the implemented control algorithm is evaluated in terms of power-factor correction, load balancing, neutral source current mitigation and mitigation of voltage and current harmonics, voltage sag and swell in a three-phase four-wire distribution system for different combination of linear and non-linear loads. In this proposed control scheme of UPQC, the current/voltage control is applied over the fundamental supply currents/voltages instead of fast changing APFs currents/voltages, there by reducing the computational delay and the required sensors. MATLAB/Simulink based simulations are obtained, which support the functionality of the UPQC. MATLAB/Simulink based simulations are obtained, which support the functionality of the UPQC.

***Keywords*—**Power Quality, UPQC, Harmonics, Load Balancing, Power Factor Correction, voltage harmonic mitigation, current harmonic mitigation, voltage sag, swell

I. Introduction

BECAUSE of the application of sophisticated and more advanced software and hardware for the control systems the power quality has become one of the most important issues for power electronics engineers. With great advanc ment in all areas of engineering, particularly, in signal processing, control systems, and power electronics, the load characteristics have changed completely. These nonlinear loads draw non-linear current and degrade electric power quality. The quality degradation leads to low power-factor, low efficiency, overheating of transformers and so on [1]. Moreover, in case of the distribution system, the overall load on the system is seldom found balanced, which cause excessive neutral currents in a three-phase four-wire distribution system. Ideally, voltage and current waveforms are in phase, power factor of load equals unity, and the reactive power consumption is zero; this situation enables the most efficient transport of active power, leading of the cheapest distribution system. Relating to power quality issues, the designers of power quality conditioner systems are required to follow the recommendations of some world-wide accepted standards like IEEE-519-1992, IEC 1000-3-2, IEC 1000-3-4 recommended practice and requirements for harmonic control in electric power systems.

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In the past, the solutions to mitigate these identified power quality problems were through using conventional passive filters. But their limitations such as ,fixed compensation, resonance with the source impedance and the difficulty in tuning time dependence of filter parameters have ignited the need of active and hybrid filters[2]-[4]. Under this circumstance, a new technology called custom power emerged [5], [6], which is applicable to distribution systems for enhancing the reliability and quality of the power supply.

The Unified Power Quality Conditioner (UPQC) is one of the best solutions to compensate both current and voltage related problems, simultaneously [7-9]. As the UPQC is a combination of series and shunt active filters, two active filters have different functions. The series active filter suppresses and isolates voltage-based distortions. The shunt active filter cancels current-based distortions. At the same time, it compensates reactive current of the load and improves power factor. There are many control strategies reported in the literature to determine the reference values of the voltage and the current of three-phase four-wire UPQC, the most common are the p-q-r theory[10],modified single-phase p-q theory[11], synchronous reference frame(SRF) theory[12], symmetrical component transformation [13],and unit vector template (UVT) technique [14] etc. Apart from this one cycle control (OCC) [15] (without reference calculation) is also used for the control of3-phase, 4-wire UPQC.

This paper presents a 3-phase, 4-wire UPQC for an improvement of different power quality problems. A control technique based on UTT is used to get the reference signals for series APF, while ISCT is used for the control of Shunt APF. The proposed control technique is capable of extracting most of the load current and source voltage distortions successfully. The series AF is controlled to eliminate supply voltage harmonics and voltage regulation against voltage sag and swell while, the shunt APF is controlled to alleviate the supply current from harmonics, negative sequence current, reactive power and load balancing. The performance of the proposed system is demonstrated through simulated waveforms using SPS Matlab/Simulink enviournment.

The UPQC configuration and the load under consideration load are discussed in Section II. The control algorithm for UPQC is discussed in Section III. The SIM POWER SYSTEM (SPS), Matlab/ Simulink based simulation results are discussed in Section IV and finally Section V concludes the paper.

II. System Description

The system under consideration for three-phase four-wire distribution system is shown in Fig.1.The UPQC is connected before the load to make the source and the load voltage free

from any distortions and at the same time, the reactive current drawn from source should be compensated in such a way that the currents at source side i_s, would be in phase with utility voltages. Provisions are made to realize voltage harmonics, voltage sag and swell in the source voltage by switching on/off the three-phase rectifier load, R-L load and R-C load respectively. The UPQC, realized by using two voltage source inverters is shown in Fig.2. One acting as a shunt APF (Active Power Filter), while the other as series APF. The shunt APF is realized using a thee-phase, four leg voltage source inverter (VSI) and the series APF is realized using a three-phase, three leg VSI. Both the APFs share a common dc link in between them. The four-leg VSI based shunt active filter is capable of suppressing the harmonics in the source currents, negative sequence of source current, load balancing and power-factor correction. The implemented control algorithm consists mainly of the computation of three-phase reference voltages of load voltages ($v^*_{la,}$ v^*_{lb} and v^*_{lc}), and the reference currents for the source current ($i^*_{sa,}$ i^*_{sb} and i^*_{sc}).

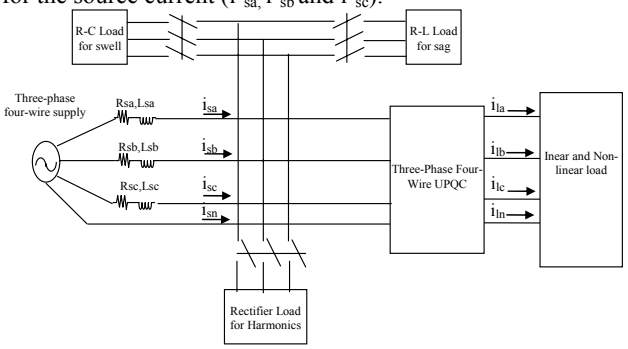

Fig. 1 System under consideration

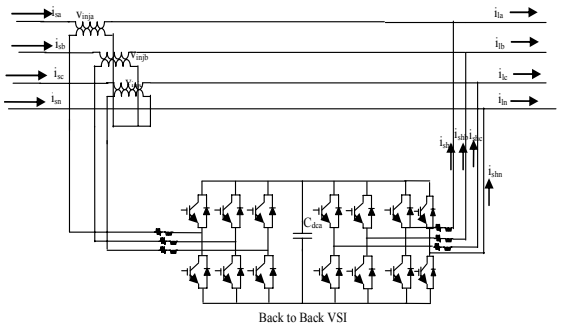

Fig. 2 UPQC Block Diagram

The voltage at the source side before UPQC, the load voltage at load, the voltage injected by series APF and the dc link voltage between two inverters are represented by v_s, v_L, v_{inj} and V_{dc} respectively. Whereas, the current on the source side, total current drawn by all the loads and the current injected by shunt APF are represented by i_s, i_l, and i_{sh} respectively. The load under consideration is a combination of linear and non-linear loads. Single-phase lagging power-factor load is taken as a linear load, where as a three-phase diode bridge rectifier with a resistive load on dc side is considered as a non-linear load. The values of the circuit parameters and load under consideration are given in Appendix.

III. Control Strategy of Series APF

The series is controlled in such a way that it injects voltages ($v_{fa,}$ v_{fb} and v_{fc}), which cancel outs the distortions present in the supply voltages ($v_{sa,}$ v_{sb} and v_{sc}), thus making the voltages at PCC ($v_{la,}$ v_{lb} and v_{lc}) perfectly sinusoidal with the desired amplitude. In other words, the sum of supply voltage and the injected series filter voltage makes the desired voltage at the load terminals. The control strategy for the series APF is shown in Fig.3. Since, the supply voltage is distorted, a phase locked loop (PLL) is used to achieve synchronization with the supply voltage [14].Three-phase distorted supply voltages are sensed and given to PLL which generates two quadrature unit vectors (sin*wt*,coswt).The in-phase sine and cosine outputs from the PLL are used to compute the supply in phase,120^o displaced three unit vectors (u_a ,u_b u_c) using eqn.(1) as:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \quad (1)$$

The computed three in-phase unit vectors then multiplied with the desired peak value of the PCC phase voltage (V^*_{lm}), which becomes the three-phase reference PCC voltages as:

$$\begin{bmatrix} v^*_{la} \\ v^*_{lb} \\ v^*_{lc} \end{bmatrix} = V^*_{lm} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (2)$$

The desired peak value of the PCC voltage under consideration is 338V (=415sqrt (2)/sqrt(3)).The computed voltages from reference voltages from eqn.(2) are then given to the hysteresis controller along with the sensed three phase PCC voltages($v_{la,}$ v_{lb} and v_{lc}).The output of the hysteresis controller is switching signals to the six switches of the VSI of series APF. The hysteresis controller generates the switching signals such that the voltage at PCC becomes the desired sinusoidal reference voltage. Therefore, the injected voltage across the series transformer through the ripple filter cancels out the harmonics, voltage sag or swell present in the supply voltage.

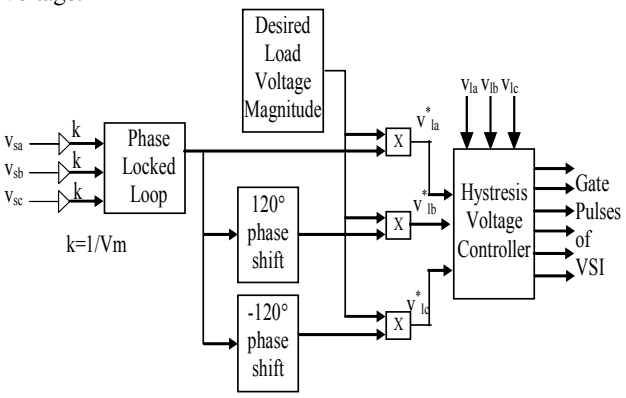

Fig. 3 Control Scheme of Series APF using UTT

IV. Control Strategy of Shunt APF

The control algorithms for shunt APF consists of the generation of 3-phase reference supply currents (i^*_{sa}, i^*_{sb} and i^*_{sc}).The control algorithm based on ICST for shunt APF is shown in Fig.4. The symmetrical component transformation matrix can be applied to instantaneous voltages and currents. We can then define the instantaneous symmetrical component of voltages as:

$$\begin{bmatrix} v_{a0} \\ v_{a1} \\ v_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \quad (3)$$

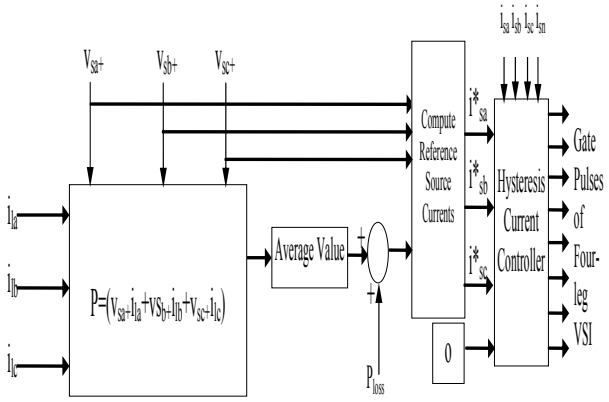

Fig. 4 Control Scheme of Shunt APF using ISCT

Similarly, we can define the instantaneous symmetrical component of currents. The primary objective of the control algorithm shown in Fig.7 is to obtained balanced source currents. Therefore reference source currents can be considered as:

$$i^*_{sa} + i^*_{sb} + i^*_{sc} = 0 \quad (4)$$

From the power factor consideration, the phase angle between v_{a1} and i_{sa1} is Φ then:

$$\angle\{v_a + a v_b + a^2 v_c\} = \angle\{i^*_{sa} + a i^*_{sb} + a^2 i^*_{sc}\} + \phi$$

$$\tan^{-1}\left\{\frac{K_1}{K_2}\right\} = \tan^{-1}\left\{\frac{K_3}{K_4}\right\} + \phi$$

where

$$K_1 = \frac{\sqrt{3}}{2}(v_b - v_c),\ K_2 = \left(v_a - \frac{1}{2}v_b - \frac{1}{2}v_c\right),$$

$$K_3 = \frac{\sqrt{3}}{2}(i^*_{sb} - i^*_{sc}),\ K_4 = \left(i^*_{sa} - \frac{i^*_{sb}}{2} - \frac{i^*_{sc}}{2}\right)$$

Solving the above equations we get

$$(v_b - v_c - 3\beta v_c) i^*_{sa} + (v_c - v_a - 3\beta v_b) i^*_{sb} + (v_a - v_b - 3\beta v_c) i^*_{sc} = 0 \quad (5)$$

where $\beta = \frac{\tan\phi}{\sqrt{3}}$.

For power-factor correction β=0, the source currents are to be in phase with the source voltages. It implies that the reactive power demand of the load is supplied by the shunt APF of the UPQC. The prime objective of the control algorithm is to supply the load active power and the losses of the UPQC in power-factor correction mode:

$$v_a i^*_{sa} + v_b i^*_{sb} + v_c i^*_{sc} = p_{lavg} + p_{loss} \quad (6)$$

where, p_{lavg} filtered average load active power using moving average filter calculated from load power

$$p_l = v_{sa+} i_{la} + v_{sb+} i_{lb} + v_{sc+} i_{lc}$$

where, v_{sa+}, v_{sb+} and v_{sc+} are the positive sequence of the three-phase source voltages calculated as per equation(3).

The active load power is calculated by moving average filter with averaging time of half cycle of the source frequency. The amplitude of the P_{loss} is the output of DC bus voltage PI controller for self supporting bus of the UPQC which can be expressed as;

$$I^*_{d(n)} = I^*_{d(n-1)} + K_{pd}\{V_{de(n)} - V_{de(n-1)}\} + K_{id} V_{de(n)} \quad (7)$$

where $V_{de(n)} = V_{dcr} - V_{dca(n)}$ denotes the error in V_{dc} calculated over reference value of V_{dc}. and average value of V_{dc}.K_{pd} and K_{id} are proportional and integral gains of the dc bus voltage PI controller.

After solving eqn.4, 5and 6 the reference source currents can be obtained as:

$$i^*_{sa} = \{v_a - (v_b - v_c)\beta\}(p_{lavg} + p_{loss})/A$$

$$i^*_{sb} = \{v_b - (v_c - v_a)\beta\}(p_{lavg} + p_{loss})/A$$

$$i^*_{sc} = \{v_c - (v_a - v_b)\beta\}(p_{lavg} + p_{loss})/A$$

where $A = \sum i = a, b, c V_i^2$

In this proposed control algorithm, the sensed(i_{sa}, i_{sb} and i_{sc}) and reference source currents(i^*_{sa}, i^*_{sb} and i^*_{sc}) are compared in a hysteresis current controller to generate the switching signals to the switches of the shunt APF which makes the supply currents sinusoidal, balanced in in- phase with the voltage at PCC. Hence the supply current contains no harmonics or reactive power component. The source neutral current is compensated to fallow a reference signal of zero magnitude by switching the fourth leg of the VSI, through the hysterisis controller. By doing this, the supply neutral current can be eliminated. In this control scheme, the current control is applied over the fundamental supply currents instead of the fast changing APF currents, thereby reducing the computational delay and number of required sensor. In addition to this, the load or the filter neutral current are not sensed, thereby reducing the computational delay.

V. Results And Discussion

The proposed control scheme has been simulated using MATLAB/ Simulink and its Sim-Power System toolbox. The performance of UPQC is evaluated in terms of voltage and current harmonics mitigation, load balancing, power-factor correction and mitigation of voltage sag and swell under different load conditions.

A. Performance of UPQC for load balancing and power-factor correction

Fig. 5 shows the response of UPQC with linear lagging power-factor load for power-factor correction and load balancing. The shunt APF is put into operation at 0.1 sec.

Fig.5 (e) shows that after 0.1 sec the source voltage and source current in phase 'a' are exactly in phase. At t=0.2 sec the load is changed from three phase to two phase to make the load unbalanced and restored to three-phase balanced load at t=0.3 sec. During this period, a current 19.23A RMS (i_{ln}) flows in the neutral conductor as shown in Fig.5 (g). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.5 (f). It is also observed from Fig.5 (h) that during unbalanced load operation, the dc voltage is maintained to its reference value.

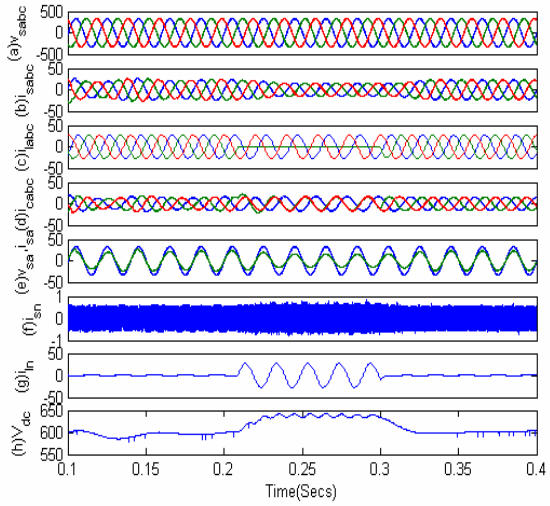

Fig. 5 Performance of UPQC for load balancing and power factor correction

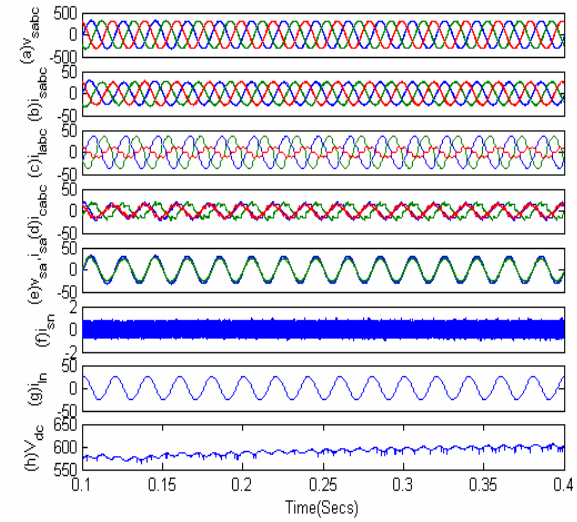

Fig. 6 Performance of UPQC for load balancing, power factor correction and current harmonic mitigation

B. Performance of UPQC for load balancing, power-factor correction and current harmonic mitigation

Fig.6. shows the response of UPQC for power-factor correction, load balancing and current harmonic mitigation. In order to demonstrate the response of UPQC for load balancing, power factor correction and current harmonic mitigation, the load under consideration is a combination of a three-phase diode bridge rectifier with resistive load and two single phase lagging power factor load in phase 'a' and 'b' only. Because of this unbalanced load, a current 17.50A RMS (i_{ln}) flows in the neutral conductor as shown in Fig.6 (g). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.6 (f). It is observed that the supply currents are balanced, sinusoidal and in-phase with the voltages as is shown in Fig.6 (b).

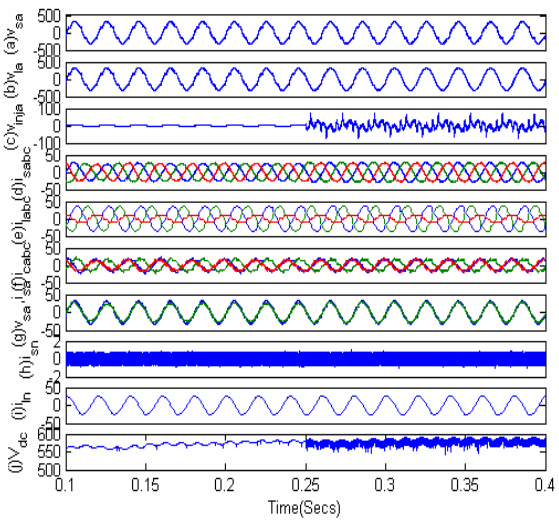

Fig. 7 Performance of UPQC for load balancing, power factor correction, current and voltage harmonic mitigation

C. Performance of UPQC for load balancing, power-factor correction, current and voltage harmonic mitigation

Fig.7 shows the response of UPQC for load balancing, power factor correction, voltage harmonic mitigation and current harmonic mitigation. In order to verify the effectiveness of control algorithm for voltage harmonic mitigation, a three-phase diode bridge rectifier with resistive load on dc side is switched on at 0.05 sec. Because of this the voltage across the load becomes distorted. To visualize the shunt APF and series APF performance individually, both APF's are put into operation at different instant of time. At time t_1=0.1 sec, shunt APF is put into operation first. It is observed from Fig.7 (d) that the supply currents are balanced; sinusoidal and in-phase with the voltages even under non-sinusoidal utility voltage. The source current THD in phase 'c' is improved form 15.10 % to 4.36 %. At time t_2=0.25 sec the series APF is put into the operation. The series APF starts compensating voltage harmonics immediately by injecting out of phase harmonic voltage, making the load voltage at load distortion free. The voltage injected by series APF is shown in Fig. 7(c). Here load voltage THD is improved form 5.38 % to 2.47 %. The harmonic spectra of the source current and the load voltage in phase 'c' with compensation and without

compensation are shown in Fig. 8. Because of unbalanced load, a current 18.69A RMS (i_{ln}) flows in the neutral conductor as shown in Fig.7 (i). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.7 (h).

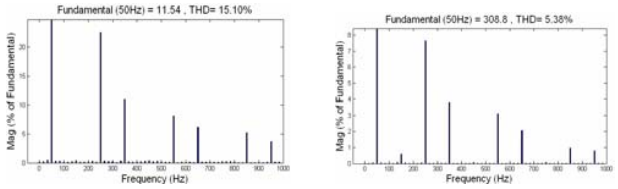

Fig.8 (a) - (b) Source current and Load voltage without compensation

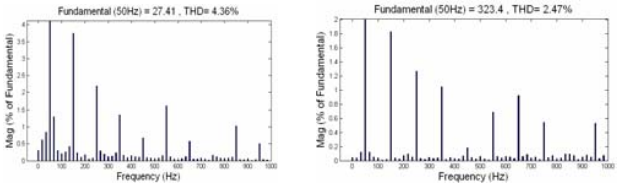

Fig.8(c) - (d) Source current and Load voltage with compensation

D.Performance of UPQC for load balancing, power-factor correction, current and voltage sag mitigation

The simulation results for voltage sag compensation are shown in Fig. 9. There are four instants; t_1, t_2, t_3 and t_4. At time t_1=0.10 s, the shunt APF is put into the operation and its operation is as discussed previously. At time t_2=0.25 s, series APF is put into operation. Now a 10 kW, 40 Kvar (inductive) load is switched on at t=0.35 s and switched off at t=.045 sec. Because of this a sag is developed on the system at time t_3=0.35 s. This sag lasted till time t_4=0.45 s, as shown in Fig. 9 (a). After time t_4=0.45 s, the system is again at normal working condition. During this voltage sag condition, the series APF is providing the required voltage by injecting in phase compensating voltage equals to the difference between the reference load voltage and supply voltage, as shown in Fig. 9 (c). The load voltage profile in Fig. 9 (b) shows that UPQC is maintaining it at desired constant voltage level at load even during the sag on the system such that the loads cannot see any voltage variation. Because of unbalanced load, a current (i_{ln}) flows in the neutral conductor as shown in Fig.9 (i). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.9 (h).

E. Performance of UPQC for load balancing, power-factor correction, current and voltage swell mitigation

At time t_1=0.10 s, the shunt APF is put into the operation and at time t_2=0.20 s, series APF is put into operation. A swell is now introduced on the system by switching on a 10 kW, 40 Kvar (capacitive) from time t_3=0.35 s to t_4=0.45 s, as shown in Fig. 10. Under this condition the series APF injects an out of phase compensating voltage in the line through series transformers, equal to the difference between the reference load voltage and supply voltage, as shown in Fig.10 (c). The load voltage profile in Fig.10 (b) shows the UPQC is effectively maintaining the load bus voltage at desired constant level. Fig.10 (i) shows that a current (i_{ln}) flows in the neutral conductor, which is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.10 (h).

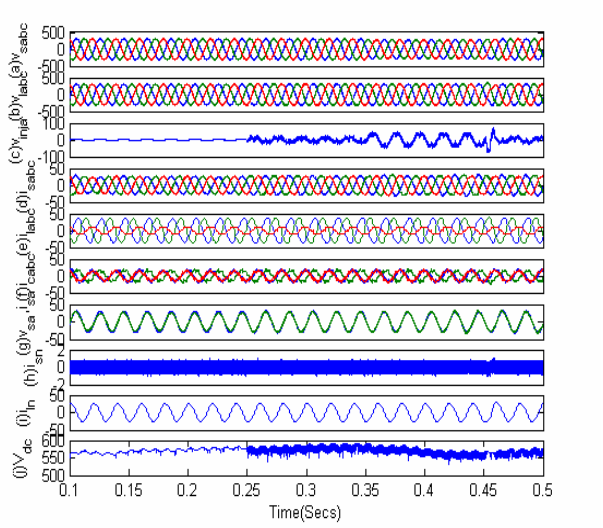

Fig.9 Performance of UPQC for load balancing, power factor correction, current harmonic and voltage sag mitigation

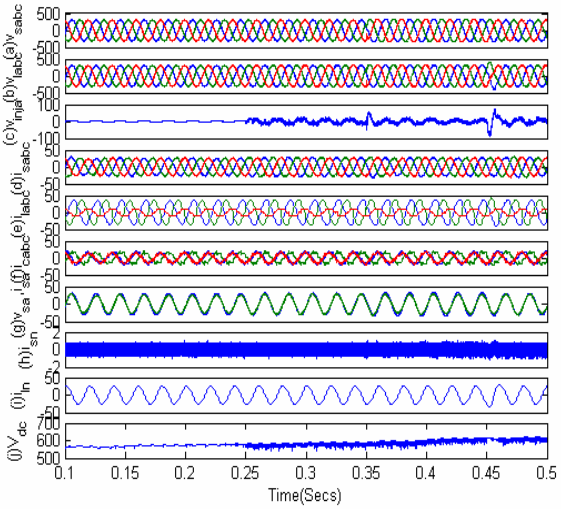

Fig.10 Performance of UPQC for load balancing, power factor correction, current harmonic and voltage swell mitigation

F. Performance of UPQC for sudden load change

In order to show the response of UPQC for sudden load change the load across the dc side of the rectifier is increased at t=0.25 s. It is observed from Fig.11(b) that in addition to the load balancing, power factor correction and current harmonic mitigation, the UPQC controller acts immediately without any delay in the operation and gain the new steady state. It is also

observed from Fig. 11 (f) that there is small dip in dc voltage at t=0.25 s, but dc link is able to regulate the dc voltage to its previous value. Fig.12 (i) shows that a current (i_{ln}) flows in the neutral conductor, which is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Fig.11 (h).

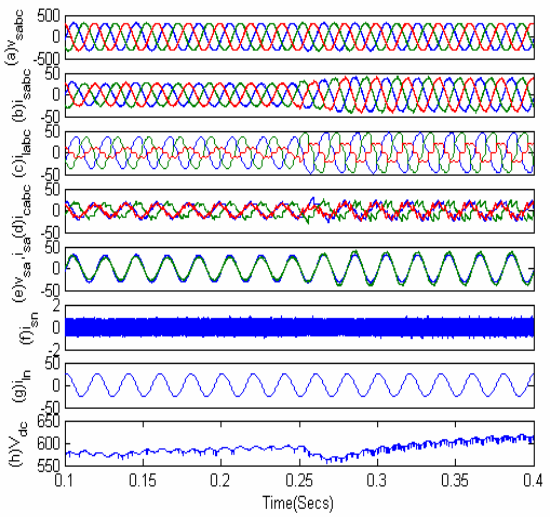

Fig. 11 Performance of UPQC during sudden load change

VI. Conclusion

The proposed control scheme based on UTT and ISCT for the three-phase four-wire UPQC has been validated through simulation results, using MATLAB software along with simulink and sim-power system toolbox. The performance of the UPQC has been observed to be satisfactory for various power quality improvements like load balancing; source neutral current mitigation, power-factor correction, voltage and current harmonic mitigation, mitigation of voltage sag and swell. The source current THD is improved from 15.10 % to 4.36 %, while the load voltage THD is improved form 5.38 % to 2.47 %. In addition to this the performance of UPQC has been found satisfactory during transient conditions.The system parameters used are as follows:

Appendix

Supply voltage and line impedance: 415 V L-L, f=50 Hz, R_s=0.1ohm, L_s=1.5mH
Filter:R=7ohm,C=5µF
DC bus capacitance: C_{dc}=3000µF
Transformer: 250MVA, 58kV/12kV
Loads: Two single-phase linear load of 12KW, 8KVar in phase ‘a’ and ‘b’ only and a Three-Phase Rectifier Load R=50 ohm on dc side.

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