# Variable Input Range Continuous-time Switched Current ΔΣ Analog Digital Converter for RFID CMOS Biosensor Applications

Boram Kim, Shigeyasu Uno, and Kazuo Nakazato

**Abstract**— Continuous-time delta-sigma (ΔΣ) analog digital converter (ADC) for radio frequency identification (RFID) complementary metal oxide semiconductor (CMOS) biosensor has been reported. This  $\Delta\Sigma$  ADC is suitable for digital conversion of biosensor signal because of small process variation, and variable input range. As the input range of continuous-time switched current  $\Delta\Sigma$  ADC (Dynamic range : 50 dB [1], [2]) can be limited by using current reference, amplification of biosensor signal is unnecessary. The input range is switched to wide input range mode or narrow input range mode by command of current reference. When the narrow input range mode, the input range becomes ± 0.8 V. The measured power consumption is 5 mW and chip area is 0.31 mm² using 1.2 μm standard CMOS process. Additionally, automatic input range detecting system is proposed because of RFID biosensor applications.

*Keywords*— continuous time, delta sigma, A/D converter, RFID, biosensor, CMOS.

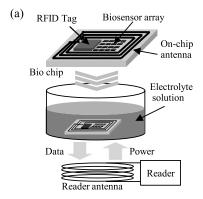
### I. INTRODUCTION

FID technology is a generic term that is used to describe a Rsystem that transmits the information of a tag wirelessly, using electromagnetic wave or inductive coupling. Depending on integrated circuit and antenna technology development, RFID has been used in various applications; smart card, factory automation system, toll gates for motor vehicles and container control system. Recently, other application examples have reported that RFID biosensor chips integrate the RFID and biosensor [3]-[5]. The advantage of RFID biosensor (Fig. 1) over wiring interface biosensor system include the following; inexpensive and low noise, subaqueous measuring system, the I/O buffer circuit is unnecessary, and application of implantable sensor. As the low power consumption and high accuracy, ADC that converts the biosensor analog signal is very important element of inner circuitry. However, existing  $\Delta\Sigma$  ADC has some drawbacks.

In this paper, continuous-time  $\Delta\Sigma$  ADC for RFID CMOS biosensor chip is discussed and optimized. In section 2 we decide the suitable ADC for RFID biosensor. Section 3 explains the principle of variable input range by using current reference. In section 4, the automatic input range detect system is proposed.

Boram Kim is with the Department of Electrical Engineering and Computer Science, Graduate School of Engineering, Nagoya University, 464-8603 Japan, e-mail: (r kimu@nuee.nagoya-u.ac.jp)

S. Uno and K. Nakazato are with the Department of Electrical Engineering and Computer Science, Graduate School of Engineering, Nagoya University, 464-8603 Japan.



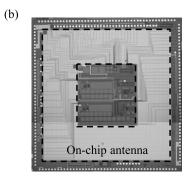


Fig. 1 (a) RFID biosensor measuring system. (b) Micrograph of the chip.

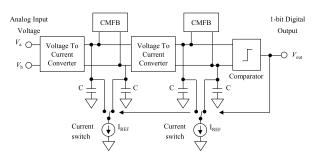


Fig. 2 The architecture of the continuous-time switched-current  $\Delta\Sigma$  modulator.

The operation of this system is explained and confirmed by result of HSPICE simulation. Finally, Section 5 gives some conclusions.

#### II. SUITABLE ADC FOR RFID BIOSENSOR

As for our RFID biosensor circuit, ADC of high accuracy, small size and low power consumption is required because a signal change is small, and chip area and RFID power is limited. The delta-sigma ( $\Delta\Sigma$ ) ADC is suitable because of small size, low power consumption, and high resolution. There are two kinds of  $\Delta\Sigma$  ADC; discrete-time (DT)  $\Delta\Sigma$  ADC and continuous-time (CT)  $\Delta\Sigma$  ADC. DT  $\Delta\Sigma$  ADC has disadvantages because it requires large area for low pass filter (LPF) for anti-aliasing and high power consumption in switched capacitor input circuit. Above all, switch of ADC input range disturbs biosensor circuit output signal, which is a significant problem. Conventional CT  $\Delta\Sigma$  ADC uses resistance and a large capacitor, resulting in the large area. Moreover, it is not accurately controllable due to the process variation. To solve these problems, continuous-time switched current (CTSC)  $\Delta\Sigma$  ADC [1], [2] is used (Fig. 2). LPF is not needed for this type, and there is an advantage that it does not use resistance because it uses the current source for feedback. The input stage of CTSC  $\Delta\Sigma$  ADC has not switched capacitor circuit but differential pair of MOSFETs, so that biosensor output signal is not influenced by sampling clock. Hence, this type is suitable for our RFID system.

### III. VARIABLE INPUT RANGE BY CURRENT REFERENCE

## A. Principle

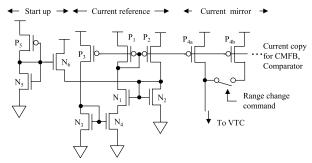


Fig. 3 Current reference with CMOS technology only.

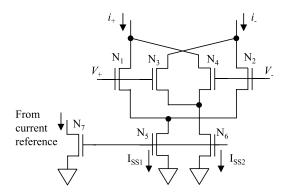


Fig. 4 The circuit diagram of voltage to current converter.

Because of a small signal change of biosensor, sensed signal should be amplified before digital converting [3], [4]. However,

the same function can be achieved by limiting the input range of CTSC  $\Delta\Sigma$  ADC. This is possible since the transconductance of voltage to current converter (VTC) [6] is determined by the tail currents. Figure 3 shows the circuit diagram of current reference [7]. This current reference is built by CMOS FETs only. The generated current can be copied by the current mirror and supplied to common-mode feedback (CMFB) circuit, comparator and VTC. For optimal linearity, the ratio of transistors (N<sub>1</sub> = N<sub>2</sub> : N<sub>3</sub> = N<sub>4</sub>) is set to 5:3, and the ratio of the tail current level  $I_{SS1}$ : $I_{SS2}$  is set to 4:1 [6]. The circuit diagram of VTC is shown in Fig. 4. The difference of two output current is given by

$$i_{+} - i_{-} = 2.58\sqrt{2I_{SS2}K2}(V_{+} - V_{-}),$$
 (1)

where K2 is proportional to W/L ratio of  $N_3$  and  $N_4$ . Equation (1) shows that gain of VTC depends on the tail current  $I_{SS2}$ . Since the tail current of VTC is increased when the range change command is ON, the input range becomes narrower at higher gain of VTC.

# B. Measurement

The measured result of variable input range CTSC  $\Delta\Sigma$  ADC is shown in Fig. 5 and 6. The sampling frequency is set to 330 kHz. When input range is set to wide (Fig. 5), input range is almost 0 - 5 V. Contrastively, the input range become  $V_b \pm 0.8$  V, when input range is set to narrow range mode (Fig. 6). In narrow input range mode, the input range is variable according to  $V_b$ . Figure 7 shows micrograph of the CTSC  $\Delta\Sigma$  ADC fabricated by 1.2  $\mu$ m standard CMOS process. The measured power consumption is 5 mW and chip area is 0.31 mm² (Current reference: 0.09 mm², CTSC  $\Delta\Sigma$  ADC: 0.22 mm²).

TABLE I
TRUTH TABLE OF INPUT RANGE DECIDE COMMAND

Input range	A	В	a	b	c
~ 2.5 V	High	High	High	Low	Low
$2.5~V\sim3.5~V$	Low	High	Low	High	Low
3.5 V ~	Low	Low	Low	Low	High

TABLE II Karnaugh Map of Control Circuit Output a

A B	Low	High
Low	Low	Low
Low High	*	High

TABLE III

KARNAUGH MAP OF CONTROL CIRCUIT OUTPUT b				
A	Low	High		
Low	Low	High		
High	*	Low		
$b = \overline{A} \bullet B$				

TABLE IV

KARNALIGH MAP OF CONTROL CIRCUIT OUTPUT O

TERRITION OF CONTROL CIRCON CONTENT				
A B	Low	High		
Low	High	Low		
High	*	Low		

 $c = \overline{B}$ 

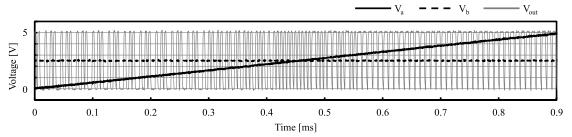


Fig. 5. The measured result of CTSC  $\Delta\Sigma$  ADC. (Wide range mode)

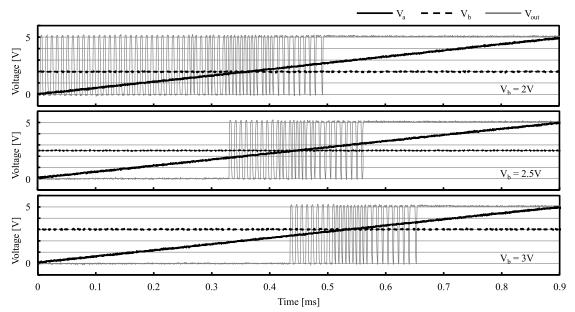


Fig. 6. The measured result of CTSC  $\Delta\Sigma$  ADC. (Narrow range mode) The input range becomes  $V_b \pm 0.8 \text{ V}$ .

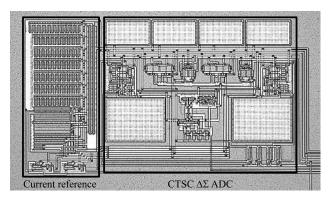


Fig. 7 Micrograph of CTSC  $\Delta\Sigma$  ADC.

# IV. AUTOMATIC INPUT RANGE DETECTING SYSTEM

# A. Principle

Figure 8 shows the block diagram of automatic input range detection system. The input range is switched to wide input range mode or narrow input range mode by range change

command. When the wide input range mode is ON, center voltage of input range is set to 2.5 V and input range becomes almost 0 - 5V. Contrastively, when narrow input range mode is ON, input range is divided into 3 ranges (2.5V or less, 2.5 V to 3.5 V and 3.5 V or more). The range of input signal is detected by two comparators and center voltage of input range is decided by control circuit command a, b, and c. The truth table of command A, B, a, b, and c is shown in Table 1. The logic expression of control circuit output a, b, and c is simplified as Table 2, Table 3, and Table 4, respectively. As a result, control circuit can be composed as Fig. 9. Only 1 NAND and 1 inverter are needed. The input signal range can automatically detected by this system.

# B. HSPICE simulation

The HSPICE simulation result of automatic input range detecting system is shown in Fig. 10. When narrow input range mode set to ON,  $V_b$  is changed by input signal  $V_a$ , automatically. The sampling frequency is set to 1 MHz. The simulated power consumption of entire system is 15 mW and estimated chip area is 0.45 mm<sup>2</sup> using 1.2  $\mu$ m standard CMOS process. The circuitry operation is confirmed by HSPICE simulation result.

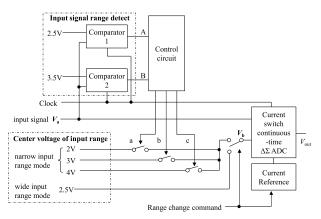


Fig. 8 Block diagram of automatic input range detecting system.

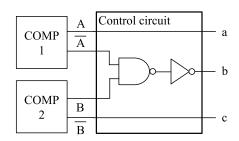


Fig. 9 Control circuit.

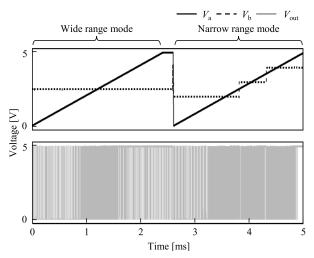


Fig. 10 The HSPICE simulation result of automatic input range detecting system.

## V.CONCLUSIONS

The present work focuses on variable input range CTSC  $\Delta\Sigma$  ADC. The input range is changed by the change of VTC gain, and the accuracy of ADC increases by narrowing the input range. The input range can be detected by proposed detecting system. Moreover, all operation can be controlled by only inside of the chip automatically and it is very advantageous to wireless system. Hence, this system is optimum for our RFID biosensor system.

## ACKNOWLEDGMENT

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## REFERENCE

- [1] L. Luh, J. Choma, and J. Draper, "A 50 MHz continuous-time switched-current ΣΔ modulator," *IEEE Int. Symp. Circuits and Systems.*, 1998, vol. 1, pp. 579 - 582.
- [2] L. Luh, J. Choma, and J. Draper, "A continuous-time common-mode feedback circuit (CMFB) for high-impedance current-mode applications," *IEEE Trans. Circuits and Systems* 2, vol. 47, pp 363 -369, 2000.
- [3] Y. Yazawa, T. Oonishi, K. Watanabe, R. Nemoto, M. Kamahori, T. Hasebe, and Y. Akamatsu, "A wireless biosensing chip for DNA detection," *ISSCC Dig. Tech.* Pap., 2005, p. 562.
- [4] Y. Yazawa, T. Oonishi, R. Watanabe, R. Nemoto, and A. Shiraishi, "Radio frequency identification sensor chips with anticollision algorithm for simultaneous detection for multiple DNA targets," *J. App. Phys.*, 2010, vol. 49, pp. 04DL13, 2010.
- [5] K. Murari, C. Sauer, M. Sanacvic, G. Cauwenberghs, and N. Thakor, "Wireless multichannel integrated potentiostat for distributed neurotransmitter sensing," in *Proc. 27th Ann. Int. Conf. IEEE EMBS*, 2005, pp. 7329 - 7332.
- [6] C. Ioumazou, F. J. Lidgey, and D. G. Haigh, "Analog IC design, the current-mode approach," IEEE press, 1993.
- [7] H. J. Oguey, and D. Aebischer, "CMOS current reference without resistance," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 1, pp. 1132 - 1135, 1997.

**Boram Kim** was born in Daejeon, Korea, on March 1, 1984. He received the B.S. degree in Electronic, Electrical and Information Engineering from Nagoya University, Aichi, Japan, in 2008 and the M.S. degrees in the Department of Electrical Engineering and Computer Science, Graduate School of Engineering, Nagoya University, Aichi, Japan in 2010, where he is currently working toward the Ph.D. degree. His present research interests include the design of on-chip antenna and continuous-time  $\Delta\Sigma$  A/D converter for RFID biosensor applications.

Shigeyasu Uno was born in Kyoto, Japan, in 1973. He received the B.S. degree in physics from Kwansei Gakuin University, Hyogo, Japan, and M.S. degree in solid-state physics and Ph.D. degree in electrical engineering from Osaka University, Osaka, Japan, in 1996, 1998, and 2002, respectively. After postdoctoral research at Osaka University, Osaka, Japan, he joined Hitachi Cambridge Laboratory of Hitachi Europe Ltd., Cambridge, UK. in 2002. In 2005, he was assigned as a visiting research professor at School of Mathematical Sciences, Claremont Graduate University, California, USA. Since 2006, he has been an assistant professor of electrical engineering at Nagoya University, Aichi, Japan. His research activity includes modeling of nano-scale semiconductor devices, simulation of biosensors, and CMOS biosensor design and development.

**Kazuo Nakazato** was born in Japan on 18 October, 1952. He received the B.S., M.S. and Ph.D. degrees in physics from the University of Tokyo in 1975, 1977, and 1980, respectively. In 1981 he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, working on high-speed silicon self-aligned bipolar devices

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SICOS (sidewall base contact structure), which were adopted in main frame computer Hitachi M-880/420. In 1989 he moved to Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Cambridge, England, as senior researcher and laboratory manager, working on experimental and theoretical study of quantum electron transport in semiconductor nano structures, including single-electron memory. Since 2004, he has been a professor of intelligent device in the Department of Electrical Engineering and Computer Science, Graduate School of Engineering, Nagoya University, Japan. His main concerns are BioCMOS technology, single molecule-CMOS hybrid devices, CMOS analog circuits for integrated sensors, and nano-scale silicon devices.