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Validation of Solar PV Inverter Harmonics Behaviour at Different Power Levels in a Test Network

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***Abstract*—**Grid connected solar PV inverters need to be compliant to standard regulations regarding unwanted harmonic generation. This paper gives an introduction to harmonics, solar PV inverter voltage regulation and balancing through compensation and investigates the behaviour of harmonic generation at different power levels. Practical measurements of harmonics and power levels with a power quality data logger were made, on a test network at a university in Germany. The test setup and test results are discussed. The major finding was that between the morning and afternoon load peak windows when the PV inverters operate under low solar insolation and low power levels, more unwanted harmonics are generated. This has a huge impact on the power quality of the grid as well as capital and maintenance costs. The design of a single-tuned harmonic filter towards harmonic mitigation is presented.

***Keywords*—**Harmonics, power quality, pulse width modulation, total harmonic distortion.

I. Introduction

IN the electricity delivery process power electronic converters are employed at generation, transmission, and distribution levels of the grid. It comes at a price, however, since power electronics converters such as inverters generate a sea of unwanted harmonics, due to fast switching semiconducting devices. There is an increase in connecting renewable energy sources to the grid. Solar PV system inverters are designed to operate optimally at high efficiencies. However, the connection of grid-tied solar PV systems enhances power harmonics. This distorts the grid voltage. Constant research is being done on improving voltage regulation through reactive power control of PV inverters. Due to the increase of PV penetration, harmonic distortion on electrical networks generated from PV inverters is increasing. Reference [1] shows that when some PV inverters operate under low solar insolation, even more unwanted harmonics are generated. Solar insolation for PV systems is expressed as the average irradiance in kilowatt hours per year per kilowatt peak rating. Low solar insolation occurs during early mornings and late afternoons. During these periods, inverters operate at lower power levels and some employ reactive power compensation methods to increase the output voltage levels. Inverters used in grid-tied solar PV systems operate at low power conditions when there is a decrease in solar irradiation patterns such as overcast conditions or during early morning and late afternoon. During this low power operation, an inverter produces more undesirable harmonics due to the use of pulse width modulation (PWM), in the voltage control process. Inverters are an integral part of solar PV grid-tied systems, and undesirable harmonics. The low order harmonic amplitudes increase with a decrease in PV inverter output power [1]. Low solar irradiance has a significant impact on deteriorating power quality of the output of a PV system [2]. According to Salvatierra et al., it is even necessary to disconnect grid connected PV systems in the early hours of the morning in order not to affect the power quality of residential networks [3].

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II. Harmonics, THD and Distortion Factor

Harmonic currents flowing through power system impedances generate voltage harmonics and distort the supply voltage. The n[th] harmonic is equal to n times the fundamental frequency, namely n*f, where n is a positive integer. When n is a positive fractional number, an inter-harmonic (n*f) is generated. Inverters produce aforementioned harmonics that affects Total Harmonic Distortion (THD), Distortion Factor (DF) and Power Factor (PF). This relationship is shown in the following equations:

$$Power\ Factor = pf = \frac{P_{avg}}{V_{rms} * I_{rms}} \tag{1}$$

$$I_{rms} = \sqrt{(I_{dc})^2 + \sum_{k=1}^{\infty}(I_{k\_rms})^2} \tag{2}$$

$$P_{avg} = V_{1rms} * I_{1rms} \ * Displacement\ Factor \tag{3}$$

$$Distortion\ Factor = \frac{I_{1rms}}{I_{rms}} \tag{4}$$

$$THD = \frac{\sqrt{\sum_{k\neq 1}^{\infty} I_{k\_rms}{}^2}}{I_{1rms}} \tag{5}$$

$$Distortion\ Factor = \sqrt{\frac{1}{1+THD^2}} \tag{6}$$

$$pf = Displacement\ Factor * Distortion\ Factor \tag{7}$$

$$pf = cos\Theta * \sqrt{\frac{1}{1+THD^2}} \tag{8}$$

This shows that in order to determine the actual PF of a system, one need to measure the phase angle between the current and voltage fundamental as well as the THD of the current. So, the higher harmonic content, the worse the PF. THD is an indication of how much extra heat will be dissipated when a distorted voltage is fed to a resistive load. This ties up with (8) and is an indication of additional losses due to current flow [4]. Small currents may have high THD and it could be misleading, thus the fundamental of peak-demand current is referenced in Total Demand Distortion (TDD);

$$TDD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n{}^2}}{I_L} \tag{9}$$

where I_n is the magnitude of individual RMS harmonic components, and I_L is the maximum demand rms load current at fundamental frequency. The TDD current is normalized to the maximum demand load current in (5). TDD and THD would be the same at full load [5].

III. Inverter Voltage Regulation

High PV penetration causes voltage rises in LV grids, especially at the end of the line. Voltage fluctuation due to bi-directional power flow in grid-tied LV networks is illustrated in Fig. 1 [6]. Some PV inverters may switch off if an overvoltage limit is exceeded, if they adhere to the grid code. Solar PV inverters therefore need to be able to regulate their output voltage.

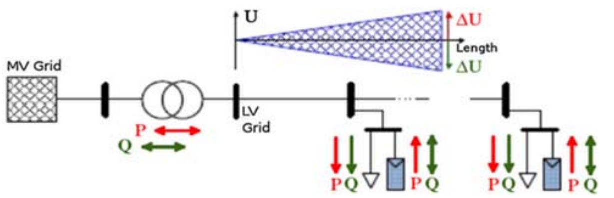


Fig. 1 Illustration of Voltage fluctuation in LV system [6]

PV inverters use PWM switching in semiconductor devices to convert DC to AC. This is very efficient, but PWM generates harmonics during the high dv/dt and di/dt semiconductor switching transients. High modulation frequencies are used to output a smoother sinusoidal AC voltage waveform and to keep the physical size of the LC filter small. Excessive noise and harmonics from grid-connected PV inverter systems may degrade the power quality of power networks to such an extent that it could cause disruption of utility network operation and/or sensitive equipment to malfunction [7]. Over voltage due to high PV penetration causes reduced lifetime of supply side equipment as well as demand side equipment [8].

A. Voltage Regulation and Balancing through Compensation

The EN50160 European grid standard prescribes a ±10% rated LV and MV voltage range. Changes in loads, supplies and reactive power-flows through transmission lines alter bus voltage values. A large number of solar PV inverters cause voltage instability due to intermittent power production due to varying solar irradiation patterns. A common technique to achieve voltage control is through reactive power compensation [8]. The following is a derivation of the optimal power equations (14) and (15) delivered by an inverter [9]:

The inverter output voltage is represented by Vs and the grid voltage by Vg in the schematic diagram of the model in Fig. 2. X_L is the leakage reactance of the line and transformer. Let's assume a unity PF and zero grid phase angle of the grid voltage. The inverter has to generate an output voltage Vs, with α the phase angle referenced to the grid voltage Vg. The active power is P and reactive power is Q.

$$S = V_g * I_s{}^* = P + jQ \tag{10}$$

$$I_s = \frac{V_s - V_g}{jIs * X_L} \tag{11}$$

$$S = V_g \left(\frac{V_s - V_g}{jIs * X_L}\right)^* \tag{12}$$

$$= \frac{V_s V_g}{X_L} sin\alpha + j(\frac{V_s V_g}{X_L} cos\alpha - \frac{V_g 2}{X_L}) \tag{13}$$

$$P = \frac{V_s V_g}{X_L} sin\alpha \tag{14}$$

$$Q = \frac{V_s V_g}{X_L} cos\alpha - \frac{V_g 2}{X_L} \tag{15}$$

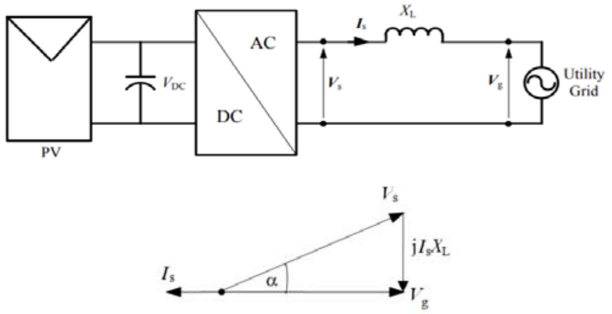


Fig. 2 Inverter equivalent circuit connected to utility grid and phasor diagram [9]

Voltage regulation and balancing through compensation in simulation using (14) and (15) conclude that the inverter under test needed reactive power levels of about 4% active power under maximum solar irradiation conditions [9].

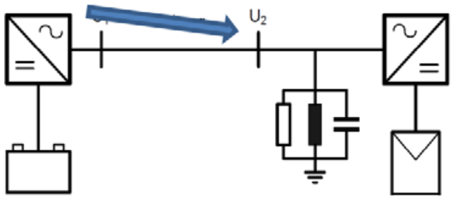
IV. Practical Measurements on the Test Network

Practical harmonic and THD measurements at various inverter power levels, were taken with a Power Quality meter on a LV test network at a university in Germany. The harmonic behavior was monitored.

A. Test Setup

The test setup is as shown in Figs. 3 (a) and (b). The grid was represented by a battery driven bi-directional 3-phase 240V SMA Sunny Island inverter shown on the left hand side and the test inverter on the left hand side a 5-kW single phase

240V SMA Sunny Boy solar PV inverter in Fig. 3. A 200W heater was used as the load. The arrows indicate point U_2 where the measurements were taken with the PQ meter. The PV array supply was simulated by an adjustable DC supply.



(b)

(a)

Fig. 3 (a) Inverter grid-connected test circuit (b) Schematic diagram of Inverter grid-connected test circuit

TABLE I
DIFFERENT INVERTER POWER LEVEL MEASUREMENTS

Power [W]	Current [A]	Voltage [V]
123	0.538	229.74
227	0.990	229.63
528	2.296	229.83
822	3.575	229.84
1118	4.862	229.98
1315	5.720	229.78
1696	7.380	229.75
2525	10.975	230.07
2882	12.526	230.11
4023	17.465	230.4

B. Test Results

Measurements were taken at power levels ranging from 124 W to 4023 W by adjusting the inverter MPPT, as shown in Table I. Fig. 4 shows that the inverter current amplitude of the 3rd harmonic increases linearly up to the 500 W and then almost stays constant up to the maximum power level. Fig. 5 shows that the inverter current amplitude of the 5th harmonic increases linearly up to the 1 kW then decreases to 2 kW and then increases again up to the maximum power level. Fig. 6 shows that the inverter current amplitude of the 7th harmonic behaves similarly to the 5th harmonic. Fig. 7 shows that the inverter current amplitude of the 9th harmonic increases linearly up to 1 kW then drops to 25 mA and stays constant up to the higher power levels. Figs. 8 and 9 show that the inverter current amplitude of the 11th and 13th harmonic increases but in a zig zag pattern. However, if we normalize these current harmonics to that of the current supplied by the inverter the pattern looks completely different as displayed in Figs. 9-14. The third harmonic is the most dominant and decreases exponentially as power in increased. All the harmonics (3rd to 13th) that were measured increases on average as the power is decreased.

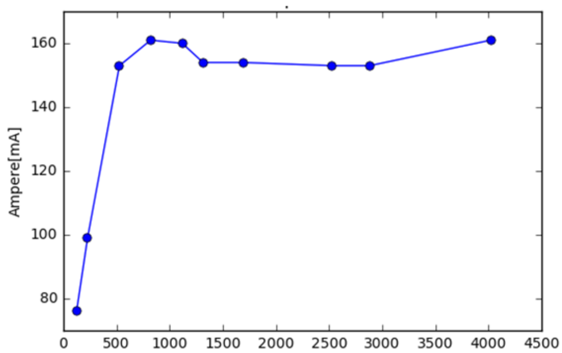


Fig. 4 3rd Current harmonic vs power levels [W] of inverter

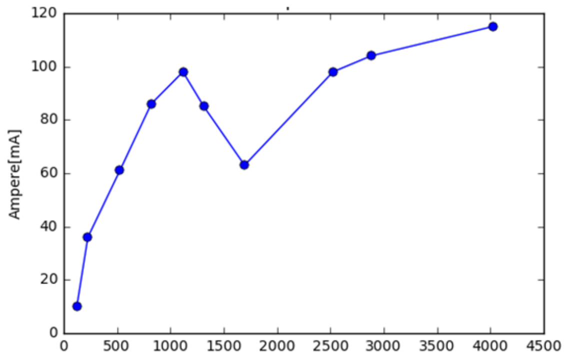


Fig. 5 5th Current harmonic vs power levels [W] of inverter

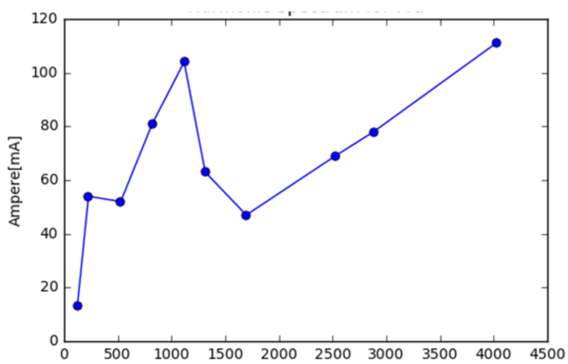


Fig. 6 7th Current harmonic vs power levels [W] of inverter

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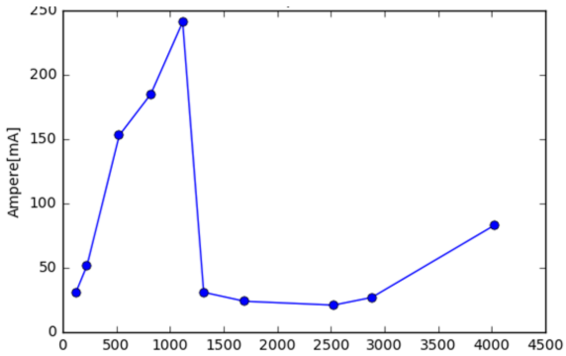

Fig. 7 9th Current harmonic vs power levels [W] of inverter

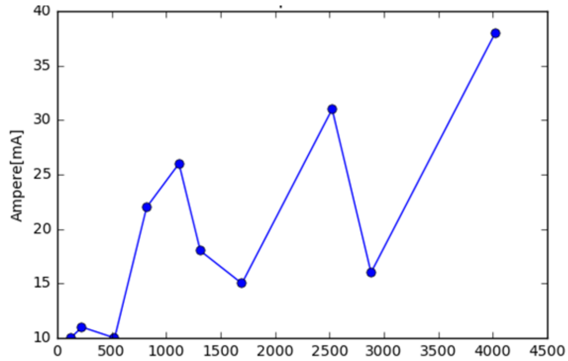

Fig. 8 11th Current harmonic vs power levels [W] of inverter

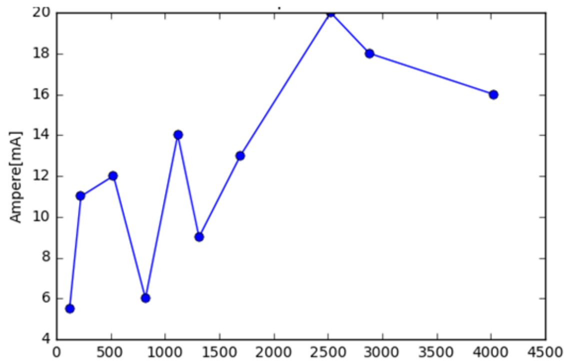

Fig. 9 13th Current harmonic vs power levels [W] of inverter

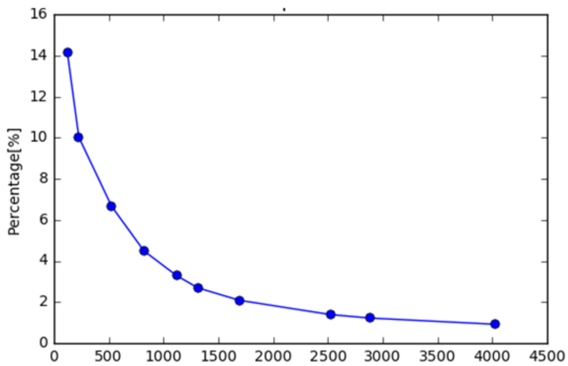

Fig. 10 Normalized 3rd Current harmonic (%) vs power levels [W] of inverter

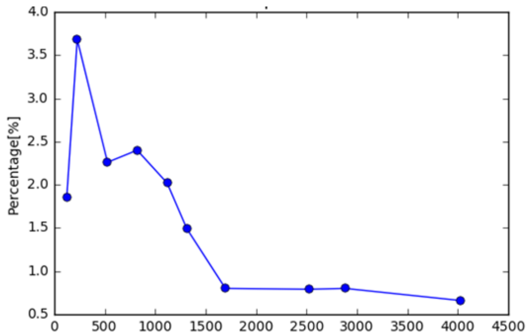

Fig. 11 Normalized 5th Current harmonic vs power levels [W] of inverter

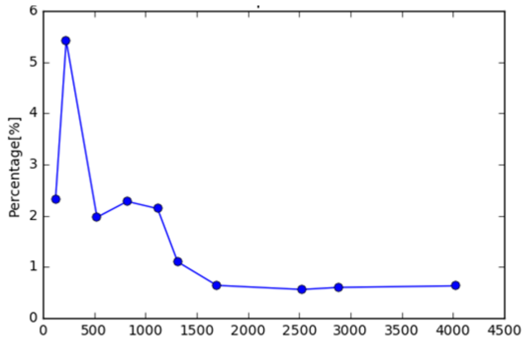

Fig. 12 Normalized 7th Current harmonic (%) vs power levels [W] of inverter

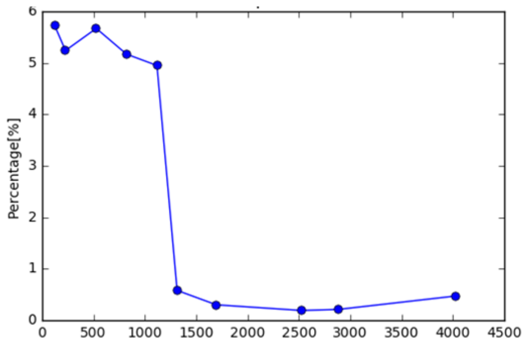

Fig. 13 Normalized 9th Current harmonic (%) vs power levels [W] of inverter

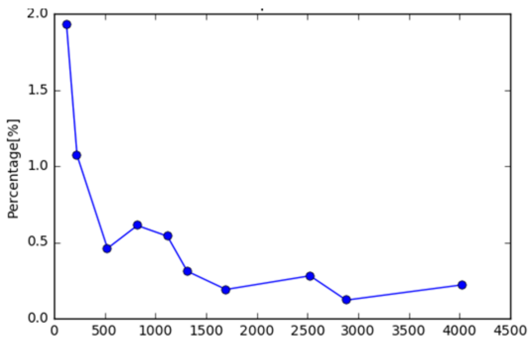

Fig. 14 Normalized 11th Current harmonic (%) vs power levels [W] of inverter

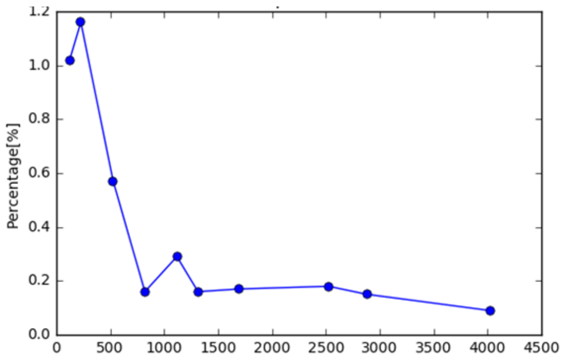

Fig. 15 Normalized 13th Current harmonic (%) vs power levels [W] of inverter

V. Harmonic Mitigation

One of the most common methods of harmonic reduction is through filtering. Line reactors or chokes can be installed on the line side the load. Harmonic trap filters, broadband filters or active filters can be installed to attenuate harmonic propagation, depending on the degree of voltage distortion. Notch filters are normally used to mitigate a specific harmonic. In order to design a notch filter, one needs the values of the facility bus voltage, the load in kVA, the PF and the total harmonic current produced by the load as a percentage of the fundamental current.

The harmonic single tuned filter design steps are as follows:

1. Selection of a tuned frequency for the filter: The tuned frequency is selected based on the harmonic characteristics of the loads where the power is applied. The filtering needs to start at the lowest harmonic frequency generated by the load. Say the 5th harmonic.
2. Calculation of capacitor bank size and the resonant frequency: In general, the filter size is based on the load reactive power requirement for PF correction. See the schematic diagram of the filter configuration in Fig. 16. The reactor size is selected to tune the capacitor to the required frequency. In this example, it is the 5th harmonic.

At the fundamental frequency; $X_{filter} = X_{cap} = X_L$ (16)

So, at the 5th harmonic; $X_{cap} = h^2\, X_L = 5^2\, X_L$ (17)

Since the capacitance value of the PF correction capacitor is known, the value of X_L can be calculated as;

$$X_{cap} = h^2\, X_L \tag{18}$$

3. Calculating filter reactor size: The filter reactor size can now be calculated to tune the capacitor to the desired frequency of the 5th harmonic;

$$X_{L(fund)} = \frac{X_{Cap\,(wye\ or\ delta)}}{h^2} \tag{19}$$

4. Evaluation of the filter frequency response. Now the filter frequency response needs to be evaluated to ensure that the filter is not generating a new resonance at a frequency that could cause additional issues. The harmonic at the parallel resonance below the notch frequency is calculated as follows:

$$h_0 = \sqrt{\left[\frac{X_{cap\,(wye\ or\ delta)}}{X_{T\,(fund)} + X_{L\,(fund)}}\right]} \tag{20}$$

5. Evaluation with tolerances: Generally, the tolerance for the capacitors are +15% and +/- 5% for the inductance. These tolerances can sometimes make a big difference and can create harmful resonance [10].

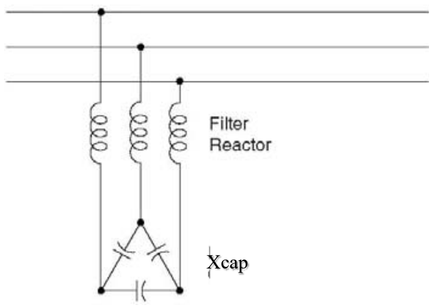

Fig. 16 Filter configuration [10]

Harmonic trap filters are LC configured, shunt connected and tuned below the normally large 5th harmonic. In this way, the 7th harmonic is also being attenuated. Broadband filters are connected in series and also serves as protection to adjustable frequency drives (AFDs). It attenuates all harmonics including the third harmonic. Active filters are installed at the end bus of power distribution lines, to attenuate harmonic propagation resulting from resonance between PF correction capacitors and line inductors. The active filter acts as a low resistor to the external circuit and cancels all harmonics up to the 50th one [11].

VI. Conclusions

THD increase with low levels of solar irradiance and some go above the 5% THD limit set by the IEEE and IEC power network standards [12]. It has been shown that current THD increases with a decrease in solar irradiation (W/m^2) levels and that current THD decreases with an increase in inverter output current or power [13]. This relates to [14] that refers to high current THD under low generation and low current THD under high generation conditions according to (9). This is validated by the test results due to the fact that the magnitude of the different normalized odd harmonics decreased with an increase in the inverter power/current levels (Figs. 10-15). The decrease in harmonics is also proportional to an increase in solar irradiation levels. It was clearly shown that the majority of individual harmonic terms increase with a decrease in power levels. Equations (6)-(8) show that at low power levels (high THD) the PF decreases significantly. Electricity consumption costs will also increase due to higher harmonic content that results in a poor PF. The measurements of PV inverter harmonics behaviour at lower power levels in the test network validated some of the previous research done on the topic in [1]-[14]. The capital and maintenance costs are increased, in cases where a single-tuned harmonic filter design is insufficient to reduce harmonic distortion. This leads to multiple filter designs to attenuate, for example the 5th, 7th and 11th harmonic, particularly when dealing with large loads.

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