International Journal of Information, Control and Computer Sciences
ISSN: 2517-9942
Vol:2, No:6, 2008

UML Modeling for Instruction Pipeline Design

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***Abstract*—**Unified Modeling language (UML) is one of the important modeling languages used for the visual representation of the research problem. In the present paper, UML model is designed for the Instruction pipeline which is used for the evaluation of the instructions of software programs. The class and sequence diagrams are designed & performance is evaluated for instructions of a sample program through a case study.

***Keywords*—**UML, Instruction Pipeline, Class Diagram & Sequence Diagram.

I. Introduction

UML is a powerful modeling language used to represent the research problems visually. A lot of literature is available on modeling problems by the use of UML, but limited research papers are reported in literature on applications of UML for the computer architecture research problems. By the use of UML, software and hardware architecture problems can be solved and performance can be judged after modeling of the problem. Real time system based on UML model is described by Selic and Rumbaugh[1]. The first represented of UML in the field of telecommunication sector is proposed by Holz [2]. The concept of UML was first invented by the Greddy Booch et al. [3]. The UML application is also proposed by the researchers for the web based application & one of the important papers on this is [4]. Various computer architecture models which can be used for the further research work are available in [5]. The latest research in 2007 on distributed computing is reported by the researchers [6]. UML based Vehicle control system is also reported in the literature by Walther et al. [7]. OMG is an important active group for inventing the different versions of the UML. The research papers on these are [8, 9] in which group describes the UML diagram based on XML meta data specification. Performance modeling and prediction tool for parallel and distributed programs are described by Planna et al. [10, 11] and also describe customizing the UML for modeling performance oriented applications. Recently Saxena et al. [12] proposed a UML model with performance computation for the Multiplex System for the processes which are executing in the distributed environment.

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The present research work is an attempt for proposing a model for instruction pipeline design through the concepts of UML. This model is designed for the execution of multiple instructions of software programs. These instructions can be executed either in sequential or parallel manner. The class and sequence diagrams are designed and a case study is also reported for the verification of the proposed UML model and performance is also evaluated for the instructions executed in the sequential or parallel manner. By the use of proposed model one can increase the efficiency of the computer system. Earlier software and hardware architecture models are designed on the basis of top down approach but the present model is based upon the bottom up approach which is much faster in comparison of the existing approaches.

II. Background

A. Process

Let us first define the process which may be the group or block of instructions of program, macro, sub programs and subroutines. For defining the process, there is a need of the processing element. The processing element is defined as a stereotype and generally used to handle the concurrent processes executing in the parallel and distributed environments. The famous approach to handle the concurrent processes is Torus Topology. Fig. 1 shows the definition of processing unit

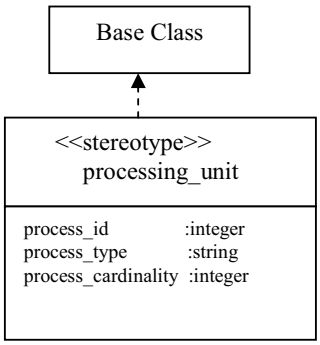


Fig. 1 Definition of Processing Unit

The class diagram of process is defined in Fig. 2.

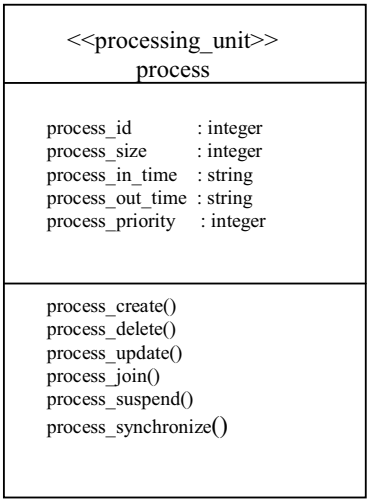


Fig. 2 Class definition of process

The instance of the process is defined by the use of object xyz which is shown in Fig. 3:

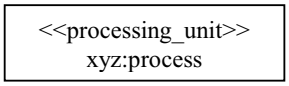


Fig. 3 Instance of class

The set of the instances of the class process is modeled by the use of multiple objects which is shown below:

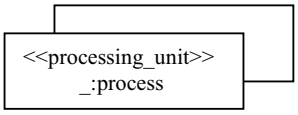


Fig. 4 Multiple instances of object

In above figure _:process shows the name of multiple objects.

B. Instruction Pipeline Design

Let us define the concept of the instruction pipeline design. In this design, stream of instructions are executed in the overlapped manner by the use of different kinds of buffer. These instructions are executed either in sequential manner or in parallel manner. There are seven stages in the instruction pipeline design which are needed to be model by the use of UML for increasing the efficiency of computer system. The seven stages of instruction pipeline design are shown below in Fig. 5.

In the Fig. 5 instruction is first fetched (F) from cache memory generally one per cycle and then decoded (D) the instruction according to the resources. In the issue (I) stage, pipeline reserves the right to issue the secure instruction and after this in the several stages, instructions are executed (E) and finally write (W) the results by the Write Back Method. Any Instruction of a program like c = a+b, and c = axb can be computed by the use of the above diagram.

III. Proposed UML Model

The UML modeling is necessary to judge the performance of the instruction pipelining design. The portion of the UML Class Model for the Instruction Pipeline Design is shown below in Fig. 6. In this figure the block or group of instructions of a process are fetched by the Cache Memory which may be the type of instruction cache (I_Cache) and data cache (D_Cache). Instruction cache handles the number of instructions of a program while data cache handles the required data used for execution of the corresponding instruction.

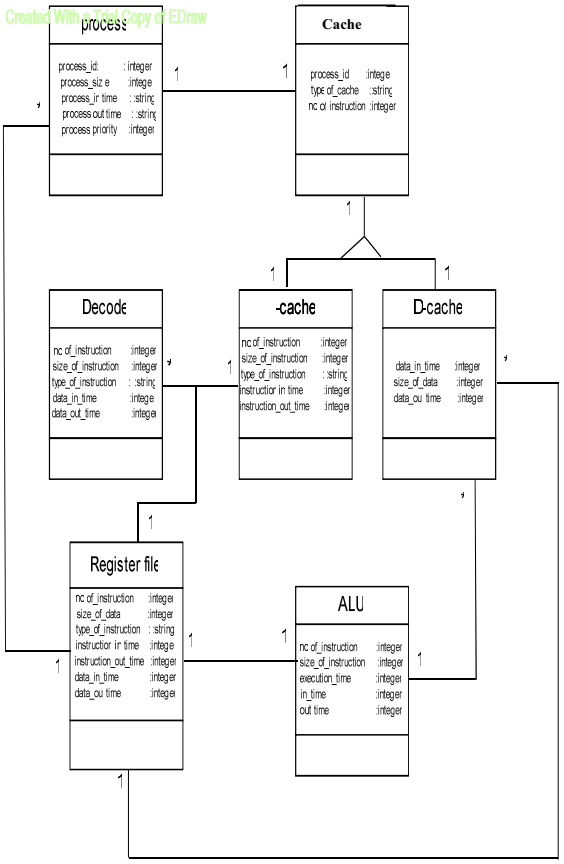


Fig. 6 UML Class Diagram for Instruction Pipeline

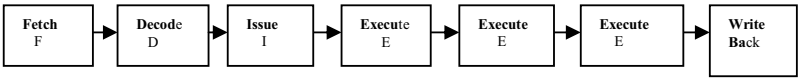


Fig. 5 Seven stages of Instruction Pipeline design

Relationships among the classes are shown in given Figure. After fetching the instructions, these are decoded and finally executed in the Arithmetic Logical Unit (ALU class) and outputs are stored into the register file by the use of Write Back Method. The Sequence Diagram for the execution of the instructions of a program is also given in Fig. 7.

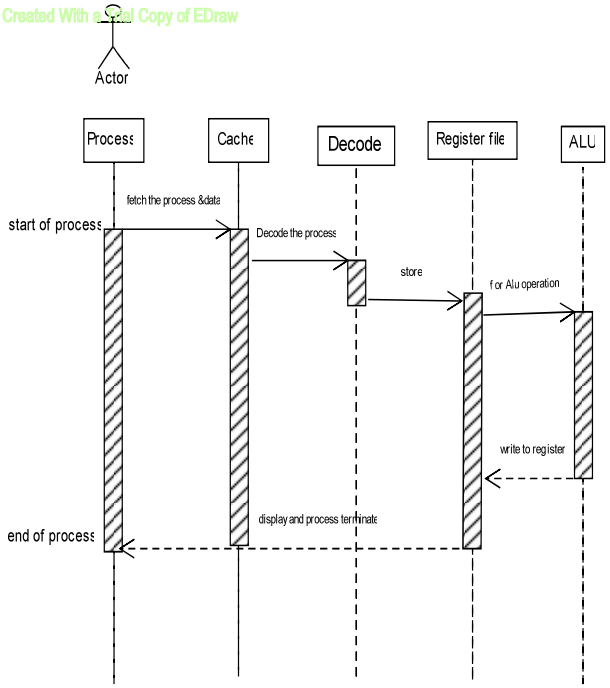
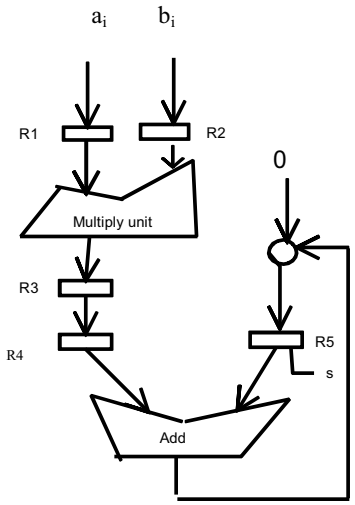


Fig. 7 Sequence Diagram of Instruction Pipeline

IV. A Case Study

Let us consider the example which is to be executed by the use of proposed UML model. In the instruction pipeline design, there are two techniques used to evaluate the block or group of instructions. These two techniques are known as With Internal Data Forwarding and Without Data Forwarding. In the example, one wants to evaluate $S= \sum a_i x b_i$ where the range of i=1(1)n. Without data forwarding, the instructions are written by the use of register file in which major portion for the computations are shown by three instructions as shown in Fig. 8.

In the block of instructions as shown in figure, the three instructions are executed in the sequential manner and in looping structure by the use of ALU class of above model. With Internal Data Forwarding, the instructions are written below by the use of register file in which major portion for the computations are shown by three instructions. These instructions are shown below as per following Fig. 9. In this



$R_1 = a(1)$
$R_2 = b(1)$
$I_1: R_3 \leftarrow (R_1) \times (R_2)$
$I_2: R_4 \leftarrow (R_3)$
$I_3: R_5 \leftarrow (R_5) + (R_4)$

Fig. 8 Without Data Forwarding

I_1' and I_2' can be executed simultaneously with the internal data forwarding. In this, these three instructions are fetched directly into the input register file R_4 of above class model. The output of the multiplier is also routed through the register R_3. This reduces the total execution time of the three instructions.

$R_1 = a(1)$
$R_2 = b(1)$
$I'_1: R_3 \leftarrow (R_1) \times (R_2)$
$I'_2: R_4 \leftarrow (R_1) \times (R_2)$
$I'_3: R_5 \leftarrow (R_4) + (R_5)$

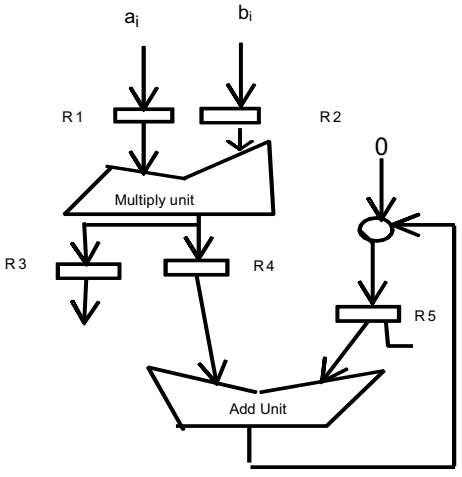


Fig. 9 With Internal Data Forwarding

In both of the techniques, the numbers of instructions are same but executed in the different manner. The second technique is most popular technique and performance is evaluated and found that the Internal Data Forwarding reduced the total execution time of these three instructions.

V. Conclusion

From the above, it is concluded that the UML Class model is a powerful model used to depict the software development problems and the hardware problems. In the Instruction Pipelining Designing, the Internal Data Forwarding saves the execution time of the block or group of instructions of the process. The present work is further extended by considering the different kinds of instructions executed in the different kinds of the buffer known as sequential buffer, loop buffer, target buffer, etc. The present work is considered only for the linear Instruction Pipeline Design therefore, the UML modeling application for Instruction Pipeline Designing can be further extended for the non-linear Instruction Pipeline Designing.

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