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Third Order Current-mode Quadrature Sinusoidal Oscillator with High Output Impedances

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***Abstract*—**This article presents a current-mode quadrature oscillator using differential different current conveyor (DDCC) and voltage differencing transconductance amplifier (VDTA) as active elements. The proposed circuit is realized fro m a non-inverting lossless integrator and an inverting second order low-pass filter. The oscillation condition and oscillation frequency can be electronically/orthogonally controlled via input bias currents. The circuit description is very simple, consisting of merely 1 DDCC, 1 VDTA, 1 grounded resistor and 3 grounded capacitors. Using only grounded elements, the proposed circuit is then suitable for IC architecture. The proposed oscillator has high output impedance which is easy to cascade or dive the external load without the buffer devices. The PSPICE simulation results are depicted, and the given results agree well with the theoretical anticipation. The power consumption is approximately 1.76mW at ±1.25V supply voltages.

***Keywords*—**Current-mode, oscillator, integrated circuit, DDCC, VDTA.

I. Introduction

An oscillator is an important basic building block, which is frequently employed in electrical engineering applications. Among the several kinds of oscillators, a quadrature oscillator is widely used because it can offer sinusoidal signals with 90° phase difference, for example, in telecommunications for quadrature mixers and single-sideband [1].

Several implementations of second order quadrature oscillators using different high-performance active building blocks, such as, OTAs [2], current conveyors [3], four-terminal floating nullors (FTFN) [4-5], current follower [6], current differencing buffered amplifiers (CDBAs) [7], current differencing transconductance amplifiers (CDTAs) [8], fully-differential sec-ond-generation current conveyor (FDCCII) [9], and differencing voltage current conveyor (DVCCs) [10], have been reported. Recently, it has been proved that the third order oscillator provides good characteristic with lower distortion than second order oscillator [11-12]. From our literature found that the third order oscillator employing CCCIIs [11], OTAs [12-13], CDTAs [14], have been proposed.

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The aim of this paper is to propose a third order current-mode oscillator, based on DDCC and VDTA. The features of the proposed circuits are that: the oscillation condition can be adjusted independently from the oscillation frequency by electronic method. The circuit construction consists of 1 DDCC, 1 VDTA, 1 grounded resistor and 2 grounded capacitors. The PSPICE simulation results are also shown, which are in correspondence with the theoretical analysis.

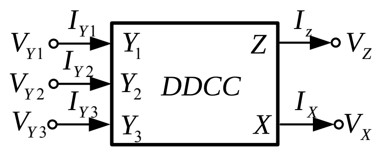
II. Theory and Principle

A. Basic Concept of DDCC

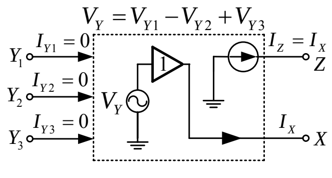
The electrical behaviors of the ideal DDCC are represented by the following hybrid matrix [15]:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \end{bmatrix}. \quad (1)$$

The symbol and the equivalent circuit of the DDCC are illustrated in Fig. 1(a) and (b), respectively.



(a)



(b)

Fig. 1 DDCC (a) Symbol (b) Equivalent circuit

B. Basic Concept of VDTA

The circuit symbol of VDTA is shown in Fig. 2, where V_P and V_N are the input terminals, Z and X are the output ones. Hence, Z is the current output terminal; current through Z terminal follows the difference of the voltages at V_P and V_N terminals by transconductances g_{m1}. The voltage v_Z on Z terminal is transferred into current using transconductance g_{m2}, which flows into output terminal X. The g_{m1} and g_{m2} are tuned by I_{B1} and I_{B2}, respectively. In general, CDTA can contain an arbitrary number of x terminals, providing currents I_X of both directions. All terminals of VDTA exhibit high impedance values [17]. The characteristics of the ideal VDTA are represented by the following hybrid matrix:

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}. \quad (2)$$

If the VDTA is realized using CMOS technology, g_{m1} and g_{m2} can be respectively written as

$$g_{m1} = \sqrt{kI_{B1}}\ , \quad (3)$$

and

$$g_{m2} = \sqrt{kI_{B2}}\ . \quad (4)$$

Here k is the physical transconductance parameter of the CMOS transistor. I_{B1} and I_{B2} are the bias current used to control the g_{m1} and g_{m2}, respectively.

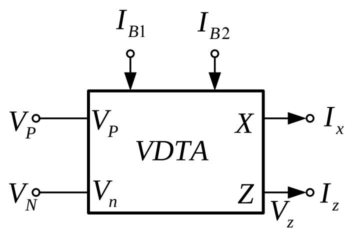


Fig. 2 The circuit symbol of VDTA

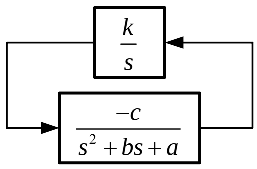


Fig. 3 Block diagram for design of proposed oscillator

C.General Structure of 3rd oscillator

The oscillator is designed by cascading an inverting second order low-pass filter and the lossless integrators as systematically shown in Fig. 3 [13]. From block diagram in Fig. 3, we will receive the characteristic equation as

$$s^3 + bs^2 + as + ck = 0 \quad (5)$$

From Eq. (5), the condition of oscillation (OC) and frequency of oscillation (FO) can be written as

$$OC : ab = ck \quad (6)$$

and

$$\omega_{osc} = \sqrt{a} \quad (7)$$

From Eq. (5), if $a = c$, the oscillation condition and oscillation frequency can be adjusted independently, which are the oscillation condition can be controlled by *b* and *k*, while the oscillation frequency can be tuned by *a*.

D.Proposed Oscillator

The completed 3rd current-mode quadrature oscillator is shown in Fig. 4. The condition of oscillation and frequency of oscillation can be written as

$$\frac{1}{C_1 R} = \frac{g_{m2}}{C_3}\ , \quad (8)$$

and

$$\omega_{osc} = \sqrt{\frac{g_{m1}}{C_1 C_2 R}}\ . \quad (9)$$

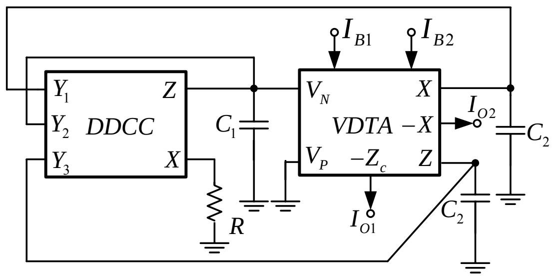


Fig. 4 Proposed current-mode oscillator

If $g_{m1} = \sqrt{kI_{B1}}$, $g_{m2} = \sqrt{kI_{B2}}$ and $C_1 = C_2 = C_3 = C$, the condition of oscillation and frequency of oscillation can be rewritten as

$$\frac{1}{R} = \sqrt{kI_{B2}}\ , \quad (10)$$

and

$$\omega_{osc} = \frac{1}{C}\sqrt{\frac{(kI_{B1})^{\frac{1}{2}}}{R}}\ . \quad (11)$$

It is obviously found that, the condition of oscillation and frequency of oscillation can be adjusted independently, which are the oscillation of oscillation can be controlled by setting

I_{B2}, while the frequency of oscillation can be tuned by setting I_{B1}. From the circuit in Fig. 4, the current transfer function from I_{o1} to I_{o2} is

$$\frac{I_{o2}(s)}{I_{o1}(s)} = \frac{g_{m1}}{sC_2}. \tag{12}$$

For sinusoidal steady state, Eq. (12) becomes

$$\frac{I_{o2}(j\omega)}{I_{o1}(j\omega)} = \frac{g_{m1}}{\omega C_2} e^{-j90^\circ}. \tag{13}$$

The phase difference ϕ between I_{o1} and I_{o2} is ϕ = -90° ensuring that the currents I_{o2} and I_{o1} are in quadrature.

III. Results of Computer Simulation

The working of the proposed oscillator has been verified in PSpice simulation. Internal constructions of DDCC and VDTA used in simulation are respectively shown in Figs. 5 and 6. The PMOS and NMOS transistors have been simulated by respectively using the parameters of a 0.25μm TSMC CMOS technology [16]. The transistor aspect ratios of PMOS and NMOS transistor are indicated in Table I. The circuit was biased with ±1.25V supply voltages, V_{BB}=-0.55V, C_1=C_2=C_3=50pF, I_{B1}=I_{B2}=60μA and R=3.5kΩ. This yields simulated oscillation frequency of 1MHz. Fig. 7 shows simulated quadrature output waveforms. Fig. 8 shows the simulated output spectrum, where the total harmonic distortion (THD) is about 2.95%. The quadrature relationship between the generated waveforms has been verified using Lissagous figure and shown in Fig. 9. The power consumption is approximately 1.76mW.

TABLE I
Dimensions of the Transistors

Transistor	W (μm)	L (μm)
M_1-M_4	3	0.25
M_5-M_8	1	0.25
M_9-M_{10}	10	0.25
M_{11}-M_{12}, M_{13}-M_{16}	5	0.25
M_{17}-M_{20}	8	0.25

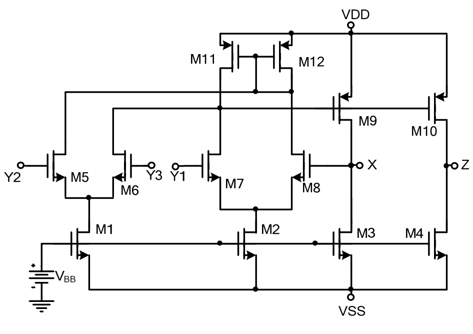


Fig. 5 Internal construction of the CMOS DDCC

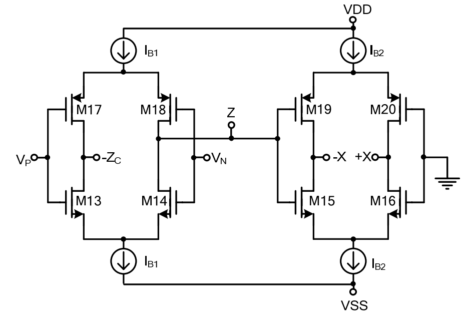


Fig. 6 Internal construction of the CMOS VDTA [17]

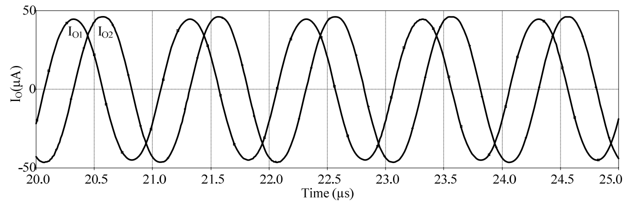


Fig. 7 The simulation result of quadrature outputs

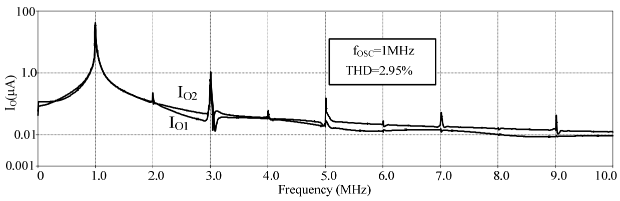


Fig. 8 Frequency spectrum of signal in Fig. 7

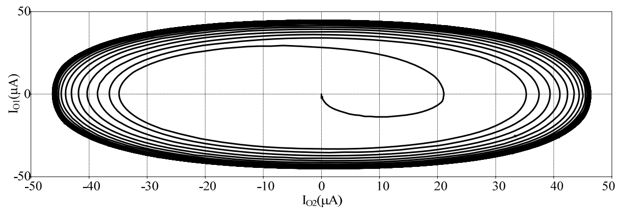


Fig. 9 Relative of the output waveform

IV. Conclusion

A 3rd current-mode quadrature sinusoidal oscillator based on DDCC and VDTA has been presented. The features of the proposed circuit are that: oscillation frequency an oscillation condition can be orthogonally adjusted via input bias current; it consists of 1 DDCC, 1 VDTA, 1 grounded resistor and 3 grounded capacitors, which is convenient to fabricate. The PSPICE simulation results agree well with the theoretical anticipation.

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