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Thermal Evaluation of Printed Circuit Board Design Options and Voids in Solder Interface by a Simulation Tool

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***Abstract*—**Quad Flat No-Lead (QFN) packages have become very popular for turners, converters and audio amplifiers, among others applications, needing efficient power dissipation in small footprints. Since semiconductor junction temperature (T_J) is a critical parameter in the product quality. And to ensure that *die* temperature does not exceed the maximum allowable T_J, a thermal analysis conducted in an earlier development phase is essential to avoid repeated re-designs process with huge losses in cost and time.

A simulation tool capable to estimate *die* temperature of components with QFN package was developed. Allow establish a non-empirical way to define an acceptance criterion for amount of voids in solder interface between its exposed pad and Printed Circuit Board (PCB) to be applied during industrialization process, and evaluate the impact of PCB designs parameters. Targeting PCB layout designer as an end user for the application, a user-friendly interface (GUI) was implemented allowing user to introduce design parameters in a convenient and secure way and hiding all the complexity of finite element simulation process. This cost effective tool turns transparent a simulating process and provides useful outputs after acceptable time, which can be adopted by PCB designers, preventing potential risks during the design stage and make product economically efficient by not oversizing it.

This article gathers relevant information related to the design and implementation of the developed tool, presenting a parametric study conducted with it. The simulation tool was experimentally validated using a Thermal-Test-Chip (TTC) in a QFN open-cavity, in order to measure junction temperature (T_J) directly on the *die* under controlled and knowing conditions. Providing a short overview about standard thermal solutions and impacts in exposed pad packages (i.e. QFN), accurately describe the methods and techniques that the system designer should use to achieve optimum thermal performance, and demonstrate the effect of system-level constraints on the thermal performance of the design.

***Keywords*—**Quad Flat No-Lead packages, exposed pads, junction temperature, thermal management and measurements.

I. Introduction

THE size reduction and the increase of the features included in electronic devices result in energy consumption in concentrated regions [1]. At high current densities, around 10W/cm2 and considering systems with operating frequencies in the GHz order and complex layout imposed by technological developments, there are a growing number of challenges related with optimization of heat dissipation path [2], [3].

An economically efficient management of thermal properties is among the main priorities in the engineering of electronic components, with a tendency to produce circuits with 3D functional characteristics [2].

Nowadays, the numerical simulations performed during thermal analysis demonstrate that the increase of T_J may degrade the performance of electronic components by more than a third. Therefore, it is essential and desirable to promote passive optimized solutions - increasing heat transfer phenomena before the production process [2], [4]. This approach can be accurately predicting the thermal performance of integrated components (IC) without build a prototype. Anyway, it can be concluded that inclusion of materials with better thermal conductivity will allow adequate heat dissipation. In this sense, include metals (such as copper, whose thermal conductivity is about 386 W/mK at room temperature), compared to polymeric materials having a lower thermal conductivity [3]. The approach considers critical components with exposed pad to allow the heat transfer from the package to the environment, through the PCB layers.

The numerical calculations are governed by the conservation laws expressed by Navier-Stokes and converted in the form of infinite volume, which involves the calculation of temperature, pressure and speed for a given volume [5]. Allowing the calculation of the heat flow and thermal fields generated in the representative model and for different heat transfer coefficients. Whereas volume elements through the mesh refinement, yielding higher resolution as the volume decrease. There still the needed to re-design the 3D mesh system taking into account aspects related to the high mesh refinement and boundary conditions to eliminate dependencies of numerical solution with the mesh. The transfer phenomena and also the fluid flow are considered in the solver methodology which follows a set of conservation laws presented herein. Considering the fluid flow, the methodology obeys in the first instance to the conservation of mass and quantity linear motion [5]:

$$\nabla . \mathbf{u} = 0 \quad (1)$$

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$$\rho\left[\frac{\partial \mathbf{u}}{\partial t} + \nabla.\mathbf{uu}\right] = -\nabla p + \nabla\boldsymbol{\tau} \quad (2)$$

where, u is the fluid velocity vector, ρ the density of the fluid, τ the stress tensor with a pressure p. Equations (1) and (2) are deducted from a balance of forces and movement amount of an infinitesimal volume of fluid, also called representative volume element. Additionally, is still necessary to consider the energy conservation equation to heat transfer:

$$\rho\frac{\partial \mathbf{e}}{\partial t} + \rho\nabla.(\mathbf{eu}) - \nabla.(\delta\nabla\mathrm{T}) = \rho g.\mathbf{u} - \nabla.(p\mathbf{u}) + \rho Q \quad (3)$$

with δ is the transport coefficient, T the temperature and Q a load quantity subject to a gravity force g.

Considering a bulk-like solid-state material, the thermal conductivity (k) can be defined by first-order Fourier-Biot equation: $k = \frac{\Delta Q}{\Delta t}\frac{1}{A}\frac{\Delta x}{\Delta T}$, as the quantity of heat (ΔQ), transmitted during time Δt through a thickness Δx, in a direction normal to a surface of area A, due to a temperature difference ΔT, under a steady-state conditions and when the heat transfer is dependent only on the temperature gradient [6].

The project motivation is related with voiding phenomenon which occurs in solder interface underneath the exposed pad of BTC (Bottom Terminated Components), such as QFN packages. The discontinuity in solder interface is caused by voiding that raises concerns in the product reliability. In terms of thermal dissipation efficiency, there is no established acceptance criterion, since critical voiding level is application dependent. The acceptance criterion is a topic of some speculations and discussions. There are real production situations for which acceptance criterion appears to be too much restrictive, without benefit, causing unjustified production rejections. Within this motivation was decided to conduct a parametric study to evaluate the impact of solder discontinuity area and PCB design options in the degradation of thermal efficiency. The optimization process is to define the parameters that maximize the transfer phenomena, which gives a proper system configuration that is thermally and reliability improved. Same methodologies are presented and compared by [4]. Husain and Kim also used the methodology based on GA (Genetics Algorithms) to search for the optimal solutions and avoid numerical costs [7].

A. Thermal Management in Integrated Circuits (IC)

The semiconductor manufacturers encourage the adoption of BTC (Bottom Termination Components) packages due to its low price, while electronic engineers advise it due to the fact that these types of packages provide an efficient thermal dissipation through the PCB [8]. The mechanical connection medium is usually called exposed pad and components that present this package are usually called BTC, that gathers a variety of components including QFN (Quad Flat No-Lead), DFN (Dual Flat No-Lead), SON (Small-Outline No-Leads), LGA (Land Grid Array) and MLF (Micro Lead Frame), among others [9]. The silicon die of the component is placed on top of the lead frame which is connected to the PCB. The purpose of the exposed pad is to promote a way of low thermal resistance between the silicon die of the component and the structure to which it is attached. To highlight the main function of this structural feature, the exposed pads are also often referred to as thermal flags [9]. The exposed pad is located under the component resulting in low thermal resistance path between the chip and the PCB. Thereby, the PCB becomes a kind of heat sink. It is an economically efficient solution but it requires a set of cautions to ensure optimal performance and reliability of the system to be met [8], [10].

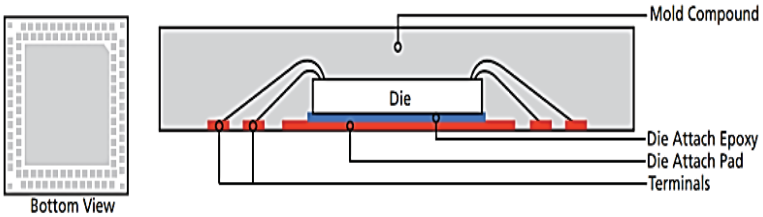


Fig. 1 Bottom View and Cross Section of Dual-Row QFN Package [11]

Nowadays, there are in the market cost-efficient solutions with optimal thermal characteristics. Due to excellent thermal and electrical characteristics, the packages with exposed pad (e.g. QFN) were introduced in the late 80s. Despite its advantages, such packages suffer major thermal and mechanical problems related to reliability problems [11]. These problems are mainly due to differences in thermal and mechanical characteristics of the various materials involved [12]. And the critical function of a package is to dissipate heat from the die to absorb strain resulting from the mismatch of coefficients of thermal expansion (CTE) of the die, substrate, and the integrated heat spreader (IHS) during temperature cycling.

Additionally, the electronic industries as another important challenge, find an adequate solder paste volume for the welding process of components. Decreasing the solder paste volume, short-circuit are eliminated but thermal efficiency and also the reliability could not be enhanced (e.g. fatigue caused by thermal cycling, vibration or shocks) [13], [14].

The power consumed by integrated circuit (IC) is dissipated on the surface of its die in the form of heat, rising up the semiconductor junction temperature. The electronic components manufacturers characterize the thermal behavior of encapsulated devices by defining an equivalent thermal

resistance (θ_{JA}) for a power dissipated on the die surface (P_{diss}). Thus, the junction-to-ambient equivalent thermal resistance can be expressed as [13]:

$$\theta_{JA} = \frac{\Delta T_{JA}}{P_{diss}} = \frac{(T_j - T_A)}{P_{diss}} \quad (4)$$

The junction temperature is a critical parameter for product's quality and for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. The maximum junction temperature is a limiting worst case that should not be exceeded, which should be guaranteed by ensuring a significant margin of safety.

B. Impact of Voiding Phenomena on Thermal Efficiency

Voids are caused by the amount of outgassing flux that gets entrapped in the solder joint during reflow. The reliability of a solder joint may depend not only on the size, but also on location and frequency. The factors that affect the void formation are complex and depend on the interaction of many factors [14]. Nowadays, the inspection criteria have been very subjective, and there are no established standards for void size and area in a solder interface for it to be deemed defective [15]. These discontinuity areas in solder interface between exposed pad and PCB and can be inspected by x-ray equipment (Fig. 2). The darker areas correspond to solder settled between exposed pad and PCB, while lighter areas correspond to voids formed during the process of gas released which can cause reliability problems. The short circuits risk is minimized by reducing the solder paste volume.

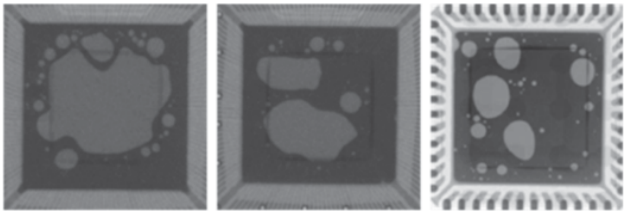


Fig. 2 *Voids* inspection in solder interface with an x-ray equipment

The solder interface between the exposed pad and PCB is part of the main thermal dissipation path. Ideally, the solder interface would not have any discontinuity. In this case, its geometry could be seen as an orthogonal parallelepiped which base has dimensions of exposed pad and which height is equal to the component stand-off in relation to the PCB. The following expression defines the absolute thermal resistance along orthogonal parallelepiped body as a function of its material and its dimensions: $\theta = \frac{1}{k}\frac{x}{A}$ where, k is the thermal conductivity of the material with length and a section area (A) of the exposed pad [13]. According to the previous expression, the thermal resistance is inversely proportional to the section area. It means that, with the area reduction, the thermal resistance increases. The increase of the discontinuity area caused by voiding leads to the breakdown of thermal dissipation efficiency and could lead to a high semiconductor junction temperature. This statement causes a concern in terms of the reliability of the final product.

C. Optimizing PCB Layout to Reach Thermal Performance

According to the EIA/JEDEC Standard, are considered the following impact factors on thermal resistance (θ_{JA}) that leads to an increased thermal efficiency [10]: the PCB Design reaches almost 100%, with the increase of PCB layer (FR-4) or copper layers leads to a decrease in thermal resistance (θ_{JA}). And the decrease of PCB layer (FR-4) thickness leads to a decrease of thermal resistance (θ_{JA}). Additionally, the chip dimension has an impact of 50% on thermal resistance, followed by the package configuration with 35%. The external factors, like the temperature reaches almost 7% and the altitude 18%. The lowest value is for power dissipation with an impact value up to 3% on thermal resistance. So, the process of optimization of thermal dissipation can be decomposed in optimizing actions across following parts of physical model:

- Solder interface between exposed pad and PCB;
- Conducting to the PCB top layer;
- Conducting across the thermal vias;
- Conducting along the PCB out of the component;
- Convection between the surfaces of the PCB and surrounding air bulk.

These paths can be seen as a specific thermal resistance that makes part of thermal resistance network between the component and the ambient (θ_{ja}), as shown in Fig. 3 [16].

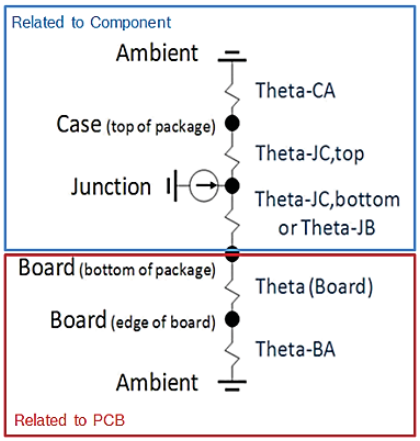


Fig. 3 Thermal resistance equivalent model (2-R)

Excluding convection and radiation associated with the surfaces of the package, all paths of heat conduction are going through exposed pad, solder layer that connects it to the PCB and top layer copper. Thus, special care should be taken with respect to the interface in this range of heat conduction paths. The FR-4 (fiberglass-reinforced epoxy laminate) is one of the most commonly used PCB materials with a very low thermal conductivity. And an inexpensive way to improve thermal transfer for FR-4 PCBs is to add thermal vias - plated through-holes between conductive layers [13]. In order to effectively transfer heat from the top metal layer of the PCB to the inner

or bottom layers, thermal vias must be incorporated into the thermal pad design. The number of thermal vias will depend on the application, power dissipation, and electrical requirements. However, increase thermal vias will improve the package's thermal performance, but there is a point of diminishing returns where additional thermal vias may not significantly improve the performance [17].

II. Simulation Tool for Thermal Optimization of IC with Exposed Pad

The present article shows a thermal study of components, depending on PCB design options and voids in solder interface between the exposed pad and PCB. For this propose, a numerical tool based on a commercial finite element method, was developed to evaluate the thermal behavior of components with exposed pad (e.g. QFN). The simulation software was implemented, through creation of ANSYS Parametric Design Language (APDL) scripts, which can be adopted by PCB developers as a day-to-day supporting tool and a non-empirical way to establish acceptance criteria for thermal plan voiding. Prevent potential risks at design stage and, at the same time, make the product economically efficient by not oversizing it. The model is optimized in terms of trade-off between speed and accuracy and it is fully parameterized.

A Graphical User-Interface (GUI) was implemented using the Visual Basic (VBA) programming language. The interface allows the users configure the required model parameters - APDL scripts, in a convenient and secure way, and hiding from end-user all the finite element process and APDL complexity. The user is able to modify the PCB and component dimensions, number of copper layers and their thickness, number and dimensions of thermal vias, voiding level in solder interface, among others. The implemented solution is validated experimentally in a prototype phase. Furthermore, this cost effective tool, requires a minimum of learning effort by the user and provides simulation result in a short time.

The main goal of this project involves the quantification of the discontinuity level on the degradation of thermal efficiency. It is intended to establish acceptance criteria for solder interface discontinuity in terms of percentage of its nominal exposed pad area. Since the PCBs are designed based on intuition and experience of the engineer, and if the operation is deficient, design process is repeated with huge losses in cost and time. Thus, thermal performance validation based on thermal analysis software is essential and, desirably, and should take place before the production process.

A. Methodology of the Thermal Dissipation Tool

The developed tool is composed by a Mechanical APDL script, which makes the simulation process more transparent to the end-user, with mathematical model defined and conducted through the scripting language. Most components can be modeled in a simplified way, without affecting the usability of the simulation results. For example, using a two-resistors model (2-R), a four-resistors model, RC model (transient simulation), and a DELPHI model, etc. [17].

The created model comprises a regular QFN component, a solder interface and a PCB, with a structure that can be observed in Fig. 4 (a). The QFN component is in the center of a square PCB, and taking advantage of the symmetry model only a quarter of the model is simulated, making the simulation process faster. The model parameters are possible to be set through a Graphic User-Interface (GUI) that must produce a script file that defines an ARGS array of parameters and fills it with the values with a predefined sequence.

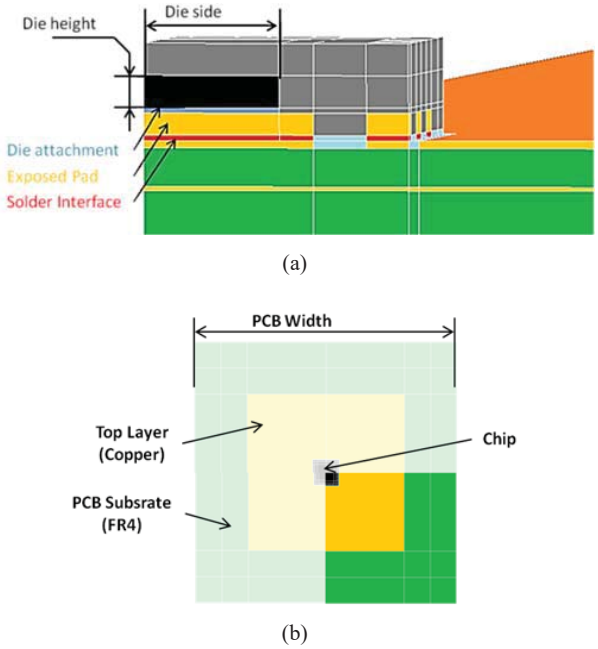


Fig. 4 (a) Detailed view of the geometric model and (b) top view of the model, with ¼ of model implemented (bottom)

The mathematical model and the respective simulation process are defined and controlled through a set of parameters grouped into five subsets. The largest subset consists of chip dimensions of PCB, quantities of thermal vias and copper layers, etc. The same subset also defines test conditions (ambient temperature, dissipated power, convection coefficients), which result in the simulation model boundary conditions. Parts of code can be enabled the construction of geometry model, the assignment of materials, the definition of density of finite element mesh and mesh creating. The properties of materials are also defined in a separate group of parameters.

The structure of the implemented APDL script, defines the mathematical model based on parameters provided by the user (Fig. 5). The script is capable to configure and invoke the Ansys solver and exports the results into a text file and PNG files - temperature gradient and heat flux of the model. The developed script can be seen as a sequence of delineated stages, each of these steps is implemented as a block of code with a type of actions. The model is parameterized and allows to vary different parameters, such as PCB and component dimensions, number of copper layers and their thickness,

number and dimensions of thermal vias, solder interface voiding level, among others.

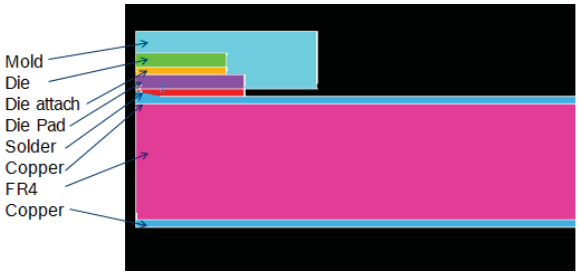


Fig. 5 Model defined in Mechanical APDL script

From the point of view of ANSYS simulation solver, the solid modeling option was adopted to create a finite element mesh – it means the creation of bodies and subsequent creation of mesh. Furthermore, The ANSYS preprocessor provides a wide variety of tools to create points, lines, areas, volumes and geometric shapes. And a variety of operations (extrude, Booleans, scale, move, copy, reflect) indispensable in the case of a complex geometry. The following approach was adopted: orthogonal parallelepipeds with total or partial overlap are created and "overlap" Boolean operation is applied in the end (for example, a parallelepiped which comprises the outer contour of the PCB and parallelepiped comprising an inner layer of copper).

```
!WHOLE PCB
    BLOCK,0,PCB_S/2,0+ELAY_H,PCB_H-ELAY_H,0,PCB_S/2
!LAYER BOTTOM
    BLOCK,0,L_BOT_S/2,0,ELAY_H,0,L_BOT_S/2
!Volume itself
    BLOCK,0,L_BOT_S/2,ELAY_H,PCB_H-
ELAY_H,0,PCB_S/2 !To cut PCB
    BLOCK,0,PCB_S/2,ELAY_H,PCB_H-
ELAY_H,0,L_BOT_S/2 !To cut PCB
!...
!Other blocks here
!...
ALLSEL,ALL
VOVLAP,ALL  !Overlap all Volumes
```

Fig. 6 Creation of orthogonal parallelepipeds of the model

The Fig. 6, shows the creation of the first four orthogonal parallelepipeds of the model and logical operation that overlap the geometry, resulting in a set of bodies (volumes) leading to a conformal mesh. It was decided to place model in the XZ plane with the "center of symmetry" in point (0,0) and considered one quarter of model positioned in directions "+X" and "+Z". It is also important to mention that while a parallelepiped was created - corresponding to bottom layer of copper, there were also created two parallelepipeds that "pass through" the printed circuit. Two types of elements were created to construct the finite element mesh, named EL_SOLID70 a linear element that has the ability of 3D heat conduction and EL_MESH200 an element type used to aid in the process of a finite element mesh creation through a sweep method. The geometry of the element SOLID70 has eight nodes with a single degree of freedom, with the temperature at each node. The element can be applied to steady-state or transient 3D thermal analysis.

Before associate a material type to a certain solid body (volume), it is necessary to create the materials used in the model by defining their respective properties. It is necessary to be able to reference certain line, area, volume or set of these, through a combination of commands, such as ALLSEL, VSEL, ASEL, LSEL, VSLA, ASLV, ASLL, ISLA, among others. Fig. 7, shows the assignment of material and element type to components that comprise thermal vias of the printed circuit, the FR4 substrate of printed circuit and exposed pad of electronic component. At the end of the listing can be seen the assignment of EL_MESH200 element type to INNER_SOURCE_AREA area.

```
CMSEL,S,WHOLE_VIAS,VOLU
VATT,VIAS_MAT,,EL_SOLID70
CMSEL,S,FR4_VOLU,VOLU
VATT,FR4_MAT,,EL_SOLID70
CMSEL,S,EPAD_VOLU,VOLU
VATT,EPAD_MAT,,EL_SOLID70
!...
!Other attributions here
!...
CMSEL,S,INNER_SOURCE_AREA,AREA
AATT,,,EL_MESH200
```

Fig. 7 Material and element type assignment

A technique to control the finite element mesh density consists in defining the quantity of finite elements along a certain line. The definition of the quantity of elements (parameter MESH_VIAS_S) along the lines that constitute the downside surfaces of thermal vias, modeled in simplified form as orthogonal parallelepipeds. The CMSEL command selects component WHOLE_VIAS previously created and which groups of the volumes correspond to thermal vias of printed circuit board. The ASLV command selects all the areas comprised by the previously selected volumes, while the command LSLA selects all lines comprised by the previously selected areas. The LSEL, R, LOC, Y, 0 command selects the set of previously selected lines (all lines of the component WHOLE_VIAS) those that belong to the bottom surface of the printed circuit board. Finally, the command LESIZE defines the quantity of elements for each selected line equal to MESH_VIAS_S.

After materials and element types are defined for all solids and density of finite element mesh. The area INNER_SOURCE_AREA is meshed that enables the mesh creation in the component INNER_PCB_WO_VIAS using sweep method. Then, mesher is configured to create a mapped mesh with hexahedral elements (commands MSHAPE and MSHKEY). After creating the mesh with hexahedral elements for all solids, the *mesher* is configured to create tetrahedral elements on the remaining solids.

The physical model can be described as follows: heat is generated inside electronic component (*Joule effect losses*) and it is transferred to the environment through dissipation

paths, present a certain thermal resistance that results in a temperature increase. In the designed simulation model the transfer of heat by conduction in solids and by convection from the top and bottom of the PCB towards the environment is considered. A heat generation rate [W/m^3] is applied to silicon die and convection coefficients and room temperature are defined on the top and bottom sides of the PCB. Post-processing steps consists of the extraction of results to be sent to GUI (written to the file results.txt), with the temperatures of the nodes located at the point which for used border conditions must contain the highest temperature.

B. Graphic User Interface (GUI)

Fig. 8 presents a snapshot of the graphical user interface (GUI) developed in Visual Basic for Applications (VBA). To hide from the end-user, all the complexity of APDL script and to make the introduction of model parameters more user-friendly and secure (disallow introduction of parameters that are not valid), as well as to facilitate the extraction of final results. The resulting tool is invoked from a Microsoft Excel file, which simultaneously serves as a storage of simulation results, and which can be extended by the end-user with the intended data processing features (graphics, mathematical operations, etc.), since this is commonly used by engineers in their day-to-day tool.

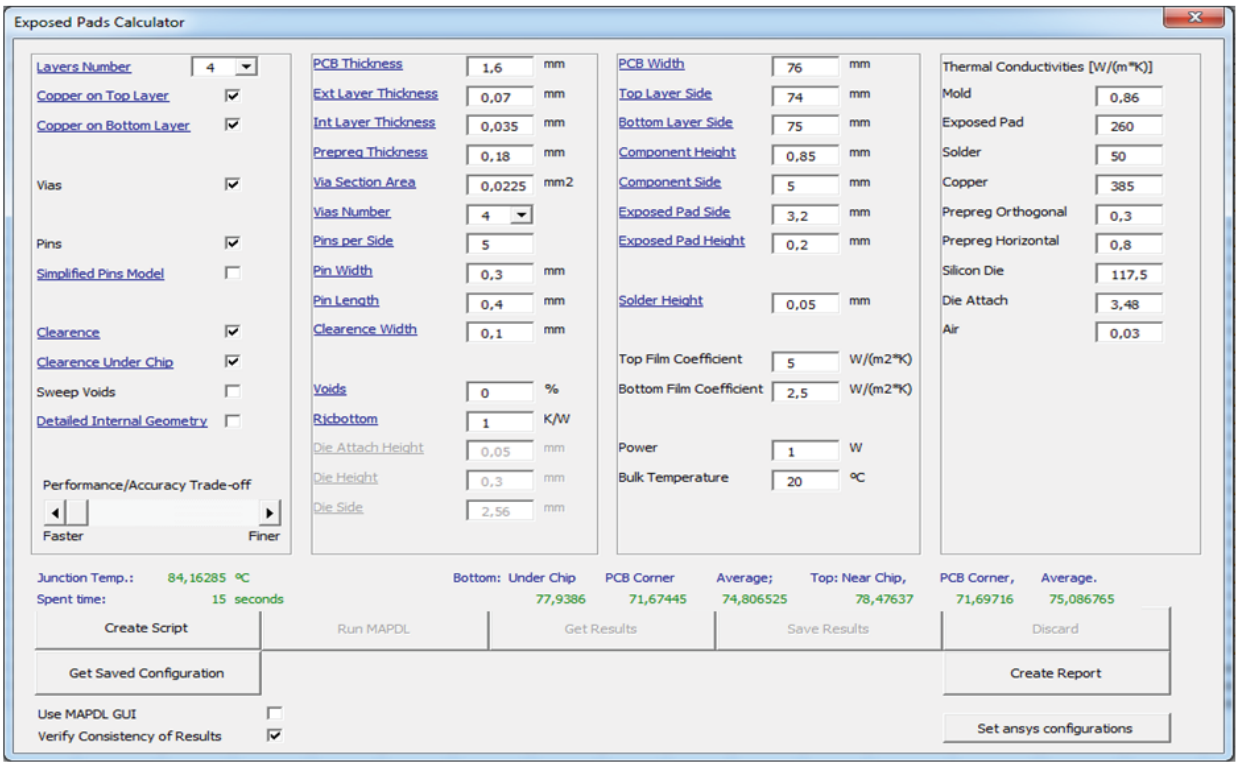


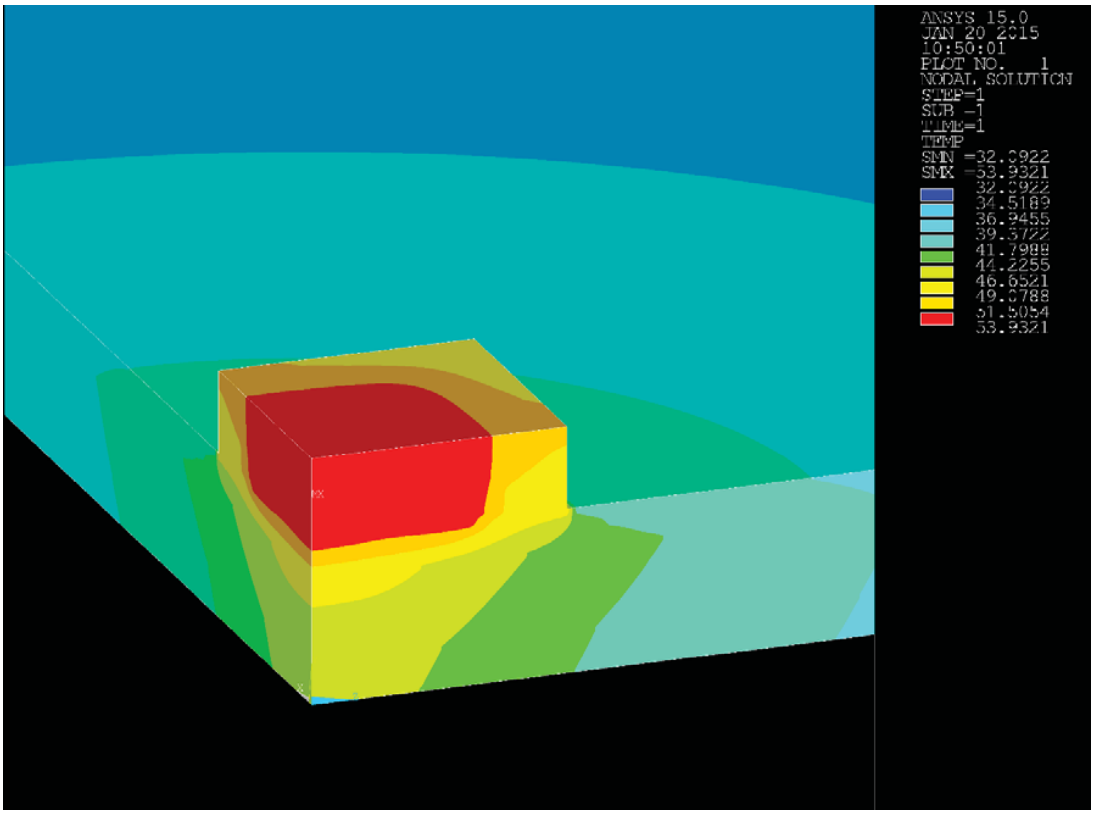
Fig. 8 User-friendly interface in *Visual Basic for Applications*

C. Tool Organization and Interface Features

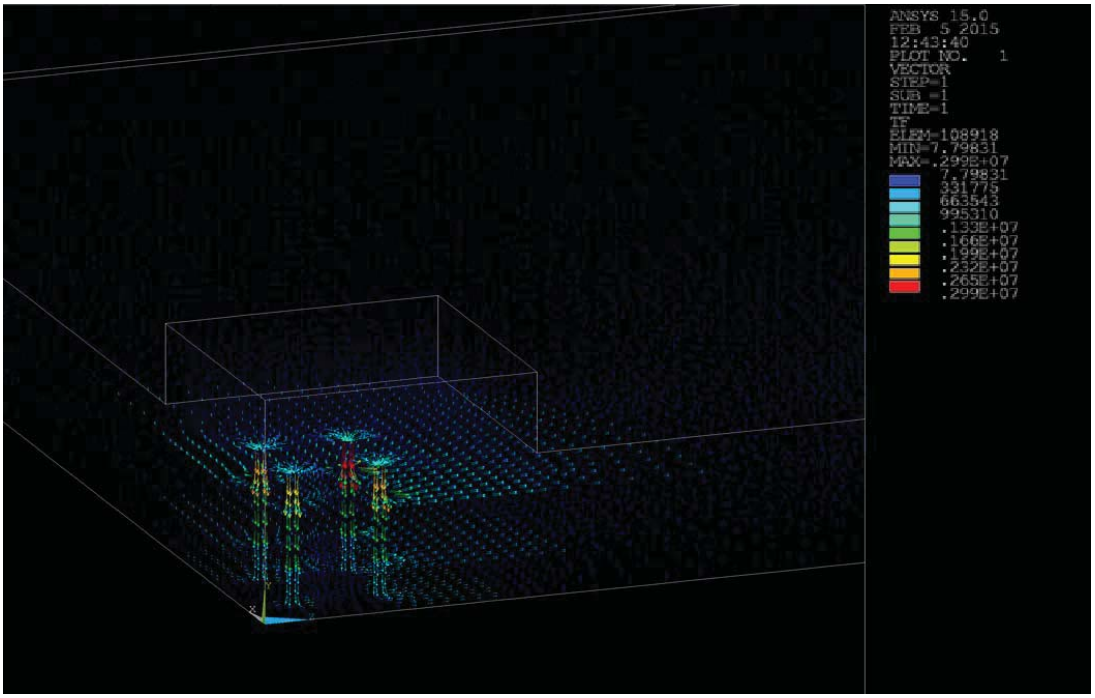
The simulation tool is composed by a "EPadCalculator.xlsm" file and “MAPDL_files” folder that has the supporting files (such as scripts, libraries, input/output files) structured as follows: mystart.mac -contains the main MAPDL program, maclib.txt -contains a library of special macros used by the mystart.mac, parm. parm -implements the interface from Excel to MAPDL, defining ARGS array and the results.txt -implements interface from MAPDL to Excel containing the current results. After performing the simulation and saving of respective results, the folder will also contain a "plot_files" folder that contains the images acquired during post-process phase of MAPDL script. These images are used in automatic creation of reports, for this action the simulation results must be saved and a report created. The reports, when required, will be stored in the "report_files" folder that is automatically created in the same directory as the folder "plot_files". The report is produced as Microsoft Word document that contains configuration information, extracted results, comments made by the user and images that represent resulting thermal gradient and thermal flux (Fig. 9).

The "EPadCalcutor.xlsm" file has calculation sheets that cannot be edited manually: *Results* spreadsheet contains the saved simulation results. The *SweepVoids* spreadsheet is used by the program, which containing graphics of the junction-to-ambient thermal resistance of the package (IC) as a function of the relative void area. The developed tool also includes a spreadsheet named "ConvectionHeatTransfer" that implements the calculation of convection coefficients, through

the Elisson's model correlation and applied on the upper and lower PCB surface.



(a)



(b)

Fig. 9 Output results from simulation report: (a) temperature gradient and (b) heat flux between the IC/PCB

After configure the input parameters at GUI. The initial step consists of the creation of script by pressing "Create Script" to edit the "parm.parm" file inside "MAPDL_files" folder. After clicking on "Create Script" button it becomes impossible to edit model parameters and becomes possible to click on "Run MAPDL" or "Discard" button. In this way, the user is able to check model parameters once more, before invoke MAPDL program or discard current configuration. At the end of the simulation, the user should press "Get Results" button to refresh and show the informative line (Fig. 8). After reviewing informative line, the user must make the decision whether to keep or discard the obtained results and respective parameters set. If the user chooses to save the results, will be prompted to enter a comment that will be saved in "Results" spreadsheet and also presented in the final part of the automatically generated report.

D. Experimental Set-Up for Tool Validation

Through the characterization and qualification, the manufacturers of components are able to understand the limitations of the component's performance and provide guidance to the user with the operating specifications, thus the junction temperature is the specification for maximum operation. Experimentally there are three methods to measure the thermal parameters in a die (IC). The most reliable method is measure the junction temperature directly in the IC, displaying the temperature during operation using a thermal test chip (TTC-1002, from TEA) [18].

The experimental tests were performed using a TSP (temperature-sensitive parameter) element as a direct measure of the temperature semiconductor, which is located at the die center. Simultaneously, the thermal test chip allows control the dissipated power by the use of two power resistors (7.6Ω±10%) located near the center of the TSP. The assembled QFN test-device is composed by a TTC-1002 and a QFN open cavity (M-QFN20.65 from Mirrorsemi), attached with thermal glue (CW2000 - nickel conductive pen). Connecting the QFN pads and TTC-1002 die pads with AlSi-1% bond-wires of 30 µm diameter - with a fusing limit of 400 mA [19]-[21]. The QFNs test-devices were solder in three different PCBs, each with a relative area of voids induced in solder interface, namely 10%, 40% and 70% of the exposed pad area. Fig. 11, shows the PCB test-board and the test enclosure according to JESD51-3 and JESD51-2A [20], [22] used in experimental measurements of junction temperature (T_J). As a basic configuration will be considered low effective thermal conductivity board with thermal vias, described in JESD51 Guidelines.

The electrical method for semiconductor thermal measurements relies on the ability to measure the TSP of the device-under-test (DUT). Since the junction temperature (T_J), starts decreasing immediately at the exact cessation of applied power. Using diodes as TSP elements, which make excellent temperature sensors at low values of forward current (I_M), with the junction forward voltage [V_F] correlation is very nearly linear to the second order. Thus a change in junction temperature produces a corresponding change in junction forward voltage obtained by:

$$\Delta T_J = K.\Delta V_F \quad (5)$$

where, the correlation factor (K) is highly dependent on the value chosen for I_M. The units of K are in °C/mV and the value is typically in the range of 0.4 to 0.8°C/mV [13], [14]. Choosing a too low I_M value will cause problems in measurement repeatability for a specific diode and potentially large variations between devices. On other hand, too large values of I_M will cause significant self-heating within the diode junction area and give rise to potentially large temperature measurement errors. The diode forward voltage is read and recorded once the environment temperature has stabilized, which occurs when neither the diode voltage nor-environmental temperature measurements shows any significant fluctuations. A Memmert UN55 oven was used to obtain correction factors in p-n junction of TSP element between room temperature and 100°C using a constant temperature. Once the PCB test-board with QFN test-device diodes are mounted into the temperature–controlled environment (enclosure), and connected to the measurement system.

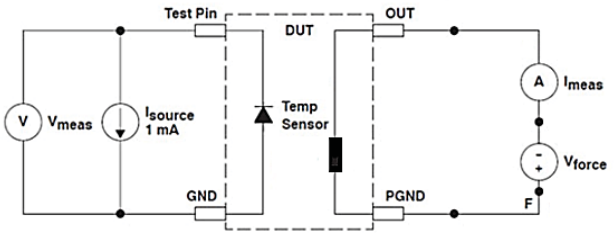


Fig. 10 Schematic diagram for T_j measurements

The diode acts as a temperature sensor when monitoring the voltage drop across the p-n junction ($\boldsymbol{v}$) when considering a direct polarized with a saturation current ($\boldsymbol{i_0}$), as shown in the above scheme. Through the Shockley equation determines the diode current as a function of temperature [23]:

$$i = i_0\left(e^{\frac{v}{nV_t}} - 1\right) \; with \; V_t = k_b/qt \quad (6)$$

with V_t the thermal voltage having a typical value of 25.85 mV at room temperature, which varies depending on the temperature (t) of the p-n junction with k_b Boltzmann's constant, and (q) the elementary charge of electron and (n) the emissivity coefficient - depends on the manufacturing process and the semiconductor material (typically n = 1). However, it is necessary to make a correction in the junction due to temperature effect (JEDEC / SEMI Guidelines) by performing the following procedure:

- Calibrate the temperature of the diode (parameter) in a temperature controllable environment, enabling the fixing and wiring, and is considered i_M = constant for performing calibration;

- Using a voltimeter for measuring (v) and a thermo-coupler for measuring T_m.

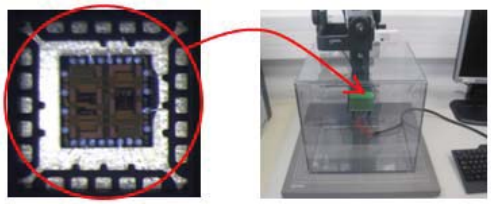


Fig. 11 QFN cavity with a Thermal Test Chip (TTC-1002) and PCB test board in a controlled environment-still air (enclosure)

Also measuring the temperature at the package (case) surface allows estimate the junction temperature during operation. In this context, the temperature in the case can be measured using an infrared camera (IR) Gobi-384, depending on the accuracy required. When the component is measured at the top, the junction temperature can be calculated using (7) [13]:

$$T_J = T_C + \Psi_{JT} * P_{diss} \quad (7)$$

where, T_j and T_c is the junction temperature and the top center temperature on the package. With Ψ_{JT} a specific value for each component (IC) with a heat transfer profile provided by the manufacturer.

III. Results and Discussion

After tool implementation was completed, it was submitted to a set of functional tests to validate the numeric tool. A part of these tests consisted in an attempt of applying tool to a practical case - reproducing the experimental conditions, using a QFN20-5x5mm test-device in order to evaluate the impact of voiding level between an IC and PCB in thermal dissipation.

A. Compare Experimental and Numerical Results

As show in Fig. 11, the measurements were performed in an enclosure with nominal dimension of 305 x 305 x 305 mm. All seams thoroughly sealed to ensure no airflow through the enclosure and shelf constructed of low conductivity material. The enclosure material is a low conductivity material (polycarbonate - 0.11 W/mK). The package is positioned in the geometric center of the chamber by adjusting the position of the support structure constructed also in a low thermal conductivity material (less than 0.5 W/m K). With the purpose to replicate the experimental tests in the simulation tool, as well as make comments on relevant statements, based on the knowledge and experience acquired during the state of the art analysis phase.

The solder interface area can be controlled using a solder mask layer over copper layer of exposed pad: 3.25 x 3.25 mm in the PCB. After the solder process, an x-ray inspection was performed to all test-boards in order to verify if the induced percentage of voids is correct. The real percentage of voids obtained after the welding process is 17,6%, 51,5% and 75,8% for each PCB, and taken into account in simulation process.

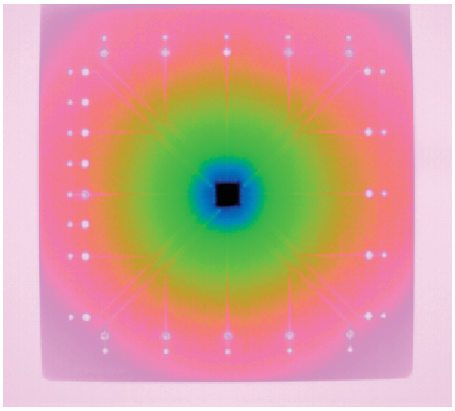


Fig. 12 Thermal measurement performed by infra-red thermal camera (Gobi-384) on the PCB (10% of voids) surface during T_J for a dissipated power of 1,5W

Choosing a low I_M value won't cause significant self-heating within the diode junction area and reducing potentially large temperature measurement errors. The forward current applied to the TTC-1002 diodes was 1 mA. Thermal diode temperature measurements are based on the change of forward-bias voltage of the diode when operated at two different currents. Δv is proportional to an absolute temperature based on the following formula. This difference in Δv of the diode at two different forward currents varies with temperature and can provide a base for the on-die temperature only while the diode is operating within its linear region. A p-n junction has an inherent temperature dependency described by (8) [23].

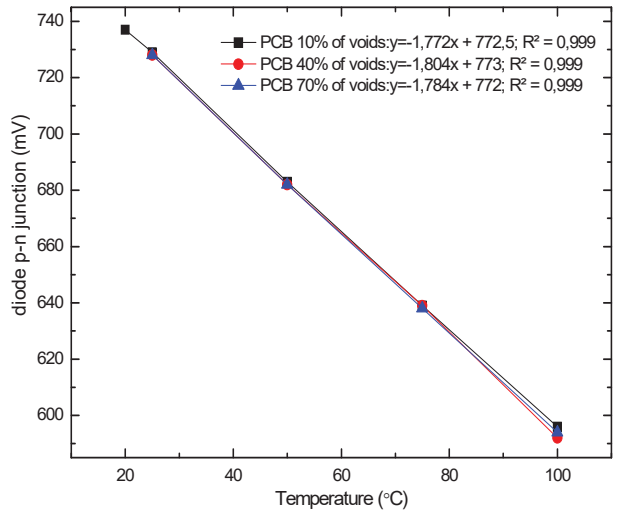
$$v = \frac{k_b T_J}{q} \ln\left(\frac{I_M}{I_s}\right) \quad (8)$$

$$T_J = m.v + T_0 \quad (9)$$

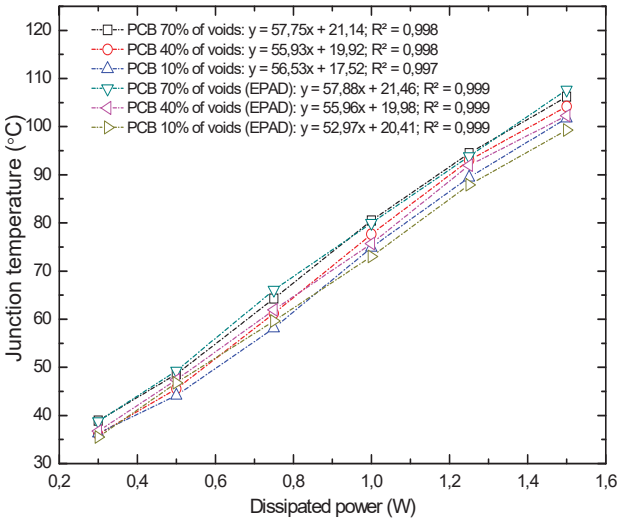
where, m is the slope equation of junction temperature as function the diode forward-voltage (v) obtained by (8). Measurements are performed when neither the diode voltage nor-environmental temperature measurements show any significant fluctuations. The average value and standard deviation of the K values from a group of the same samples provides a measure of sample uniformity.

High linearity between the temperatures applied to QFN test device and the diode p-n junction temperature for both PCBs can be observed in Fig. 13 (a), with an associated correction factor of 0.56 °C/mV.

A small difference between the experimental and numerical results is obtained by the "Exposed Pad Calculator", as shown in Fig. 13 (b). Comparing different levels of power dissipated in the IC and for PCBs with different exposed pad area - depends on the percentage of solder interface under QFN test-device. The offset value obtained for each PCB is related with the voiding level in solder interface, increasing the junction temperature as the area of voids increases. However, small differences were detected between a PCB with 17,6% and other with 75,8% of voids in solder interface.



(a)



(b)

Fig. 13 (a) Correction factor obtained in p-n junction of QFN devices, submitted to temperature between 25ºC and 100ºC and (b) junction temperature of the test-devices and obtained by the "Exposed Pad Calculator" as a function of the dissipated power

B. Thermal Efficiency Due to PCB Design/Layout

To evaluate the impact of PCB layout parameters and voids presence in solder interface, a parametric study was performed. The numerical simulation input parameters are presented on the configuration interface, Fig. 8. It was considered a QFN20-5x5x0.85 mm component with an exposed pad of 3.2x3.2x0.85 mm. The PCB has a thickness of 1.6 mm, with four copper layers and 76mm wide. For the study, a thermal resistance $R_{JC\text{-}Bottom}$ = 1ºK/W was considered and a power dissipation equal to 1W. No voids were considered in the PCB with a solder interface height equal to 0.05 mm in a temperature environment of 20°C.

With the increasing number of thermal vias, the dissipation path is optimized through the exposed pad into the PCB, leading to a decrease in the junction-to-air temperature and package surface. As shown in Fig. 14 (a), there is a reduction of 50% in junction temperature between a case with a PCB of two copper layers and 4 thermal vias under exposed pad and a PCB with eight copper layers and 64 thermal vias.

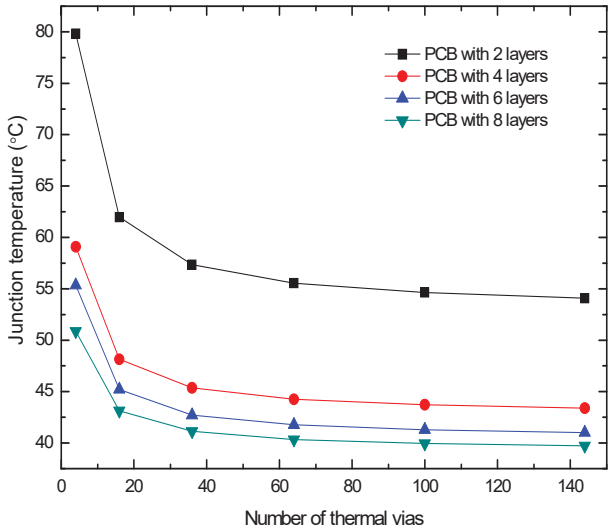
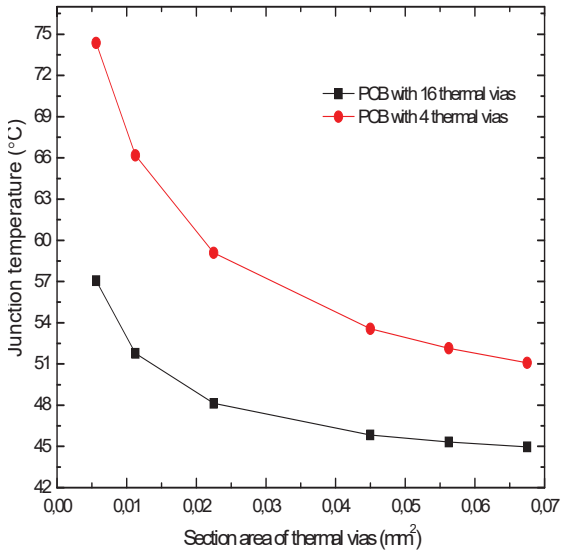
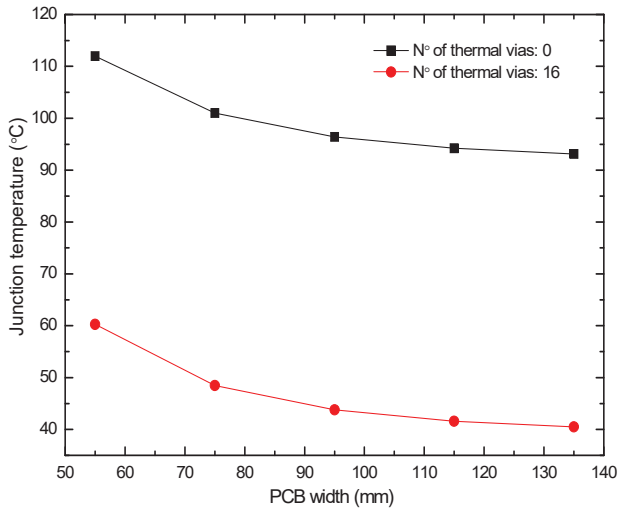


Fig. 14 Junction temperature (T_J) as a function of thermal vias number for different PCBs and b) computational time needed to obtain T_J for each PCB depending on geometric complexity

After checking the dependence on temperature (T_J) with the number of thermal vias, these analyses are focuses on the assessment of thermal efficiency as a function of the sectional area of thermal vias and PCB width, Fig. 15 (a).



(a)



(b)

Fig. 15 (a) Junction temperature (T_J) depends with the section area of thermal vias and (b) the influence of the PCB width in junction temperature

For a PCB with four layers and 4 thermal vias it is possible optimize the thermal efficiency in 32% by increasing the sectional area from 0.006 to 0.067, Fig. 15 (a). Compared with a PCB with 16 thermal vias the maximum optimization is around 20%. Fig. 15 (b) shows the impact of PCB width on thermal efficiency, where is possible to observe that number of thermal vias underneath the exposed pad has more impact in junction temperature than the increase of a square PCB between 55 mm to 135 mm.

Fig. 16 shows the temperature obtained in different locations of a PCB with 4 thermal vias as a function of the number of PCB copper layers on the PCB. Considering the numerical results for PCB with two and eight copper layers, the thermal optimization is approximately 28°C and thermal difference (~19°C) between 2 to 4 layers. It has also been determined the temperature at the top and bottom of the PCB - underneath the package. The bottom side of the PCB obtains the lower temperature compared to the upper side of PCB and underneath exposed pad. Increasing the number of layers, the temperature difference will increase due to convection phenomenon.

The computational time required to determine the junction temperature for different PCBs is presented in Fig. 17 - dependence with number of copper layers. The increased computational effort is due to complexity of the geometry and processing (for 2 up to 8 layers) required over 56 seconds determining the junction-to-air temperature. The machine that performed the simulations (i5-3320M / 8GB RAM / OS WIN7-64bits) needed only 68 seconds to determine T_J for a PCB with 8 layers.

C. Thermal Impact Due to Voids in Solder Interface

The aim of this work is evaluate the impact of voids in the solder interface. Thus, using numerical simulation tool to perform a junction temperature analysis for different areas of voids in solder interface - namely 0, 25, 36, 49, 64, 81% of area under the exposed pad by selecting the "void sweep" functionality.

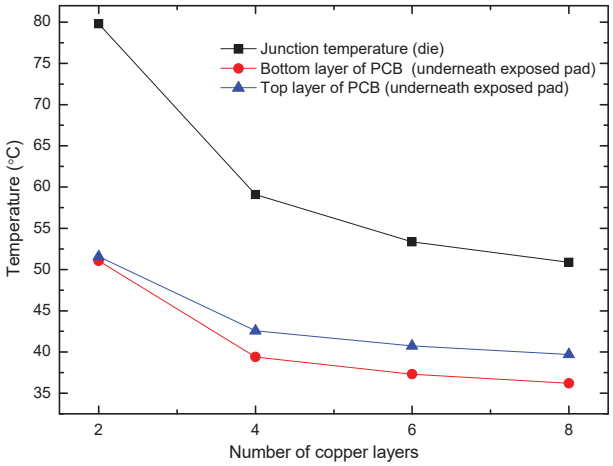


Fig. 16 temperature on different locations as a function of PCB copper layers' number

As can be observed in the Fig. 18 (a), the impact of voids phenomenon that occurs during the solder process can be minimized by adopting thermal vias. Using a PCB with 16-thermal vias occur a thermal optimization of 18% and with 36-thermal vias the improvement is approximately 24% compared with PCB with 4-thermal vias. Shown a temperature increase of 3ºC when the percentage of voids reaches 81% of the area. Additionally, Fig. 18 (b) shows that void phenomenon has significant effect for areas greater than 90%. Thus, one should beware these limits and considering the importance of the thermal paths and the number of thermal vias and PCB copper layers, according to the PCB developer needs.

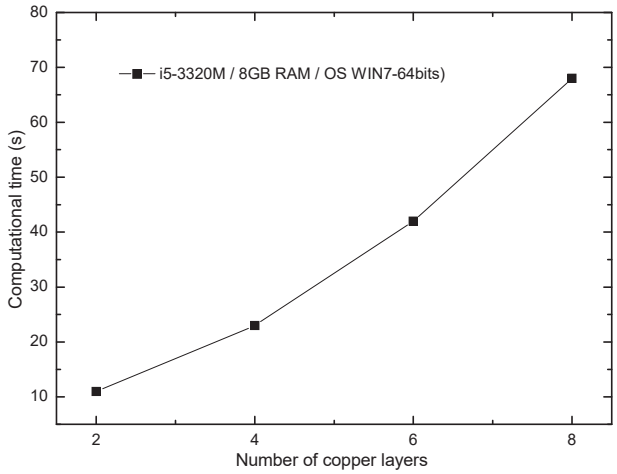
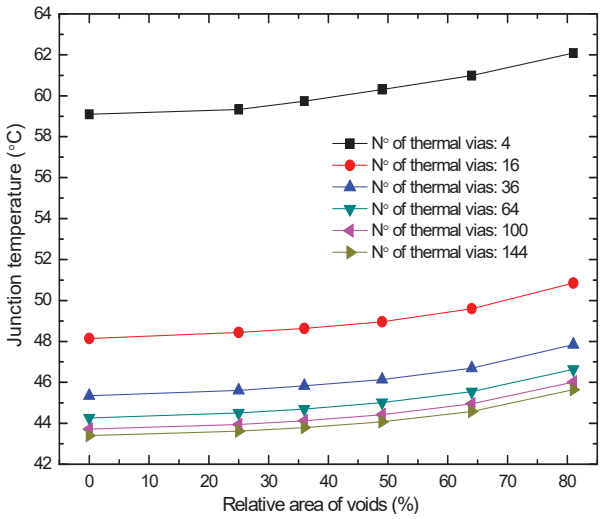
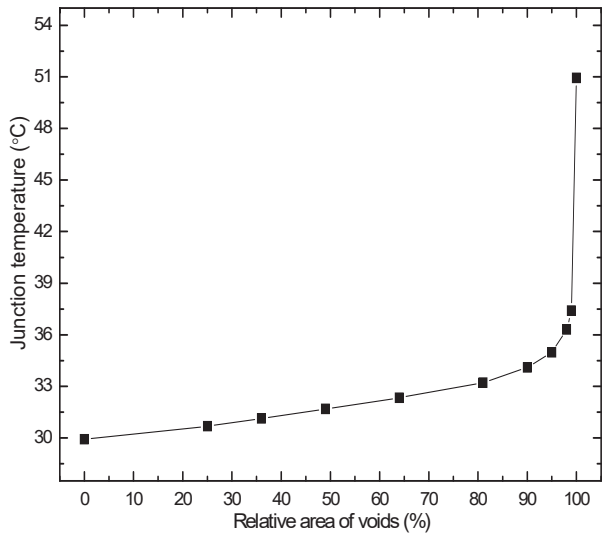


Fig. 17 Computational time needed to determine the junction temperature (T_J) for PCBs with different layers



(a)



(b)

Fig. 18 (a) Junction temperature (T_J) behavior with relative area of voids in solder interface, considering cases with different thermal vias in the exposed pad area and (b) identified a critical behavior for a case study

IV. Conclusion

The developed numerical analysis tool, called "Exposed Pad Calculator" is completed in terms of functionalities and experimentally validated, according to the JEDEC Standards. Quick and easy to use, this tool allows evaluate the ICs thermal efficiency (e.g. QFN Packages.) and provide more information than that found in documents currently used to establish the acceptance voiding level. So it can be useful to be adopted by PCBs developers as a day-to-day tool. Additionally, considers the PCB design options in the dissipation process, allowing us to evaluate and/or predict the factors with higher impact in thermal optimization of ICs.

Acknowledgment

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