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The Methodology of Flip Chip Using Astro Place and Route Tool

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***Abstract*—**This paper will discuss flip chip methodology, in which I/O pads, standard cells, macros and bump cells array are placed in the floorplan, then routed using Astro place and route tool. Final DRC and LVS checking is done using Calibre verification tool. The design vehicle to run this methodology is an OpenRISC design targeted to Silterra 0.18 micrometer technology with 6 metal layers for routing. Astro has extensive support for flip chip placement and routing. Astro tool commands for flip chip are straightforward approach like the conventional standard wire bond packaging. However since we do not have flip chip commands in our Astro tool, no LEF file for bump cell and no LEF file for flip chip I/O pad, we create our own methodology to prepare for future flip chip tapeout.

***Keywords*—**Astro, bump cell, Calibre, flip chip, LEF, methodology, SCHEME, TCL.

I. Introduction

FLIP chip, also known as controlled collapse chip connection, is a method of direct connection of a flipped electrical component onto a substrate, carrier, or circuit board by means of conductive bumps instead of the conventional wire bond. In a wire bond connection, wires are connected between the package and the I/O pads, which are located in the peripheral region outside the core area. In the flip chip methodology, bumps cells are placed in the core area since the chip is no longer limited to bond wires. For this reason the placing of the bumps is sometimes called "Area I/O" [1].

II. Flip Chip Background

Flip-chip refers to semiconductors that are mounted with the active side down [2]. Flip chip interconnection was used as early as the 1960's for IBM mainframes, and as early as the 1970's for automotive electronics. Today flip chip packaging may be found in cell phones, pagers, watches, and other devices where space is critical. While only a small fraction of wafers produced today are bumped for flip chip assembly that number is growing due to flip chip's advantage in size, performance, and the growing availability of flip chip materials and services [1].

The elimination of bond wires reduces the amount of board area needed, thus allows the overall size of the chip to be smaller. However, the disadvantage is that it cannot be replaced easily if there is a problem. Another disadvantage is heat. Heat becomes a major issue because the points soldered together are quite stiff. If the chip expands due to heat, the corresponding connectors also need to be designed to thermally expand to the same degree otherwise the connections between them will break [3].

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A. Flip Chip Process

To summarize the flip chip process, first integrated circuits are created on the wafer. Then pads are metalized on the surface of the chips. Before those chips are cut, solder dots are deposited on each of the pads. Chips are flipped and positioned so that the solder balls are facing the connectors on the external circuitry. Solder balls are then re-melted (typically using hot air reflow).Finally; the mounted chip is "underfilled" using an electrically-insulating adhesive [4]. Fig. 1 shows the image of a conventional wire bond chip and a flip chip.

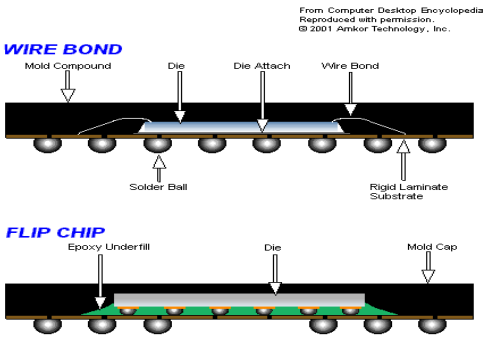

Fig. 1 The difference between wire bond chip and flip chip

III. The Methodology

In Astro, the methodology will start with a design netlist, timing and technology files. We will also need a LEF file containing the definitions for the bump cell and I/O pad. In the LEF 5.6 standard, bumps can be square or polygonal for more accurate area. Below is an example of a square bump cell definition in LEF.

```
VERSION 5.6 ;
MACRO BUMPCELL
        CLASS COVER BUMP ;
  ORIGIN 0 0 ;
  SIZE 5 BY 5  ;
  SYMMETRY X Y R90;
  PIN BUMP
  DIRECTION INOUT ;
    USE SIGNAL ;
```

```
        PORT
          CLASS CORE  ;
                LAYER METAL 6  ;
      RECT 0.0 0.0 5.0 5.0  ;
      END
          END BUMP
END BUMPCELL
```

Once placed on Astro place and route tool, the bump appears as a square as define in the LEF file.

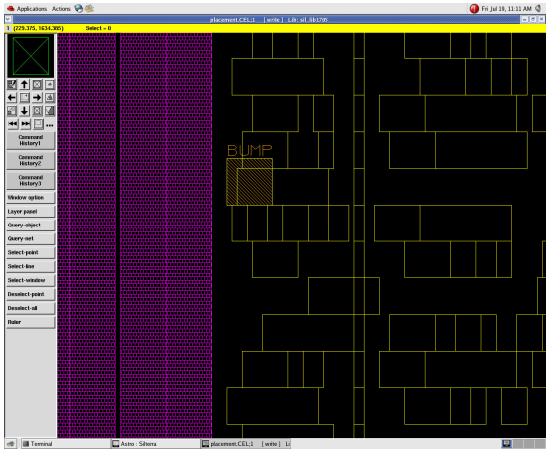

Fig. 2 A square bump cell placed in Astro

Fig. 2 shows bump cells array overlaying placed standard cells in the core area.

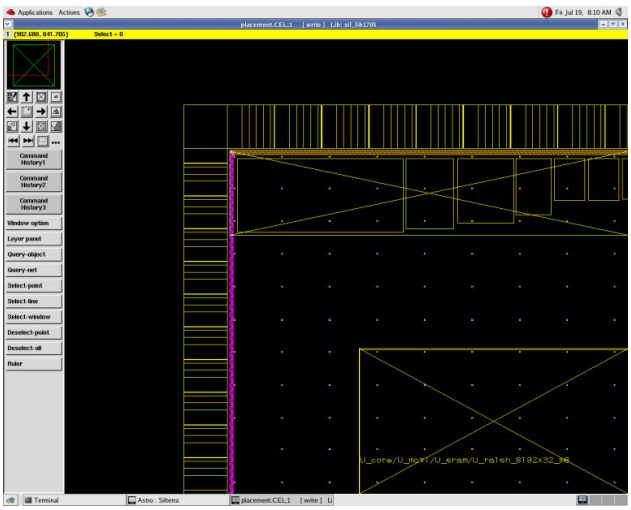

Fig. 3 An array of bump cells placed on core area

A. Steps to Run the Methodology in Astro and Calibre

1) Create LEF for bump cell and flip chip I/O pad. Note: flip chip I/O pad is modified from wire bonding I/O pad.
2) Convert bump LEF and flip chip I/O pad LEF to milkyway (Astro netlist format).
3) Create design library in Astro by reading in verilog netlist, standard cells milkyway, macros milkyway, I/O pads milkyway and bump cell milkyway.
4) Read in timing files.
5) Create floorplan with power rings and place I/O pads along with pad filler cells (refer to Fig. 4).

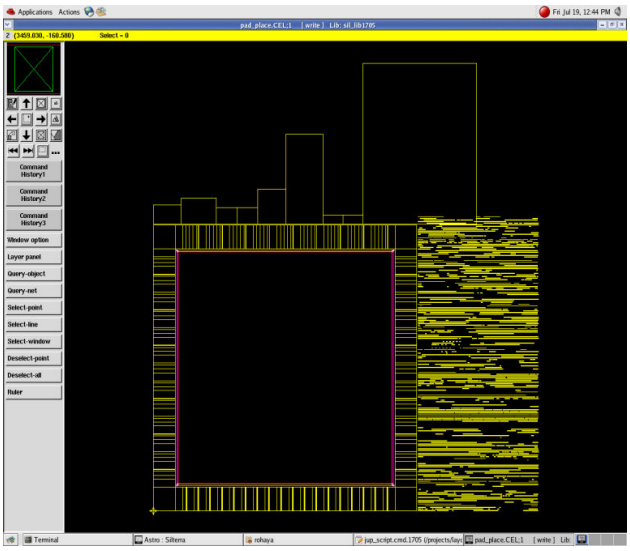

Fig. 4 Floorplan of the design

6) Place macros, bump cells array and finally standard cells on the core area. Bump cells array are created using TCL programming language.
7) Perform power routing on I/O pads, macros and standard cells.
8) Perform power network synthesis to calculate power consumption and check for any hot spots due to voltage drop.
9) Route bump nets and fix DRC.
10) Perform clock tree synthesis.
11) Route critical signal net first (clock).
12) Route the rest of the signal nets then check for DRC and LVS.
13) Fix all DRC and LVS errors.
14) Check antenna problem and fix them by inserting Antenna Diode.
15) Insert filler cells. Refer to Fig. 5 for final stage of placement and routing before exporting GDS2. Also refer to Fig. 6 for close-up look on how a bump cell is connected.

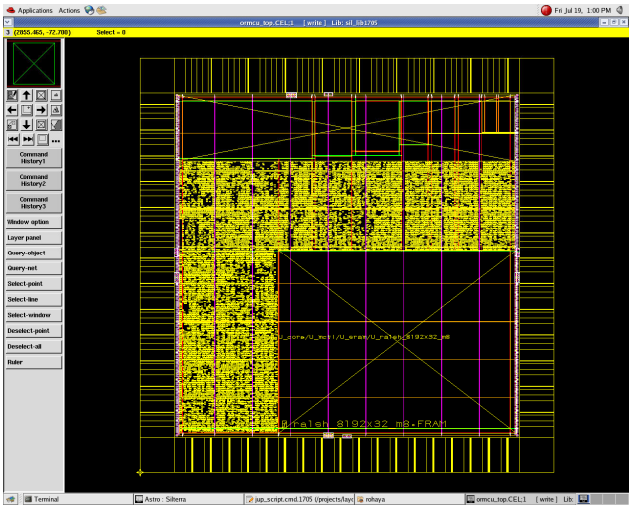

Fig. 5 Fully routed design with clean DRC and LVS

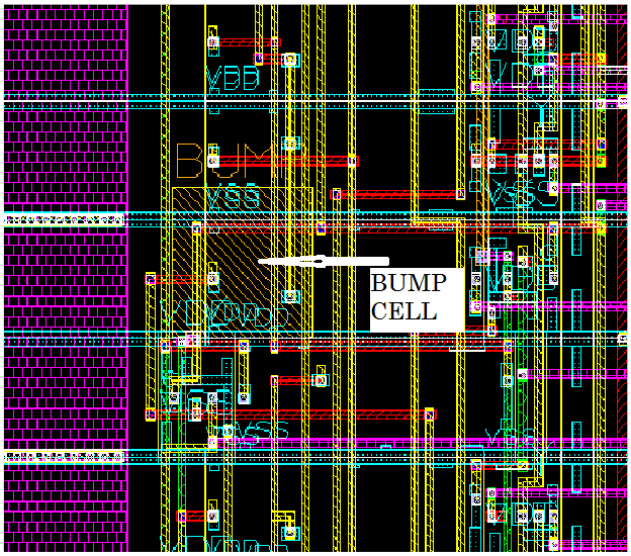

Fig. 6 Routed bump cell

16) Export GDS2 and verilog netlist.
17) Stream in GDS2 in Virtuoso Layout Editor.
18) Modify I/O pad so that it has no bonding pad to cater for flip chip methodology as in Fig. 7.

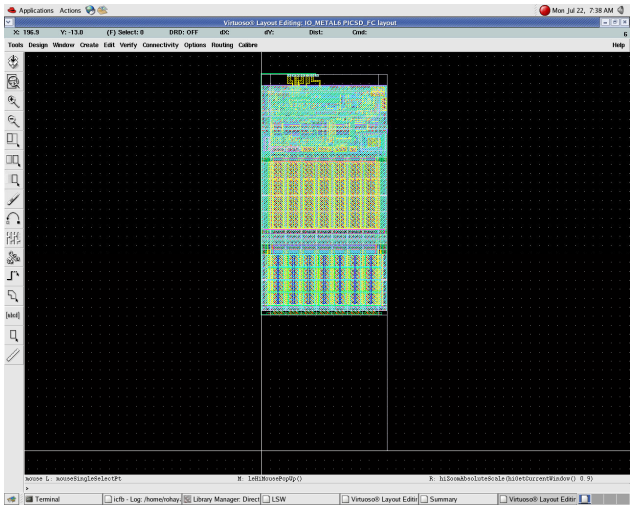

Fig. 7 Flip chip I/O pad (without bonding pad)

19) Stream in I/O pad, standard cells, macros, bump cell and filler cells.
20) Check for DRC and LVS using Calibre verification tool (refer to Fig. 8).

B. Flowchart

All the commands are executed using SCHEME programming language which is available in Astro. Only bump array is created using TCL language and read in Astro in TCL.

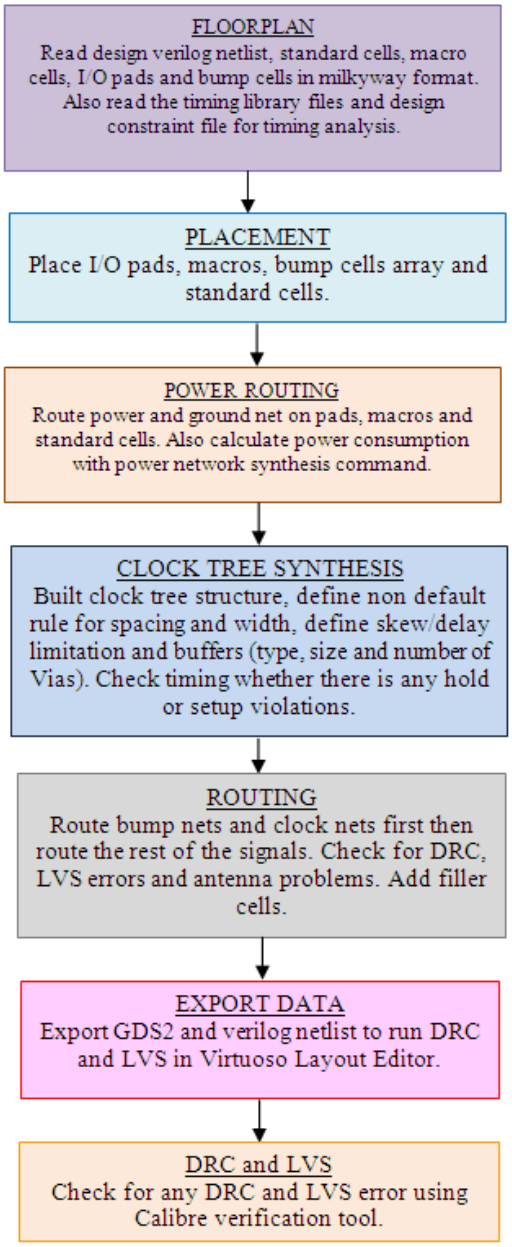

Fig. 8 Flowchart that shows the methodology of flip chip

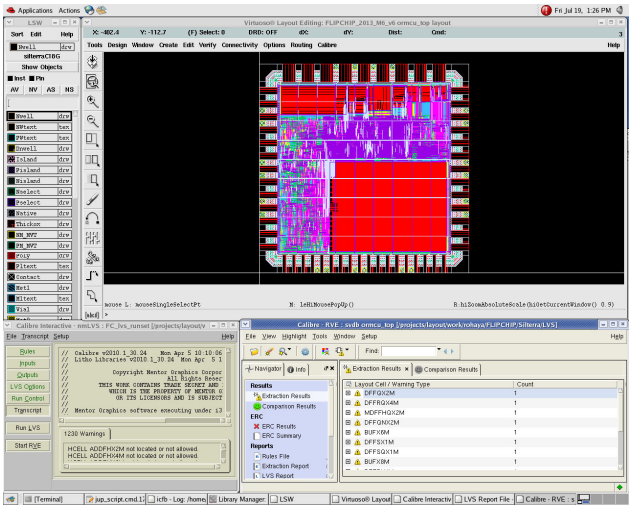

Fig. 9 Result shows the design had passed LVS

IV. Conclusions

Using the above methodology, it is possible to do a flip chip design with Astro as the place and route tool without having LEF for the bump cell and without having LEF for the flip chip I/O pads. We also do not have Astro commands for the flip chip. Our goal is to prepare for flip chip tape out in the future. For future project, the foundry will supply LEF file for both bump cell and I/O pads. We will run the script that had been created in this research.

Acknowledgment

We wish to compliment all the engineers in Mask layout group who involved in this research project.

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[1] Kevin Kelley, "Alternative Flip Chip Methodologies in First Encounter", Cadence Design Systems.
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Rohaya Abdul Wahab received her first degree in Electrical Engineering in 1989 from Cleveland State University, Ohio, USA. Currently, she is a senior engineer at the Department of Integrated Circuit Development, MIMOS Berhad. Her research interests include the methodology of back end flow for both digital and analog designs. She is a member of the Institute of Engineering Malaysia and had been working in MIMOS Berhad since 1992.