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The Impact of Process Parameters on the Output Characteristics of an LDMOS Device

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***Abstract*—**In this paper, we have examined the effect of process parameter variation on the electrical characteristics of an LDMOS device. The rate of change in the electrical parameters such as cut off frequency, breakdown voltage and drain saturation current as a function of the process parameters is investigated.

***Keywords*—**LDMOS, Process Parameters, electrical characteristics, parameter variation.

I. Introduction

THE high voltage laterally diffused MOS (LDMOS) transistor was introduced in 1972[1]. The fabrication process of the LDMOS device is compatible with that of CMOS process. This gives the possibility to combine the power transistor with the low voltage logic on the same chip and provide a low cost fabrication process. Furthermore, the use of silicon makes the process significantly cheaper than the gallium arsenide devices.

The graded short channel of LDMOS, called P-Base, improves the linearity and high frequency response. It increases the electric field in the channel such that the electrons reach their saturation velocity earlier. Other advantages of the P-Base region include the prevention of the punch through and improvement of the device transconductance [2].

The low doped long region, called N-Drift, improves the breakdown voltage and high power performance of the device. However, at the same time the drift region degrades the RF performance. This is due to the increased on-state resistance.

In this paper we discuss the impact of process parameter variations on the electrical characteristics of the device. The device fabrication steps are provided in the second section of this paper. Section III is devoted to a detailed explanation of the underlying physics. It is shown that the simulation results confirm the physics governing the device. Finally a conclusion is drawn in section IV.

II. Device Fabrication

Fig. 1 shows a cross-sectional view of the simulated LDMOS. Fabrication process starts by growing a p-type epitaxial layer (N_A=7×10^{14} cm^{-3}) over a p$^+$ substrate. It is then implanted with phosphorus (N_D=1×10^{12} cm^{-2}) to produce the n-type drift region. Field oxide, required for the high voltage application is then grown to a thickness of 600 nm.

The remaining process steps of the gate-oxide growth and poly-silicon gate deposition with doping of 1×10^{19}cm^{-3} are similar to those in the conventional CMOS process flow. The poly silicon gate extends over the 65nm thick gate oxide and terminates on the field oxide. The short channel is created by the lateral diffusion of boron implantation [1]. The source/drain region implantation is finally performed. The appropriate anneal times and temperatures were chosen to achieve the desired profiles.

A 9µm height trenched-sinker is also employed in this structure. The sinker is widely used for lateral power devices to decrease the number of contacts to only two, i.e. the drain and the gate contacts, making the LDMOS integration easier. Furthermore, by eliminating the extra surface bond wires, the bulk–source connection reduces the source inductance and thus improves the RF performance [3], [2].

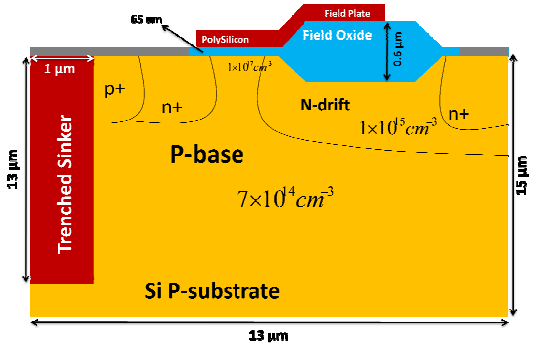

Fig. 1 Cross section of the simulated LDMOS

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III. Simulation Results And Discussions

In the following simulations all the parameters and annealing times and temperatures are kept constant and only the parameter of interest is varied.

A. N-Drift Implantation Dose

The constant doping contours shown in Fig. 2 imply the progression of depletion layer edge in the P-Base region.

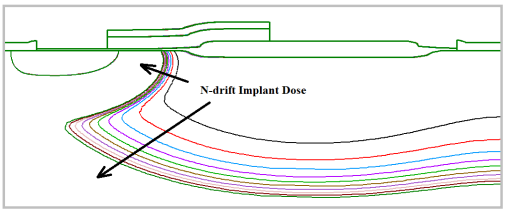

Fig. 2 Progression of depletion layer edge in the P-Base region shown by the constant doping contours

As shown in Fig. 3, the effective channel length is reduced as N-Drift doping is increased.

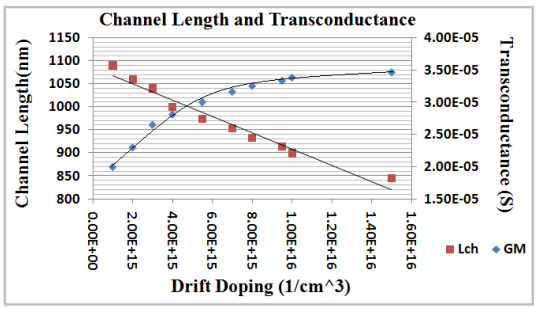

Fig. 3 The variation of L_{ch} and g_m as a function of N-Drfit doping

The on resistance, R_{on}, in this device consists of the channel resistance, R_{ch}, in series with the N-Drift resistance, R_{drift}. R_{on} reduces as a result of decreased channel length and increased N-Drift doping. This results in an increase in the transconductance of the device, g_m, for low values of doping. However, for high doping values, i.e. for values above 5×10^{15} cm^{-3}, the rate of g_m improvement decreases. This is believed to be due to the degradation of the mobility, μ, in the N-Drift region with the increase in N-Drift doping. Fig. 3 also shows the variation of g_m with increase in N-Drift doping.

A second reason for the g_m saturation may be the increased current spreading. Thus the effect of N-Drift doping on the current spreading was examined. At the n+/n of the Drain/N-Drift junction and the n/p of N-Drift/P-Base junction current spreading is expected to be significant. Simulation results reveal that the current spreading at the n+/n junction is larger for low N-Drift doping values. This is because the junction is deeper in this case. However the effect of the current spreading at the p/n junction was found much more significant as compared to the spreading at the n+/n junction. Thus as N-Drift doping is increased, the current spreading at the p/n junction dominates and lowers the g_m improvement rate.

Fig. 4 shows the cut off frequency, f_T , as a function of N-Drift doping. It is seen from this figure that f_T increases and then saturates for increased N-Drift implant dose. This can be explained if we assume the well known small signal equivalent circuit for traditional MOSFET can reasonably model the frequency response of the device [4], even though this approach does not take into account the effect of N-Drift region.

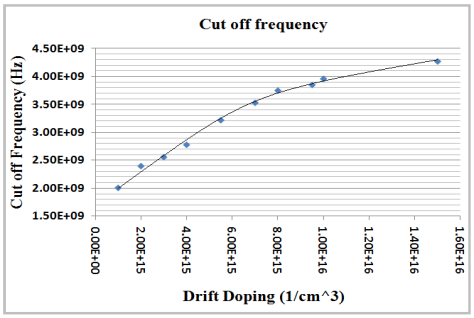

Fig. 4 The variation of f_T as a function of N-Drift doping

Fig. 5, shows the increase in the drain source current, I_{DS}, with an increase in N-Drift doping. As expected, it follows the behaviour of g_m.

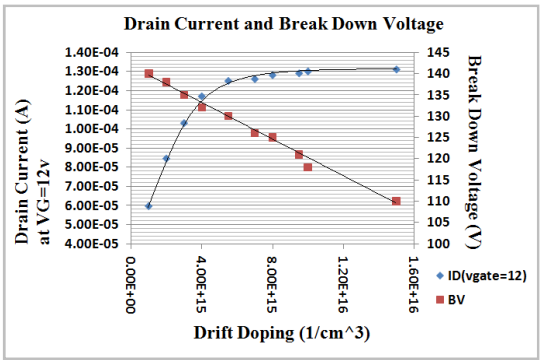

Fig. 5 The variations of ID and BV as a function of N-Drift doping

Fig. 5 also shows the effect of drift doping on the breakdown voltage, BV. Breakdown voltage degrades with the increase in N-Drift Implantation dose.

The rate of change in each of the electrical parameters as a function of N-Drift implant dose is summarized in Table I.

TABLE I
The Rate Of Change In Each Of The Electrical Parameters As A Function Of N-Drift Implantation Dose

Differential values	Low doping	High doping	Unit
$d(f_T)/d(N_{N\text{-}Drift})$	2.53E-07	0.62E-07	Hz/ cm^{-3}
$d(I_D)/d(N_{N\text{-}Drift})$	1.91E-14	6.31E-16	uA/cm^{-3}
$d(BV)/d(N_{N\text{-}Drift})$	-2E-14		V/cm^{-3}

B. P-Base Implant dose

The progression of the depletion layers into the source and N-Drift region due to an increase in P-Base implantation dose

is shown by the constant doping contours in Fig. 6. The increase of P-Base doping results in a reduction of g_m and channel mobility.

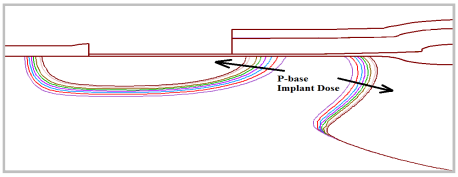

Fig. 6 The constant doping contours showing the increase in L_{ch} as a function of P-Base doping

The variation of channel length as a function of P-Base doping is shown in Fig. 7. This behaviour is expected since as the P-Base doping is increased, the depletion region widths inside the P-Base deceases. The rate of decrease of depletion width however reduces as the P-Base doping is increased. As shown further in Fig. 7, the transconductance decreases for doping values below 4×10^{17} cm^{-3}, then the rate of decrease reduces for higher doping values.

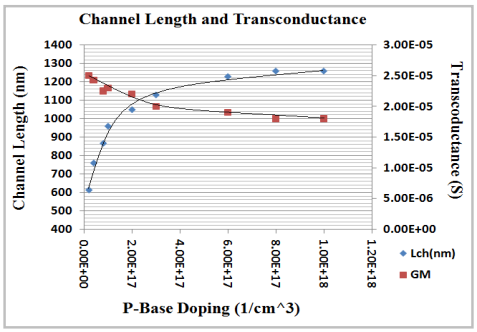

Fig. 7 The variation of L_{ch} and g_m as a function of P-Base doping

Cut off frequency follows the behaviour of g_m. This is depicted in Fig. 8.

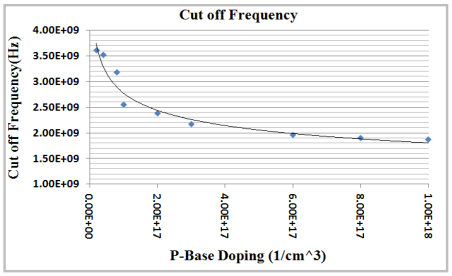

Fig. 8 The decrease of f_T as a function of P-Base doping

The second consequence of increasing the P-Base dose is the reduction of operating current due to a lower channel mobility and a higher threshold voltage.

The variation of drain saturation current as a function of P-Base doping is depicted in Fig. 9.

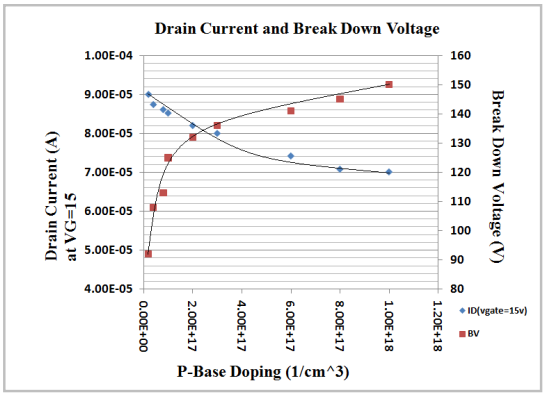

Fig. 9 The variations of I_D and BV as a function of P-Base doping

The drain voltage drops on the P-Base/ N-Drift and N-Drift/P-Substrate depletion regions. Maximum break down is achieved when the two depletion zones reach the critical electric field at the same time. This occurs when the drift region is totally depleted and the electric field profile is flattened. It could be achieved by properly choosing the N-Drift and P-Base dopings and dimensions. In this device as the P-Base doping is increased the depletion region inside the N-Drift region progresses towards the drain end and thus a complete depletion occurs. Accordingly, the area under the electric field profile and the break down voltage increases. Variation of BV with P-Base doping is shown in Fig. 9.

Table II summarizes the effect of P-Base implant dose on the electrical characteristics of the device.

TABLE II
THE RATE OF CHANGE IN EACH OF THE ELECTRICAL PARAMETERS AS A FUNCTION OF P-BASE IMPLANTATION DOSE

Differential values	Low doping	High doping	Unit
$d(f_T)/d(N_{P\text{-}Base})$	-6.83E-9	-0.63E-9	Hz/ cm^{-3}
$d(I_D)/d(N_{P\text{-}Base})$	-6.25E-17	-1.37E-17	uA/cm^{-3}
$d(BV)/d(N_{P\text{-}Base})$	4.12E-16	2.25E-17	V/cm^{-3}

C. Annealing time of N-drift region

Annealing is carried out to activate the implanted dopant atoms. Variation in anneal time, varies the doping profile. In fact, there is a square root dependence between the doping concentration and the anneal time. This dependence is believed to be related to the square root dependence of output characteristics, (see Fig. 12 and Fig. 13) on doping. If these characteristics are plotted as a function of anneal time, they show straight line behaviour. As shown in Fig. 10, as the anneal time increases, due to the dopant diffusion, the N-Drift area enlarges. Furthermore, as shown in Fig. 11, the doping density decreases at the surface and becomes more uniform. The consequences are the increase in R_{on} and also in current spreading.

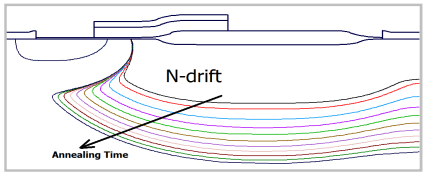

Fig. 10 The constant doping contours show increase of interface area between the P-Base and the N-Drift

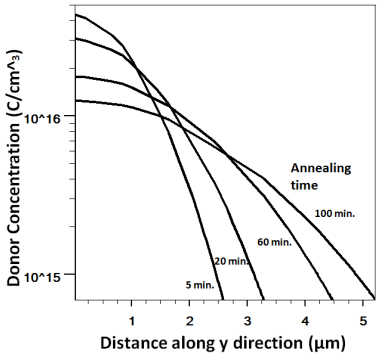

Fig. 11 N-Drift doping profile at the N-Drift surface

Fig. 12 shows the variation of the cut of frequency as a function of N-Drift doping. As the N-Drift doping is increased g_m is reduced. This is consistent with the data in Fig. 4.

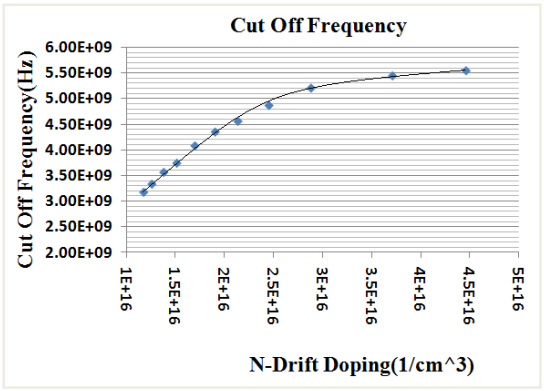

Fig. 12 The degradation of the f_T as a function of N-Drift doping as a result of increase in the N-Drift anneal time

The decrease of saturation drain current with decreased drift doping is shown in Fig. 13. This figure also shows that the BV increases as annealing time of N-Drift region is increased. This increase is due to reduction in N-Drift doping.

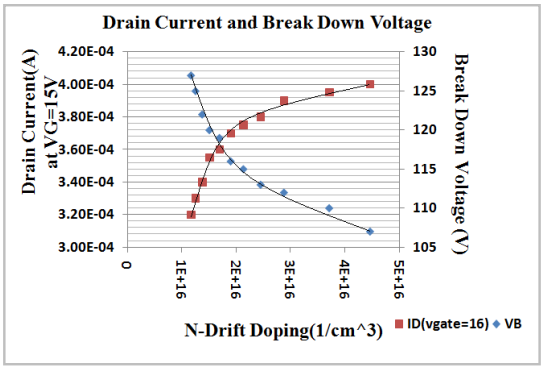

Fig. 13 The variations of I_D and BV as a function of with N-Drift doping as a result of increase in the N-Drift anneal time

The results of parameter variations have been summarized in Table III.

TABLE III
THE RATE OF CHANGE IN EACH OF THE ELECTRICAL PARAMETERS AS A FUNCTION OF N-DRIFT ANNEAL TIME

Differential values	small anneal time(high doping)	Large anneal time(low doping)	Unit
$d(f_T)/d(N_{N\text{-}Drift})$	4.13E-8	1.95E-7	Hz/ cm^{-3}
$d(I_D)/d(N_{N\text{-}Drift})$	1.04E-21	1E-20	uA/cm^{-3}
$d(BV)/d(N_{N\text{-}Drift})$	3.33E-16	2.5E-15	V/cm^{-3}

IV. CONCLUSION

We have examined the impact of variation in several important process parameters on the electrical characteristics of an LDMOS device.

The rate of change in each of the electrical parameters was reported as a function of the change in the process parameters. The results are summarized in tables I, II and III.

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