

The Grinding Influence on the Strength of Fan-Out Wafer-Level Packages

Z. W. Zhong, C. Xu, W. K. Choi

Abstract—To build a thin fan-out wafer-level package, the package had to be ground to a thin level. In this work, the influence of the grinding processes on the strength of the fan-out wafer-level packages was investigated. After different grinding processes, all specimens were placed on a three-point-bending fixture installed on a universal tester for three-point-bending testing, and the strength of the fan-out wafer-level packages was measured. The experiments revealed that the average flexure strength increased with the decreasing surface roughness height of the fan-out wafer-level package tested. The grinding processes had a significant influence on the strength of the fan-out wafer-level packages investigated.

Keywords—FOWLP strength, surface roughness, three-point bending, grinding.

I. INTRODUCTION

THE initial wafer-level packaging is known as the wafer-level chip-scale packaging (WLPCSP) technology [1]. The fan-out wafer-level package (FOWLP) technology [2] is a further development of the WLPCSP technology [3], [4], and its most significant aspect is the fan-out area [5], [6]. The FOWLP I/O numbers are much higher than the WLCSP I/O numbers. The FOWLP [7], [8] can be further developed to 2.5D/3D FOWLP [9], [10] or FO-PoP (package on package) [11], [12] through laser ablation (LSA) or through silicon via (TSV) technology. The FOWLP also shows better thermal-mechanical reliability performance [13], [14] than other packages such as plastic ball grid array (PBGA) packages [15]. The next generation wafer level packaging turns to panel carrier [16], and thus the yield will increase exponentially and the cost will reduce significantly.

There are several methods used to evaluate the silicon strength [17]. However, the 3PB (three-point bending) test is the most popular evaluation method of silicon strength. The effect factors on the silicon strength can be classified into two groups. The first group of effect factor is related to the silicon own profile. The effect factors include the silicon shape, size and thickness. Some research has shown that the silicon own profile factors do not affect the silicon strength obviously and directly [18], [19]. The second group of effect factor is related to the assembly process. The effect factors include the wafer

grinding process and the wafer sawing process. However, there are three widely accepted effect factors of silicon strength: silicon surface defects, silicon edge defects and weak planes of silicon crystal lattice [20].

The silicon surface defects and edge defects are created by the wafer grinding process and wafer sawing process, respectively. The wafer grinding process is the very first process in the whole FOWLP assembly process. The aim of grinding process is to grind the incoming wafer to the required thickness for further processes. The grinding process has three grinding steps [17]. The first grinding step is the normal grinding by fine grit wheels. The second grinding step is the fine grinding by super-fine grit wheels. The third grinding step is the polishing by ultra-fine grit wheels. The roughness of grinding side is fine enough typically after the second grinding step and thus the third grinding step is less used. Beyond the mechanical grinding method, the chemical wet etching and plasma etching methods also can replace the polishing step to gain an ultra-fine wafer surface. In comparison, the plasma etched wafer surface is smoother than the chemical etched wafer surface [21].

The wafer sawing process is conducted after the wafer grinding process. The aim of the wafer sawing process is to saw the incoming wafer to the required size for further processes. There are two wafer sawing methods: mechanical sawing method and laser sawing method [17]. The mechanical sawing method uses diamond blades to saw the wafers. Most wafer sawing tasks could be achieved perfectly by a proper blade selection. The diamond blade collection is broad, and there are different thickness and grit size diamond blades. The laser sawing method is also known as the stealth dicing method [22]. It is because the saw straight of laser sawing is extremely tiny. The saw straight cannot be observed by naked eyes, and it only becomes visible under the high magnification microscope. Therefore, the laser sawing method could offer an extreme low kerf loss [17].

The saw straight of functional wafer is coated. In order to minimize the coating effect on chippings, the laser grooving process is used to remove the coating layer before performing the mechanical sawing [23]. The laser grooving process is similar to the step cut method, and it also can help to reduce chippings.

The mechanical sawing method has the limitation of sawing thin wafers. The machine vibration and cooling water may damage the thin wafers. By contrast, the laser sawing method is quite suitable for the thin wafer sawing. However, the laser beam parameters such as repetition rate and pulse width should be carefully reviewed [24]. The Dicing-by-Thinning

Z.W. Zhong is with the School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore (phone: +65-6790-5588; e-mail: mzwzhong@ntu.edu.sg).

C. Xu is with the School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore. He is also with STATS ChipPAC Pte Ltd, Singapore (e-mail: XUCH0005@ntu.edu.sg, Cheng.XU@Statschippac.com).

W.K. Choi is with STATS ChipPAC Pte Ltd, Singapore (e-mail: WonKyoung.CHOI@Statschippac.com).

(DbT) method [25] can avoid the thin die sidewall and edge defects effectively. The DbT method saws the wafer before the wafer grinding process. However, the DbT method does not cut through the wafer. There are two pre-cut methods. One is mechanical sawing grooves, while the other one is dry etching trenches. However, although both DbT methods improve the thin die strength, the dry etching method is more superior. The pre-cut wafer is bonded to a substrate before the grinding process. Finally, the pre-cut wafer is ground till the dies raise and separate [17].

The grinding patterns lead to the directional behavior of silicon die strength. The silicon die strength depends on the location of silicon die on a wafer [26]. In order to minimize the grinding patterns effect, the polishing process or etching process should be added to the wafer grinding process.

The previous research on silicon strength [27], [28] found out the silicon wafer surface condition is critical to the silicon strength. The processed silicon strength is far lower than the ideal single crystalline silicon strength. The cause is the wafer grinding process. The wafer grinding machine and grinding wheel grit size have limitations. The grinding pattern always appears after the wafer grinding process. The grinding pattern looks like ship propellers, and it also looks like grooves by surface analysis machines. The grinding pattern can assist the loading force once the loading force is parallel with the grinding pattern [17]. The silicon die must be ground to a thinner level so as to build a thin over-molded [29] structure FOWLP [30].

In this research, the effect of the grinding on the FOWLP strength was studied. After grinding, the 3PB [31] was performed, and the FOWLP strength was evaluated by using the flexure strength value.

II. EXPERIMENTS

A. Grinding

We cannot align the molding thickness of artificial wafers with the silicon die thickness. The reason is that the EMC filler size is larger than the over-molded layer thickness [17]. Therefore, the molded-artificial-wafer grinding process cannot be neglected. In this work, we find out whether the grinding process has an effect on the molded wafer strength.

Group F specimens were used to evaluate the grinding process effect on the FOWP strength. Table I shows group F specimen specifications. Group F specimens had only one package size of 8 mm × 8 mm, and one die size of 4.264 mm × 4.264 mm. The die was placed at the geometrical center of the package. The package thickness was 348 μm.

TABLE I
GROUP F SPECIMEN SPECIFICATIONS

ID	Die dimension (mm)			Package dimension (mm)			Grinding wheel
	X	Y	Z	X	Y	Z	
F-1	4.264	4.264	0.32	8	8	0.348	W1
F-2	4.264	4.264	0.32	8	8	0.348	W2
F-3	4.264	4.264	0.32	8	8	0.348	W3
F-4	4.264	4.264	0.32	8	8	0.348	W2+Si etch

There were four sets of specimens, and they were classified by their finishing methods: grinding wheels or finishing processes. Three kinds of grinding wheels were used: W1, W2 and W3. W3 had the finest grits and W1 had the roughest grits. In order to minimize the grit effect, a supplementary process (Si etch) was added. The Si etching process smoothed the surface by a chemical method instead of the mechanical method only. It could make up the grinding limitations and helped to gain a smooth surface. The specimen final thicknesses were the same although they were ground using different wheels and processes.

B. 3PB Testing

All the specimens were placed on the 3PB fixture with their backside facing down. The sample size was 63. The fixture span was 6 mm, and the loading speed was 6 mm/min.

The 3PB test conducted had three key apparatuses. They were a tester machine, a static load cell and a 3PB fixture. The tester used was a universal tester shown in Fig. 1. This machine can be used for static testing such as tensile, compression, flexure and bending tests. The machine load cell is digitalized, and it is controlled by the computer software such as Instron Bluehill3. In this work, the Instron 2530-427 static load cell with maximum ±100 N capacity was applied.

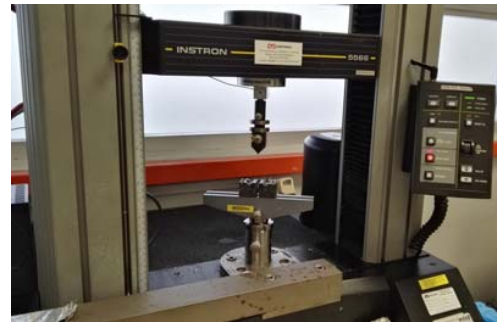


Fig. 1 Instron universal tester 5566



Fig. 2 Customized 3PB fixture

The third key apparatus is the 3PB fixture. The universal tester machine and load cell can implement various testing.

However, the tester fixture decides the testing type and method. Vector Scientific Pte Ltd helped to fabricate the fixture shown in Fig. 2 with a fabrication tolerance ± 0.05 mm. Since the IC chips are tiny and brittle, the fixture maximum load capacity is not required to be too high. However, the fixture must achieve a very narrow span to support the IC chips. In this work, the 3PB fixture is able to achieve a minimum 4 mm span, and the maximum specimen width should be less than 40 mm.

The experiment environment temperature was 25°C. There was not any pre-conditioning or heating device attached to the machine to process the specimens before or during the experiments.

III. RESULTS

The specimens were built by the FOWLP assembly process, and they were designed carefully to fulfill the research objective [17].

The FOWLP strength was investigated through the calculation of the value of flexure strength. We got the specimen fracture load and the specimen extension at the fracture load from the 3PB test. The specimen flexure strength could be then calculated using the following equation [32]

$$\sigma_{3PB} = \frac{3LF}{2BW^2} \quad (1)$$

where F is the fracture load, L is the fixture span, and W and B are the thickness and width of the specimen respectively.

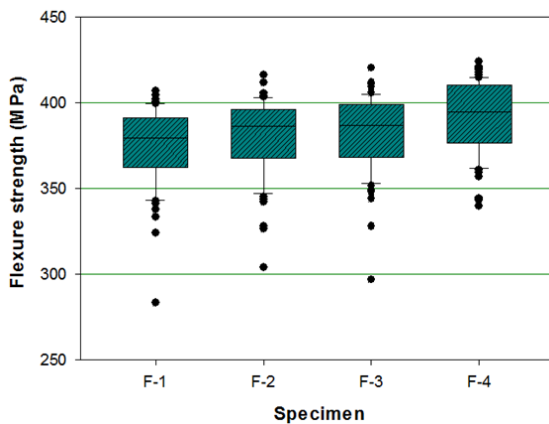


Fig. 3 3PB test flexure strength of group F specimens

TABLE II

WAFER SURFACE ROUGHNESS VALUES OF GROUP F SPECIMENS

Specimen ID	Surface roughness value Ra (μm)
F-1	0.0127
F-2	0.0098
F-3	0.0056
F-4	0.0033

Fig. 3 shows the 3PB-test flexure strength of group F specimens. The average flexure strength increases from specimens F-1 to specimens F-4. Specimens F-4 had the

highest flexure strength, and specimens F-1 had the lowest strength. The flexure strength distributions for all the specimens were almost the same. These specimens were finished by the different grinding wheels or processes. The ground-surface roughness was measured and is listed in Table II. Specimens of F-4 had the finest grinding surface, and specimens of F-1 had the roughest grinding surface. The 3PB test flexure strength had the increasing trend with the decrease of the wafer surface roughness. In other words, the finest surface wafer had the highest flexure strength, and the roughest surface wafer had the lowest flexure strength. Statistical analyses also revealed that the influence of the grinding processes on the FOWLP strength was significant.

IV. CONCLUSION

The experiments revealed that the finest surface wafer had the highest flexure strength, and the roughest surface wafer had the lowest flexure strength. The thin over-molded structure FOWLP could fulfill the requirement of volume sensitive devices.

ACKNOWLEDGMENT

The financial support of this work is provided by the Economic Development Board (EDB) Singapore Industrial Post-graduate Programme research grant. The authors are grateful for the support from EDB Singapore and STATS ChipPAC Pte Ltd.

REFERENCES

- [1] M. Brunnbauer, E. Furgut, G. Beer, and T. Meyer, "Embedded wafer level ball grid array (eWLB)," presented at the Electronics Packaging Technology Conference, 2006. EPTC '06. 8th, 2006.
- [2] C. Xu, Z. W. Zhong, and W. K. Choi, "Numerical and Experimental Study of Fan-Out Wafer Level Package Strength," in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, 2017, pp. 2187-2192.
- [3] Jin Yonggang, X. Baraton, S. W. Yoon, Lin Yaojian, P. C. Marimuthu, V. P. Ganesh, *et al.*, "Next generation eWLB (embedded wafer level BGA) packaging," presented at the Electronics Packaging Technology Conference (EPTC), 2010 12th, 2010.
- [4] S. W. Yoon, Lin Yaojian, S. Gaurav, Jin Yonggang, V. P. Ganesh, T. Meyer, *et al.*, "Mechanical characterization of next generation eWLB (embedded wafer level BGA) packaging," presented at the Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st, 2011.
- [5] Yoon Seung Wook, Lin Yaojian, and P. C. Marimuthu, "Development and characterization of 300mm large panel eWLB (embedded wafer level BGA)," presented at the Microelectronics and Packaging Conference (EMPC), 2011 18th European, 2011.
- [6] M. Prashant, Yoon Seung Wook, Lin Yaojian, and P. C. Marimuthu, "Cost effective 300mm large scale eWLB (embedded Wafer Level BGA) technology," presented at the Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th, 2011.
- [7] K. Pressel, G. Beer, T. Meyer, M. Wojnowski, M. Fink, G. Ofner, *et al.*, "Embedded wafer level ball grid array (eWLB) technology for system integration," presented at the CPMT Symposium Japan, 2010 IEEE, 2010.
- [8] Jin Yonggang, J. Teyseyre, X. Baraton, S. W. Yoon, Lin Yaojian, and P. C. Marimuthu, "Advanced packaging solutions of next generation eWLB technology," presented at the Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th, 2011.
- [9] M. Wojnowski and K. Pressel, "Embedded wafer level ball grid array (eWLB) technology for high-frequency system-in-package applications," presented at the Microwave Symposium Digest (IMS),

- 2013 IEEE MTT-S International, 2013.
- [10] Yoon Seung Wook, J. A. Caparas, Lin Yaojian, and P. C. Marimuthu, "Advanced low profile PoP solution with embedded wafer level PoP (eWLB-PoP) technology," presented at the Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd, 2012.
 - [11] Jin Yonggang, J. Teyssyre, X. Baraton, S. W. Yoon, Lin Yaojian, and P. C. Marimuthu, "Development and characterization of next generation eWLB (embedded Wafer Level BGA) packaging," presented at the Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd, 2012.
 - [12] Yoon Seung Wook, P. Tang, R. Emigh, Lin Yaojian, P. C. Marimuthu, and R. Pendse, "Fanout flipchip eWLB (embedded Wafer Level Ball Grid Array) technology as 2.5D packaging solutions," presented at the Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd, 2013.
 - [13] C. Xu, Z. W. Zhong, and W. K. Choi, "Effect of high temperature storage on fan-out wafer level package strength," in *2017 China Semiconductor Technology International Conference (CSTIC)*, 2017, pp. 1-3.
 - [14] C. Xu, Z. W. Zhong, and W. K. Choi, "Thermal effect on fan-out wafer level package strength," in *2016 IEEE 18th Electronics Packaging Technology Conference (EPTC)*, 2016, pp. 700-703.
 - [15] C. C. Liu, S. M. Chen, F. W. Kuo, H. N. Chen, E. H. Yeh, C. C. Hsieh, *et al.*, "High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration," presented at the 2012 IEEE International Electron Devices Meeting (IEDM), 2012.
 - [16] T. Braun, S. Raatz, S. Voges, R. Kahle, V. Bader, J. Bauer, *et al.*, "Large area compression molding for Fan-out Panel Level Packing," presented at the 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), 2015.
 - [17] C. Xu, "Advanced flip chip and wafer level packages for 2.5D and 3D IC package technology," PhD Thesis, Nanyang Technological University, Singapore, 2018.
 - [18] J D Wu, C Y Huang, and C C Liao, "Fracture Strength Characterization and Failure Analysis of Silicon Dies," *Microelectronics Reliability*, vol. 43, pp. 269-277, 2003.
 - [19] E. Wu, I. G. Shih, Y. N. Chen, S. C. Chen, C. Z. Tsai, and C. A. Shao, "Influence of grinding process on semiconductor chip strength," presented at the 52nd Electronic Components and Technology Conference, 2002.
 - [20] M Y Tsai and C H Chen, "Evaluation of Test Methods for Silicon Die Strength," *Microelectronics Reliability*, vol. 48, pp. 933-941, 2008.
 - [21] H H Jiun, I Ahmad, A Jalar, and G Omar, "Effects of wafer thinning methods towards fracture strength and topography of silicon die," *Microelectronics Reliability*, vol. 46, pp. 836-845, 2006.
 - [22] S. H. Chae, J. H. Zhao, D. R. Edwards, and P. S. Ho, "Effect of Dicing Technique on the Fracture Strength of Si Dies With Emphasis on Multimodal Failure Distribution," *IEEE Transactions on Device and Materials Reliability*, vol. 10, pp. 149-156, 2010.
 - [23] M. Fuegl, G. Mackh, E. Meissner, and L. Frey, "Analytical stress characterization after different chip separation methods," *Microelectronics Reliability*, vol. 54, pp. 1735-1740, 2014.
 - [24] Nitin Sudani, Krishnan Venkatakrishnan, and Bo Tan, "Laser singulation of thin wafer: Die strength and surface roughness analysis of 80 μ m silicon dice," *Optics and Lasers in Engineering*, vol. 47, pp. 850-854, 2009.
 - [25] Stephan Schoenfelder, Matthias Ebert, Christof Landesberger, Karlheinz Bock, and Jorg Bagdahn, "Investigations of the Influence of Dicing Techniques on the Strength Properties of Thin Silicon," *Microelectronics Reliability*, vol. 47, pp. 168-178, 2007.
 - [26] S. H. Chae, J. H. Zhao, D. R. Edwards, and P. S. Ho, "Effect of backside scratch direction on the Si die strength," presented at the 2010 12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2010.
 - [27] Samed Barnat, Helene Fremont, Alexandrine Gracia, and Eric Cadalen, "Evaluation by Three-Point-Bend and Ball-on-Ring Tests of Thinning Process on Silicon Die Strength," *Microelectronics Reliability*, vol. 52, pp. 2278-2282, 2012.
 - [28] L. Zhou, F. Qin, J. Sun, P. Chen, H. Yu, Z. Wang, *et al.*, "Fracture strength of silicon wafer after different wafer treatment methods," presented at the 16th International Conference on Electronic Packaging Technology (ICEPT), 2015.
 - [29] C. Xu, Z. W. Zhong, and W. K. Choi, "Epoxy molding compound effect on fan-out wafer level package strength during post-mold thermal process," in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2017, pp. 1388-1392.
 - [30] C. Xu, Z. W. Zhong, and W. K. Choi, "Thermal test effect on fan-out wafer level package strength," in *2017 12th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2017, pp. 271-274.
 - [31] C. Xu, Z. W. Zhong, and W. K. Choi, "Evaluation of Fan-out Wafer Level Package strength by three-point bending testing," in *2016 IEEE 23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2016, pp. 297-300.
 - [32] Betty Yeung and Tien-Yu Tom Lee, "An Overview of Experimental Methodologies and Their Applications for Die Strength Measurement," *IEEE Transactions on Components and Packaging Technologies*, vol. 26, pp. 423-428, 2003.